Microprocessors, **Microcomputers**, Memories, ADC, DAC, FIP, DTS, ASIC

APPLICATION NOTE

µCOM91

Upgrade from µPD7500x to µPD75000x

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Related Products
µPD750004, µPD750006, µPD750008, µPD75P0016

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Chapter 1 :Contents

Chapter 2 :Introduction

The - over more than 10 years - existing 4-Bit family µCOM75x is now continued by the µCOM75XL family. The 75XL family is an upgrade of the 75x family, using the newest technology.
The first products (75000x and 7530xx) are compatible in functionality to the existing 75x products, upgraded with more features, working with reduced power consumption and at a decreased supply voltage level.

This application note describes the differences between 7500x and 75000x products. This may be useful for users

-> who have experience with 7500x and will recognize the advantages for usage in a new 75XL design.

-> who will transfer an existing 75x design into 75XL. In this case, all items, mentioned in the chapters "Check points when transfer from 7500x -> 75000x" have to be watched seriously to prevent problems.

The application note contains the following chapters:

- **"Contents"** lists the contents of this document.
- **"Introduction"** gives a short introduction.
- The chapter **"Differences reflecting peripheral hardware"** describes the hardware differences and what has to be observed when the 75XL product shall be designed in an existing hardware.
- **"Differences reflecting the software"** describes the software differences and the check points for using an existing ROM code to switch to the new products.
- Chapter **"Additional notes"** adds some information which may be useful.

Chapter 3 :Differences reflecting peripheral hardware

This chapter describes the differences regarding hardware and peripherals:

- the extended operating voltage conditions
- the improved supply current specifications
- the available packages, changes regarding pins and ports

Operating voltage conditions

Operating voltage range from 1.8V to 5.5V

One of the major improvements of the µCOM75XL family is the reduced minimum operating voltage condition (VDD = 1.8V to 5.5V) compared with most of the µCOM75x products (VDD = 2.7V to 6.0V). This allows the usage of lower voltage type batteries or effects in an extended lifetime of the battery. Additionally it gives a wide security range of operation in case of low voltage conditions.

Extended operation speed (tcyc vs. VDD)

The µCOM75XL devices can run with a faster instruction execution time. See a comparison in the table below:

	µPD75008	**µPD75P008**	**µPD750008**	**µPD75P0016**
Supply voltage operation range (VDD)	2.7V to 6.0V	5.0V ± 10 %	1.8V to 5.5V	1.8V to 5.5V
Minimum operating voltage at tcyc = 950 ns (fosc = 4.19 MHz)	4.5V	4.5V	**1.8V**	**1.8V**
Minimum operating voltage at tcyc = 670 ns (fosc = 6.00 MHz)	not possible	not possible	4.5V (target 2.7V)	4.5V (target 2.7V)

Check points when transfer from 7500x -> 75000x

- Take care that the maximum operating voltage does not exceed 5.5V when using 75XL.
- When a resonator is used for main system clock, oscillation will get stable in VDD range : 2.2V ... 5.5V. (Improvement is planned.)
  - Take care that VDD is higher than 2.2V when using 75XL without external main system clock.
  - When VDD = 2.2V ... 2.7V, ceramic resonator has to be 1 ... 5 MHz
    When VDD = 2.7V ... 5.5V, ceramic resonator can be 1 ... 6 MHz
- The recommended oscillator type may differ from that one, recommended for 75x.

Supply current

Reduced power consumption

Due to the new design technology, the µCOM75XL devices have an improved power consumption habit.

See the comparison table below:

Parameter	Conditions	µPD75008	µPD750008
IDD1	fosc = 4.19 MHz VDD = 5.0V high speed mode	2.5 mA typ. 8.0 mA max.	**1.5 mA typ.** **4.0 mA max.**
IDD2	fosc = 4.19 MHz VDD = 5.0V HALT mode	0.5 mA typ. 1.5 mA max.	0.7 mA typ. 2.0 mA max.
IDD3	fosc = stopped 32 kHz subsystem clock operation (tcyc = 122µs) VDD = 3.0V	30 µA typ. 90 µA max.	**6 µA typ.** **18 µA max.**
IDD4	fosc = stopped 32 kHz subsystem clock HALT mode VDD = 3.0V	5 µA typ. 15 µA max.	**3.5 µA typ.** **12 µA max.** **(7 µA max. at Ta = 25° C)**
IDD5	fosc = stopped (STOP mode), no subsystem oscillator VDD = 3.0V Ta = 25° Celsius	0.1 µA typ. 5 µA max.	**0.02 µA typ.** **3 µA max.**

Check points when transfer from 7500x -> 75000x

The reduced supply current should have no negative influence for design - change. There may be some seldom cases, for example a supply current supervisor circuit, where the hardware has to be changed to match to the new conditions.

Package, pins and ports

Available package types

The package types of 7500x and 75000x are compatible:

Family	Product	Extension for package	Package type	Package dimensions without leads	Pin pitch
75x	75004 75006 75008	CU GB	42 pin shrink DIP 44 pin quad flat pack.	16 mm * 40 mm 10 mm * 10 mm	1.78 mm 0.80 mm
75XL	750004 750006 750008				

Differences regarding pins and shared pin functions

The pin configuration is the same in both types, just pin P21 got an additional shared function due to an additional timer.

Pin in CU package	Pin in GB package	7500x	75000x
44	42	P21	P21 / **PTO1**
4	21	X1 low level in STOP mode	X1 **high impedance** in STOP mode
20	38	**N**o **C**onnection (at **NC** - pin) allowed for mask types At programmable types: **VPP**, connect to VDD	**IC** for mask, **connect to Vdd** (Open is not allowed) At programmable types: **VPP**, connect to VDD

Differences regarding ports and electrical characteristics

Port	µCOM75XL series
Software selectable on-chip pull-up resistors	The value is increased , typ. 100 kΩ (µCOM75x series: typ. 40 kΩ @ 5 V).
P0.x, P1.1, P1.2, P1.3, P2.0, P2.2, P2.3, P3.x, P6.x, P7.x, P8.x	No changes compared to µCOM75x series products.
P4.x and P5.x	The N-CH open drain pin withstand 13V instead of 10V in the µCOM7500x series. In opposite to the µCOM75x series in the µCOM75XL series these ports are connected to on-chip pull-up resistors (min. 180kΩ) during the execution of an input instruction.
P1.0 / INT0	Noise elimination circuit can be enabled / disabled by software.
P2.1 / PTO1	Additional shared function (TIMER 1 output signal)

Check points when transfer from 7500x -> 75000x

- When port 2.1 is used as port, there is no difference to 75x. If the software is changed and timer 1 is used for clock output, hardware at pin P21/PTO1 has to be checked / changed.
- Take care that the pin IC is connected to VDD.
- In 75x, X1 pin gets low level (Vss) during STOP- mode.
  In 75XL, X1 pin gets high impedance during STOP- mode. Hardware compatibility has to be proved, especially in case of external clock source for main system clock.
  In 75XL, the STOP mode can be used with external clock supply.
- Port 4 and 5 in 75XL are internally pulled up during read instruction, independent if the internal pull up resistor is selected via mask option or not. Take care that the external connected signal has a low impedance when low level has to be read. Take in account that the power consumption increase slightly during read instruction, compared to 75x.

Chapter 4 :Differences reflecting the software

This chapter describes the differences of software handling.

- Changes in the system clock generation and standby control unit.
- New/changed features of the interrupt pins and the interrupt control unit.
- Additional functions of the watch timer (clock timer).
- Timer/event counter 0.
- New timer/ counter 1 functions.
- The new watch-dog function included in the basic interval timer.
- 75XL products contain more ROM - size.
- Mark mode : MK I / MK II.
- Advanced high end instruction set.
- Special function registers (SFR).
- Stack, stack pointer (SP) and stack bank selection register.
- Program status word (PSW).

System clock and standby control

System clock unit

The system clock unit is the same in both series products in principle.
There are two on-chip oscillators. With SCC register the selection of main or subsystem clock for CPU is done. With PCC register (0FB3 H), several clock frequencies based on the main system clock can be selected.

- 75XL operates faster at low voltage (tcyc = 970ns at VDD = 1.8V).
  Fastest instruction cycle time is 670 ns.
- The maximum oscillator frequency, connected to main oscillator input pin(s) is increased to 6 MHz when VDD is 2.7 ... 5.5V.
- In 75XL, X1 pin gets open drain during STOP mode. Therefore, when external main clock is used, its not necessary to protect the clock feed circuit with additional external hardware.

Main System Clock Selection

- In 75XL an additional speed can be chosen by the PCC register.

PCC1	PCC0	µCOM75x series	µPD75000x
0	0	fx/64	fx/64
0	**1**	**undefined**	**fx/16**
1	0	fx/8	fx/8
1	1	fx/4	fx/4

- In 75XL, the oscillation stable time after reset can be chosen by mask option, either 2^{15} / fx or 2^{17} / fx. (In 75x: 2^{17} / fx is fixed.)

Subsystem Clock Oscillator

Also for the subsystem oscillator the operation conditions have been changed due to the new reduced size technology.

To support a proper low voltage oscillation start-up the subsystem clock circuit has been made selectable in case of impedance (feedback amplifier, see **Figure 1.**).

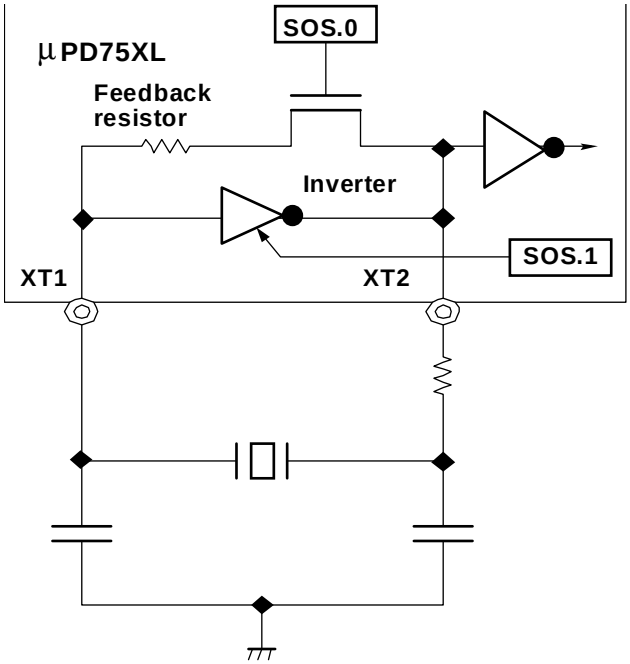

Figure 1. The µCOM75XL Series Subsystem Clock Circuit

Now the user can select a low voltage mode (start-up voltage VDD < 2.7V) and a high voltage mode (start-up voltage VDD ≥ 2.7V) via software in the SOS - register (0FCFH). Additional the subsystem clock feedback resistor can be switched off by software (see **Figure 1.**).

SOS1	SOS0	Operation
0	0	VDD < 2.7V, => normal supply current (IDD)
1	0	VDD ≥ 2.7V, => reduced supply current (IDD)
x	1	feedback resistor switched off, add. reduced supply current (IDD)

- Switching off the feedback resistor do not guarantee that oscillation stops.
- After reset, in 75XL SOS0 = SOS1 = 0, that means feed back resistor is switched on and low voltage subsystemclock oscillation is enabled.

Check points when transfer from 7500x -> 75000x

- The recommended oscillator types may be changed from the 75x recommendation. For details please refer to the related data sheet or contact your NEC sales office.

- Take care that the CPU speed selection, which is undefined in 75x (PCC = 0001), is not selected when the same operation is expected like in the former µCOM75x product.
- If no subsystemclock is used at all, disable feedback resistor via mask option.
- If the 75XL device is working at VDD ≥ 2.7V, set SOS = 1 during initialization routine to reduce power consumption.
- When an external clock source is used for subsystem clock, connect this frequency to XT1, leave XT2 open and disconnect feedback resistor.
- Take care that the mask option for oscillation stabilisation time and feedback resistor is chosen in the same way as in the 75x solution.

Interrupts

- One vectored interrupt (**INTT1**) for the additional on-chip timer / counter is added. Therefore the interrupt vector (**VRQ6**) at ROM address **000C** H and **000D** H is used. The vector can generate an interrupt request and standby release, a new request bit (**IRQT1**) is defined. This interrupt is enabled by **IET1** (bit 3 of 0FBCH).
- One of 6 interrupts can be selected as a high priority interrupt. Selection is done with the new **IPS** (0FB2 H) register. This address is also accessed in 75x devices by DI and EI instruction. In 75x, there is only one bit of the IPS register : FB2.3 = IME used.
- In 75XL interrupt mode register **IM0** defines an additional bit (**IM02**), which enables (0) or disables (1) the noise elimination circuit of the **INT0** input. If the elimination circuit is disabled, this interrupt source is able to make a stand-by release.

Check points when transfer from 7500x -> 75000x

- Confirm that IET1 bit (bit 3 of 0FBC H) is “0” to get the same function like in 75x.
- Please confirm that IPS register (0FB2 H) is not used.
  There is no problem with the state of RESET, no need to set up.
  If user sets IME bit by 4 bit access, please make sure to write only the values # 1000 B or # 0000 B into IPS to get the same operation as in the former used µCOM75x product.
- In case of using the INT0 pin user should check the settings of the IM0 register (0FB4 H). to confirm the same operation (IM0= x0xx) as in the former used µCOM75x product.

Watch timer

Watch timer mode register WM (add.: 0F98H) has two additional bits WM5 and WM4. Setting of these bits enable three different BUZZER output clocks (in 75x there was only one specific clock fixed).

Check points when transfer from 7500x -> 75000x

Take care that bit WM4 and WM5 are set to 0 when the 75XL microcomputer has to have the same operation as in the former used µCOM75x product.

Timer / event counter 0

Prepared for future expansions, bit 0,1 and 7 of the timer 0 mode register TM0 has to be set to 0.

Check points when transfer from 7500x -> 75000x

Confirm that bit 7 of the TM0 register (0FA0 H) is “0”.
Make sure that bit 7 is “0” with TM0 = # 0xxx xx00 B.

One additional timer / counter 1

- A second timer / counter is added. The structure is similar to timer 0. Timer 1 can be clocked with one of four signals generated by the internal clock generator.
- A new timer mode register TM1 and modulo register TMOD1 is available now.
- Interrupt request flag IRQT1 is set when comparator detects that modulo register and counter match to each other.
- Timer Flip Flop match signal can be put out to pin P21/PTO1 when enabled with bit TOE1.

Check points when transfer from 7500x -> 75000x

Confirm that TM1 register (0FA8 H) is not used.
There is no problem with the state of RESET, no need to set up.

The new watch-dog function of the basic interval timer

The fundamental functions and the selection of frequencies using BTM register are the same as in 75x types.

- Additionally a watch-dog timer mode is included in 75XL. It generates an internal hardware reset when enabled by software once.
  By setting the WDTM - bit (add.: 0F8BH) using the one bit set command SET1 WDTM, the basic interval timer generates an internal hardware reset when basic interval timer overflow occurs.
  After watch-dog occurrence all ports and registers are in the status after reset.

  The WDTM-bit can be set to 1 via software, but not cleared (set to 0) via software!
  After Reset WDTM = 0, that means no reset after basic interval timer overflow.

- The power on oscillator stabilization time after reset can be selected by mask option (two timings: 2^{15} / fx or 2^{17} / fx).

Check points when transfer from 7500x -> 75000x

- Confirm that WDTM register (0F8B H) is not used. There is no problem with the state of RESET, no need to set up.

- Confirm that the mask option for stand by release time is set to 2^{17} / fx to get the same stand by release time as in the former used µCOM75x product.

ROM - size in 75XL products

- In 75XL, the ROM-size values, available for the user are real mathematical “k” - units, in 75x usually less user - ROM - size is available:

750004	:	4096 * 8 Bits	(75004	4096 * 8 Bits)
750006	:	6144 * 8 Bits	(75006	6016 * 8 Bits)
750008	:	8192 * 8 Bits	(75(P)008	8046 * 8 Bits)
75P0016	:	16384 * 8 Bits		

- Location of Reset, Interrupt Vector and GETI-Instruction start address have not changed in principal. INTT1 start address (000C H + 000D H) is added.
  For the interrupt-start addresses refer to the device related documents.

Check points when transfer from 7500x -> 75000x

Due to unused interrupt start addresses can be used as usual ROM - size there should be no problem to change to 75XL.

Mark mode: MK I / MK II

The selection of one of these modes specifies the available ROM - size of the product. It is done with bit SBS.3 in SBS register (0F84 H).

SBS.3 = 1: ROM-size ≤ 16k (MK I)
SBS.3 = 0: ROM-size > 16k (MK II)

- After reset SBS.3 = 1, that means MK I - mode. For 75XL series products, where more than 16k ROM- size is used, MK II has to be selected via software.

The differences between MARK MKI and MARK MKII operation are listed in the table below:

Operation	**MK I - mode**	**MK II - mode**
RA75X Assembler command line option	-M1	-M2
SBS.3 setting	1 (RESET condition)	0
Operable ROM size	max. 16k byte	≥ 16k byte
Subroutine “Call “ stack operation	2 byte stack operation	3 byte stack operation
CALL !addr	3 machine cycles	4 machine cycles
CALLF !faddr	2 machine cycles	3 machine cycles
BRA !addr	not available	available
CALLA !addr	not available	available

- To proof and allow the additional instructions within the assembler package, the mark - mode has to be selected during assembler call in the following format:
  > **RA75X** *filename* **-C** *processor type* **-M1** (respectively **-M2**)

- For 75x devices, mark M1, M2 - mode - selection is not available.

Check points when transfer from 7500x -> 75000x

- Confirm that SBS register (0F84 H) is not used.
  There is no problem with the state of RESET (SBS = 1000 B), no need to set up.
- To get the same functionality, select the MK I mode during assembler call:
  > **RA75X** *filename* **-C** *processor type* **-M1**

Advanced High End instruction set

The 7500x devices are equipped with the standard instruction set (105 instructions). 75XL offers the Advanced High End instruction set with 145 instructions. The standard instructions are included in the advanced high end one so that all existing 75x software can also run on 75XL.
The 75XL instructions include the following advantages:

- The 8 bit and 1 bit instructions of the High End instruction set
- Four register banks instead of one in 7500x
  Therefore the SEL RBn -instructions are valid for selection of the actual register bank. The register bank is selected in RBS - register (0F82).
- 16 Bit indirect addressing:
  BR BCDE
  BR BCXA
- 16 Bit table addressing:
  MOVT XA,@BCDE
  MOVT XA,@BCXA
- In MK II mode the following instructions are also available:
  BRA !addr
  CALLA !addr

For details please refer to the device related users manual.

Check points when transfer from 7500x -> 75000x

- Confirm that RBE bit (PSW: 0FB0 H) is “0”.(Only register bank 0 is used)
  Please make sure that RBE= # 0 B and all RBE bits of vector addresses are “0”.
- Confirm that RBS register (0F82 H) for register bank selection isn’t used.
  There is no problem with the state of RESET, no need to set up.

Special function registers (SFR)

Like in 75x the special function registers (SFR) are located in memory bank15. The fundamental functions and handling is the same like in 75x series. In 75XL, there are some additional special function registers / bits. Most of the registers can be read additionally. For details please refer to the device related users manual.

Check points when transfer from 7500x -> 75000x

- Confirm that the special function registers / bits which are not available / not defined in 75x are not accessed in the software which will be transferred to 75XL.
- In this application note, hints for several special function registers / bits are discussed under separate items.

Stack, stack pointer (SP) and stack bank selection register

Functionality, habit and address of the SP is the same like in 75008. Due to 8 bit stack address-register SP, the stack is fixed onto the selected register bank. During decrement of SP contents gets...x02H, x01H, x00H, xFFH,... (same like in 75x).

- In 75000x the stack can be placed in one of the two memory banks 0, 1. This is selected by the SBS-register, bit 0 and 1. The stack is not fixed on memory bank 0 like in 7500x.
- In mark II - mode (MKII), during CALL instructions one byte more stack area is automatically used. Therefore, more stack area has to be expected.

Check points when transfer from 7500x -> 75000x

Due to SBS is set to 1000 B during reset, memory bank 0 is selected automatically.
Furthermore, stackpointer (SP) has to be defined in 75x also.
Due to directly transferred software should run in MKI - mode, the stack area, used in 75x is the same as in 75XL.

- Confirm that SBS register (0F84 H) is not used in the existing software.

Program status word (PSW)

The address (0FB0 H) in the SFR´s is the same like in 75x.

- Two bits (RBE and IST1) are added and handled during stack operation (RBE store/restore) respectively. Interrupt handling (IST1 set/reset).
- Due to High End instruction set, the MOV1 instructions can manipulate carry -flag (CY) additionally.

Check points when transfer from 7500x -> 75000x

Take care that RBE = IST1 = 0 during program run when the same function is expected like in 75x.

Chapter 5 :Additional Notes

Additional mask option

In 75XL, the oscillation stabilization time after reset can be chosen by mask option, either 2^{15} / fx or 2^{17} / fx.
In 75x: the oscillation stabilization time after reset is fixed to 2^{17} / fx.

Check points when transfer from 7500x -> 75000x

- Confirm that the mask option for stand by release time is set to 2^{17} / fx to get the same stand by release time as in the former used µCOM75x product.

Development tools

The following environment is necessary to develop µPD75000x:
Hardware (in circuit emulator) :

IE-75000-R (or IE-75001-R) + IE-75300-R-EM

Software :

- Assembler package RA75X, Version 4.50 or higher
  including the "**75XL definition files**"
- For debugging the Advanced Full screen Debugger (AFD) version 2.0x or higher can be used.

Final test using OTP - version

Please evaluate software, assembled by 75XL, using µPD75P0016.

Influence of the reduced design structure

Changed EMI behavior

Due to the reduction of the design structure down to 0.8µm technology, the high frequency conditions have changed related to the µCOM75x series products. This may have influence to the EMI conditions of an existing design, if the µCOM75XL product replaces a µCOM75x product without hardware changes.

How to proceed for EMI certification

Execute all EMI test procedures, necessary for your EMI quality certification using an 75XL One-Time-Programmable version (OTP).

Note: Do not use UV - erasable versions for EMI testing.

The EMI behavior of an OTP is different to that of a mask ROM type. This should be taken into account to qualify the test results. The differences are:

- EMR (radiation of OTP > radiation of mask ROM type due to more switching current of PROM data drivers)
- EMS (sensitivity of OTP < sensitivity of mask ROM type, due to an extended high voltage protection for programming operation; sensitivity ratio approximately: 1 : 1.3)

How to improve EMI resistance (application experiences)

To improve EMI resistance the following methods have given good results:

- Software:
  - Program application sensitive functions cyclic. Especially those ones which are normally set once (initialization procedure) or those which have influence to other program parts or those which have influence to a correct operation of the product Typical examples are LCD control registers and port mode registers.

  - Take into account, that input signals can be corrupted by strong spike signals. So it may happen, that an analog signal is detected wrong.

  - Take into account, that interrupt signals can be executed unconditionally by external spikes.
- Hardware:
  - Do not leave unused pins unconnected. Please refer to the description of recommended pin connections for unused pins.

  - Take into account, that a strong spike can change the port mode register. This can set an output programmed port into input state and vice versa. So connect unused pins with a pull-up or pull-down resistor, do not connect several pins at the same resistor. If this is not possible, program the port mode registers in short cycles.

  - The oscillator circuits are sensitive parts of a digital clocked device. The resistance is depends on the PCB layout and the nominal operation frequency of the circuit. Most sensitive are low frequency oscillators (e.g. the subsystem clock oscillator of

the µCOM75x/XL series). To reduce malfunctions, keep oscillator connections as short as possible to the device and keep signals far away, which may have a high current flow (e.g. switching of a relay). Furthermore avoid long wires at your PCB, this could effect like an antenna.

- Build so called guarded ground areas around sensitive parts like oscillator circuits or analog areas.

- In some cases a ground resistor can reduce the EMS sensitivity of the main oscillator (see figure below). But please note, that this have influence to the nominal operation of the oscillator. In this case contact you resonator/crystal manufacturer for support or specification.