Contents

1 Introduction

This application note covers layout guidelines and application details for the ZSPM401x family of DC/DC synchronous switching regulators. The ZSPM401x provides fully integrated power switches, internal compensation, and full fault protection for a broad range of applications. Depending on the product version, the output can either be a fixed value or an adjustable voltage determined by external components. Typical applications include wireless access points; cable modems; printers; set-top boxes; supplies for DVDs, LCDs, and LEDs; and portable products including GPS devices, smart phones, and tablet PCs.

2 Typical Application Schematic

The typical ZSPM401x application circuit for the product version with an adjustable output (ZSPM401xBA1W00) includes bypass capacitors on the VCC input pin, a resistive voltage divider to set the voltage on the FB feedback pin, an optional pull-up resistor for the power-good signal on the PG pin, a bootstrap capacitor on the BST pin, an output inductor, output filtering capacitors, and an optional output diode for improving load regulation and efficiency. (See Figure 2.1.)

The typical ZSPM401x application circuit for the product version with a fixed voltage output is the same except the voltage divider is not used and the FB feedback pin is connected directly to V_{OUT}. (See Figure 2.2.)

Refer to the *ZSPM401x Data Sheet* for requirements and recommendations for external components.

Figure 2.1 ZSPM4011/12/13 Application Schematic for Adjustable Output ZSPM401xBA1W00

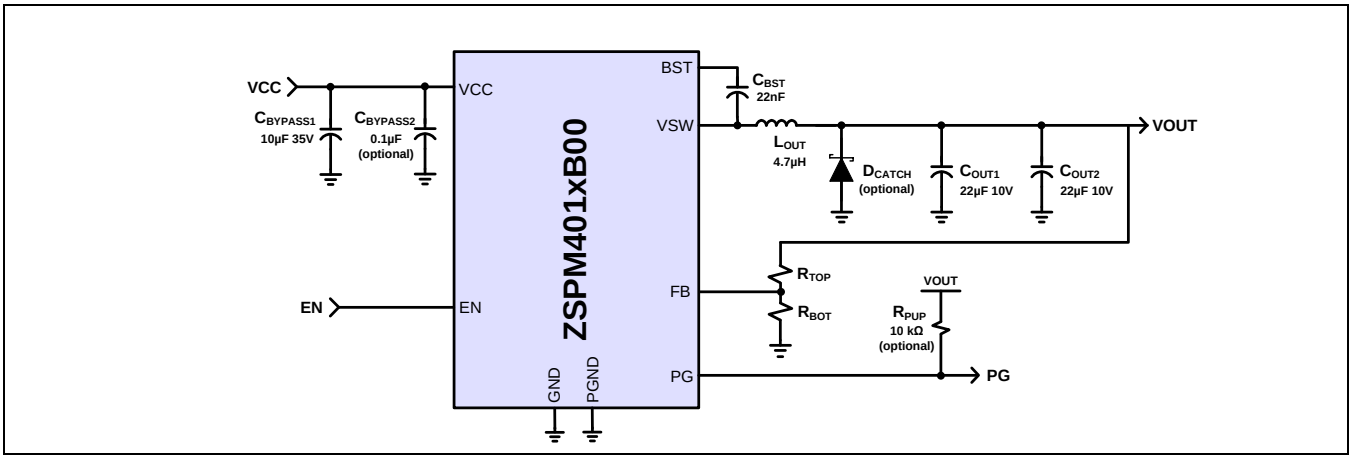
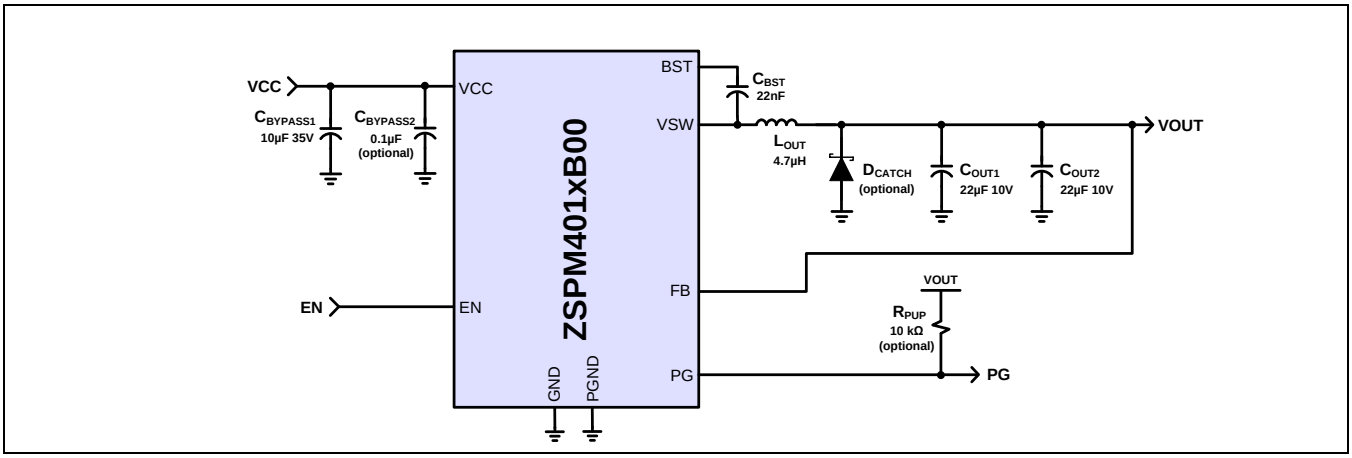


Figure 2.2 ZSPM4011/12/13 Application Schematic for Fixed Voltage Output



3 Printed Circuit Board (PCB) Layout Guidelines

For proper operation and minimum EMI, care must be taken during PCB layout. An improper layout can lead to issues such as poor stability and regulation, noise sensitivity, and increased EMI radiation. Figure 3.1 provides an example of a proper layout for the adjustable output version of the ZSPM401x.

The main guidelines are the following:

- Provide low inductive and resistive paths for loops with high di/dt
- Provide low capacitive paths with respect to all the other nodes for traces with high di/dt
- Ensure that sensitive nodes not assigned to power transmission are referenced to the analog signal ground (GND) and always separated from the power ground (PGND)

The negative ends of C_{BYPASS}, C_{OUT}, and the optional Schottky diode D_{CATCH} should be placed close to each other and connected using a wide trace. Use vias to connect the PGND node to the ground plane. To avoid additional voltage drop in traces, place the PGND node as close as possible to the ZSPM401x PGND pins.

Place the bypass capacitor C_{BYPASS} (optionally paralleled to a 0.1µF capacitor) as close as possible to the VCC pins of ZSPM401x.

In order to minimize the area between the VSW pins and the output components (L_{OUT} and C_{OUT}), place the inductor close to the VSW pins and connected directly to V_{OUT}, the output inductor L_{OUT}, the output capacitor C_{OUT}, and the PGND pins. Minimize the trace area and length of the switching nodes VSW and BST.

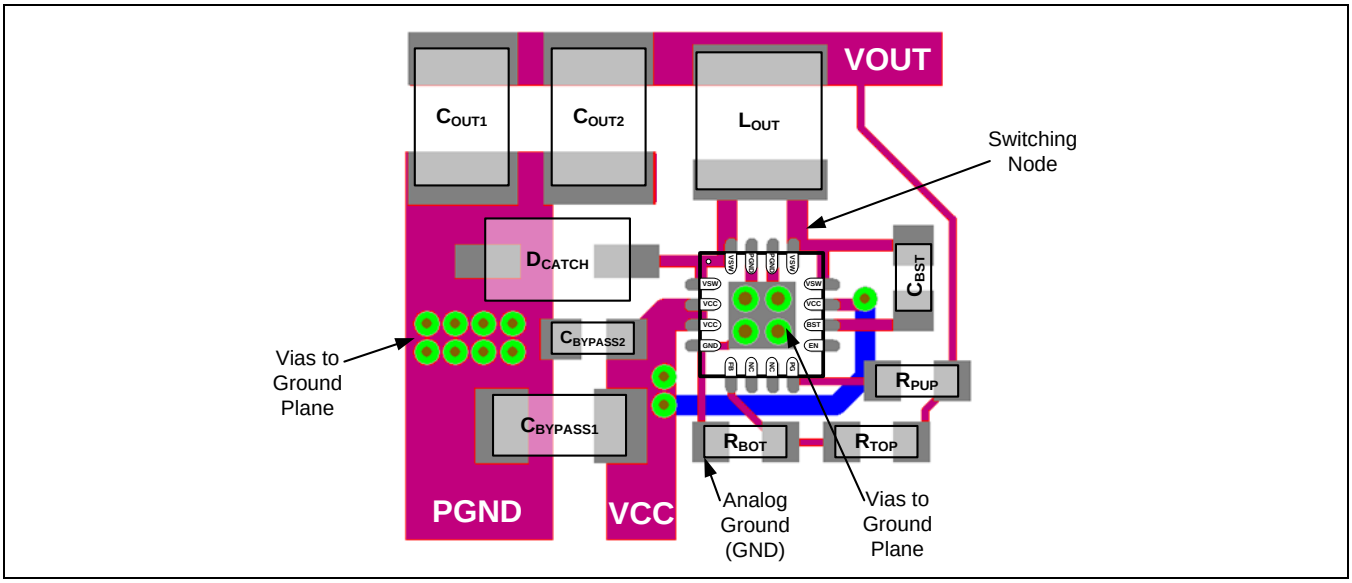
Keep the traces of the sensitive node FB as short as possible and away from switching signals. For the adjustable output voltage version of the ZSPM401x, feedback resistors R_{BOT} and R_{TOP} are required and should be placed close to the ZSPM401x. R_{BOT} must be connected to the analog ground pin (GND) directly and must never be connected to the ground plane. The analog ground trace (GND) should be connected in only one point to the power ground (PGND). A good connection point is the exposed thermal pad and vias under the ZSPM401x package, which are connected to PGND. Use a trace that ends close to the actual load to connect R_{TOP} to the V_{OUT} node.

Connect the FB pin directly to V_{OUT} for fixed output voltage versions of the ZSPM401x where R_{BOT} and R_{TOP} are not required.

The exposed thermal pad must be soldered to the PCB for mechanical reliability and to achieve good power dissipation. Vias must be placed under the pad to transfer the heat to the ground plane.

Figure 3.1 provides an example of a layout for an application board that follows these guidelines and is designed for the adjustable output version of the ZSPM401xB. See section 4 for recommended parts for this layout.

Figure 3.1 ZSPM401X PCB Example Layout, Top View for Adjustable Output Version ZSPM401xBA1W00



4 Recommended Bill of Materials

Table 4.1 provides recommended values and possible sources for external components for a typical application circuit. As discussed in section 6, the ZSPM401xB Evaluation Board in the ZSPM401xB Evaluation Kit is an example of a typical application circuit. Table 4.1 correlates the parts on the Evaluation Board (see Figure 6.1) with components in Figure 2.1. “NL” (no linkage) indicates the component is not placed on the Evaluation Board. Components marked with an asterisk (*) are only used with the adjustable versions of the ZSPM401x.

Table 4.1 External Components and Sources

Evaluation Kit Reference	Functional Reference	Functional Description	Part	Footprint	Manufacturer	Manufacturer P/N
C1	$C_{BYPASS1}$	Input Supply Bypass Cap.	10µF	0805	TDK	C2012X5R1E106M
C2	$C_{BYPASS1}$	Input Supply Bypass Cap.	10µF	0805	TDK	C2012X5R1E106M
	$C_{BYPASS2}$	Bypass Capacitor (optional)	0.1µF	Use if $C_{BYPASS1}$ ≠ low ESR ceramic cap. NL on Eval. Board.		
C3	C_{BST}	Boost Capacitor	22nF	0603	TDK	C2012C0G1E223J
C4	C_{OUT1}	Output Filter Capacitor	22µF	0805	Murata	GRM21BR60J226ME39L
C5	C_{OUT2}	Output Filter Capacitor	22µF	0805	Murata	GRM21BR60J226ME39L
C6			NL	0603		
D1	D_{CATCH}	Catch Diode (optional)	Schottky	Recommended for ZSPM4013BA1Wxx. NL on Eval. Board.		
L1	L_{OUT}	Output Filter Inductor	4.7µH		Wurth	7447779004
R1	R_{TOP}	Voltage Feedback Resistor*	6.04kΩ	0603	Susumu	RR0816P-6041-D-76H
R2.1	R_{BOT}	Voltage Feedback Resistor*	NL	0603		
R2.2	R_{BOT}	Voltage Feedback Resistor*	53.6kΩ	0603	Susumu	RR0816P-5362-D-71C
R2.3	R_{BOT}	Voltage Feedback Resistor*	17.8kΩ	0603	Susumu	RR0816P-1782-D-25C
R2.4	R_{BOT}	Voltage Feedback Resistor*	9.09kΩ	0603	Susumu	RR0816P-9091-D-93H
R2.5	R_{BOT}	Voltage Feedback Resistor*	6.04kΩ	0603	Susumu	RR0816P-6041-D-76H
R2.6	R_{BOT}	Voltage Feedback Resistor*	3.40kΩ	0603	Susumu	RG1608P-3401-B-T5
R2.7	R_{BOT}	Voltage Feedback Resistor*	2.26kΩ	0603	Susumu	RG1608P-2261-B-T5
R2.8	R_{BOT}	Voltage Feedback Resistor*	1.33kΩ	0603	Welwyn	PCF0603R-1K33BT1
R3	R_{PUP}	PG Pin Pull-up Resistor	10kΩ	0603	Required if PG is used. NL on Eval. Board	
U1		ZSPM401x DC/DC Regulator	ZSPM401XB	QFN 3mm x 3mm x 1mm	IDT	ZSPM401xBA1Wxx (ZSPM401xBA1W00 is used on the Eval. Bd.)

5 Component Selection

The 1MHz internal switching frequency of the ZSPM401x facilitates low-cost LC filter combinations. The fixed output versions allow a minimum external component count while providing a complete regulation solution with only four external components: an input bypass capacitor, an inductor, an output capacitor, and the bootstrap capacitor. The internal compensation is optimized for a total of 44µF of output capacitance and a 4.7µH inductor.

For best performance, a low ESR ceramic capacitor should be used for C_{BYPASS}. If C_{BYPASS} is not a low ESR ceramic capacitor, a 0.1µF ceramic capacitor should be added in parallel to C_{BYPASS}.

The minimum allowable value for the total output capacitance is 33µF. To keep the output ripple low, a low ESR (less than 35mΩ) ceramic is recommended. Multiple capacitors can be used in parallel to reduce the ESR.

The inductor range is 4.7µH +/-20%. For optimal over-current protection, the inductor should be able to handle up to the regulator current limit without saturation. Otherwise, an inductor with a saturation current rating higher than the maximum I_{OUT} load requirement plus the inductor current ripple should be used.

For high current modes (3A for example), the optional Schottky diode D_{CATCH} will improve the overall efficiency and reduce heat. It is up to the user to determine the cost/benefit of adding this additional component in the user's application. The diode is typically not needed.

For the adjustable output version of the ZSPM401x, the output voltage can be adjusted by sizing the R_{TOP} and R_{BOT} feedback resistors. The equation for the output voltage is

$$V_{OUT} = 0.9 \times \left(1 + \left(\frac{R_{TOP}}{R_{BOT}}\right)\right)$$

.

For the adjustable version, the ratio of VCC/V_{OUT} cannot exceed 16.

The 10kΩ pull-up resistor R_{PUP} is only required when the Power Good signal (PG) is utilized. The recommended tolerance is 0.5%.

The value of the bootstrap capacitor C_{BST} for the high-side FET gate driver is 22nF. Connect the capacitor from the BST pin to the VSW pin as shown in Figure 2.1.

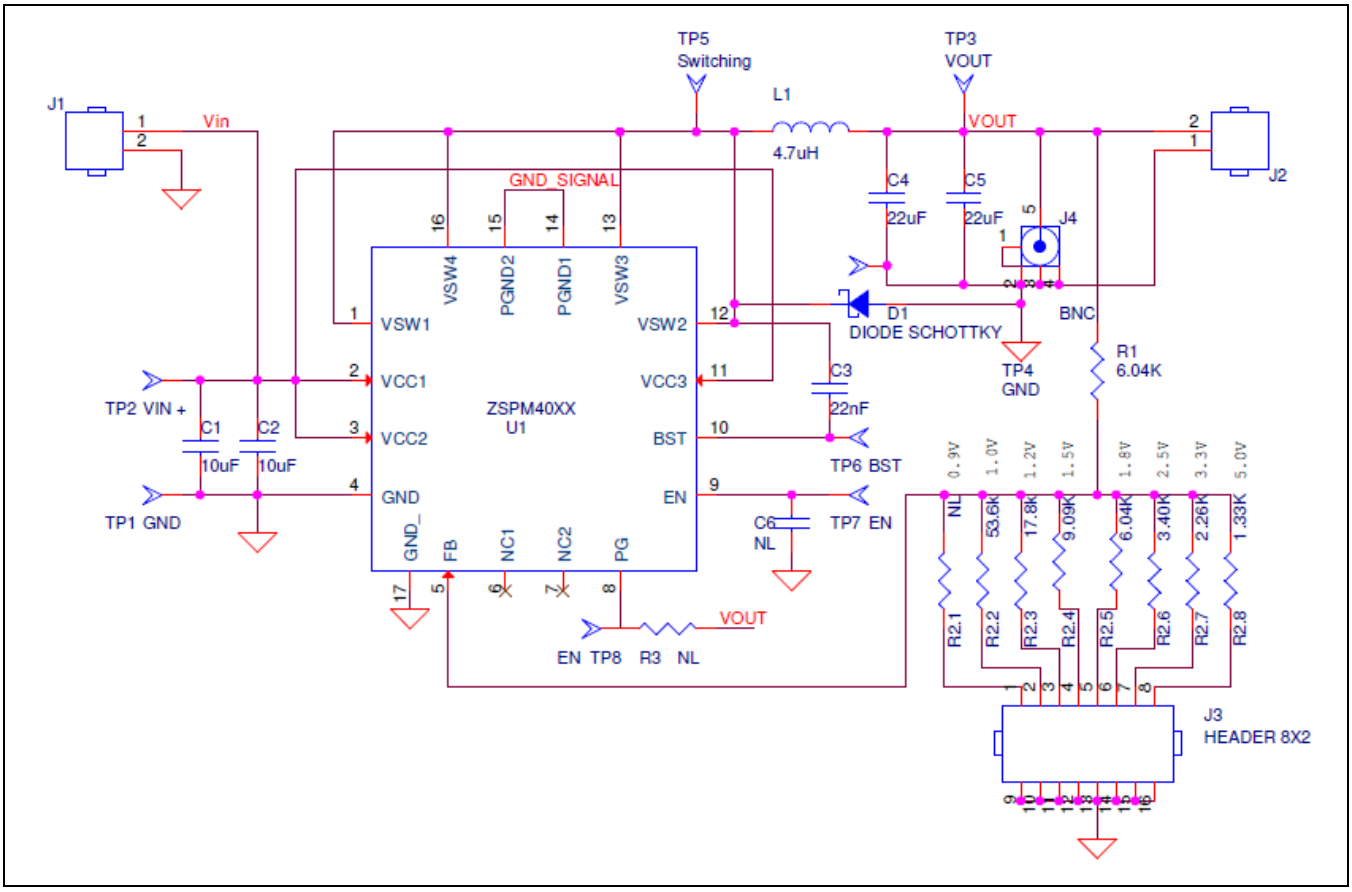
6 ZSPM401x Evaluation Board Example

The ZSPM401x Evaluation Kit uses a board that provides a good example of proper layout and component selection. It is designed to allow evaluating various combinations of the voltage divider feedback resistors (R1 and R2.x) and input/output capacitors. Refer to the *ZSPM401x Evaluation Kit Description* for details.

6.1. Input Capacitor Selection for Evaluation Board Example

There are two locations, C1 and C2, for the input capacitors on the Evaluation Board to evaluate different ESR and capacitances for the application. One of these capacitors should be a low ESR ceramic type, with a recommended minimum value of 10µF. See Table 4.1 for the capacitor values, suppliers, and part locations.

Figure 6.1 Schematic for ZSPM401x Evaluation Board as an Application Circuit Example



6.2. Output Capacitor Selection for Evaluation Board Example

There are two locations, C4 and C5, for the output capacitors on the Evaluation Board. Low ESR single or parallel ceramic capacitors are recommended to keep the output ripple low. However, other capacitors can be evaluated. One capacitor should be of low ESR ceramic type.

7 Thermal Consideration

ZSPM401x is designed for a maximum operating junction temperature T_j of 125°C. The maximum output power is limited by the power losses that can be dissipated over the thermal resistance given by the package and the PCB structures. The PCB must provide heat sinking to prevent overheating of the ZSPM401x. The exposed metal on the bottom of the QFN package must be soldered to a ground plane. It is strongly recommended that the ground be tied to other copper layers below with thermal vias. Adding more copper to the top and the bottom layers and tying this copper to the internal planes with vias can reduce thermal resistance further. For a hi-K JEDEC board and 13.5 square inch of 1 oz. copper, the thermal resistance from junction to ambient can be reduced to θ_{JA} = 38°C/W.

The power dissipation of other power components (catch diode, inductor) cause additional copper heating and can further increase the effective ambient temperature of the ZSPM401x.

8 Document Revision History

Revision	Date	Description
1.00	January 23, 2012	First release.
1.10	January 28, 2012	Content update
1.20	July 10, 2013	Updates for schematic and bill of materials. Updates for contact information and imagery on cover and headers.
	April 12, 2016	Changed to IDT branding.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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