Interface IP

MIPI CSI-2 Receiver IP Core

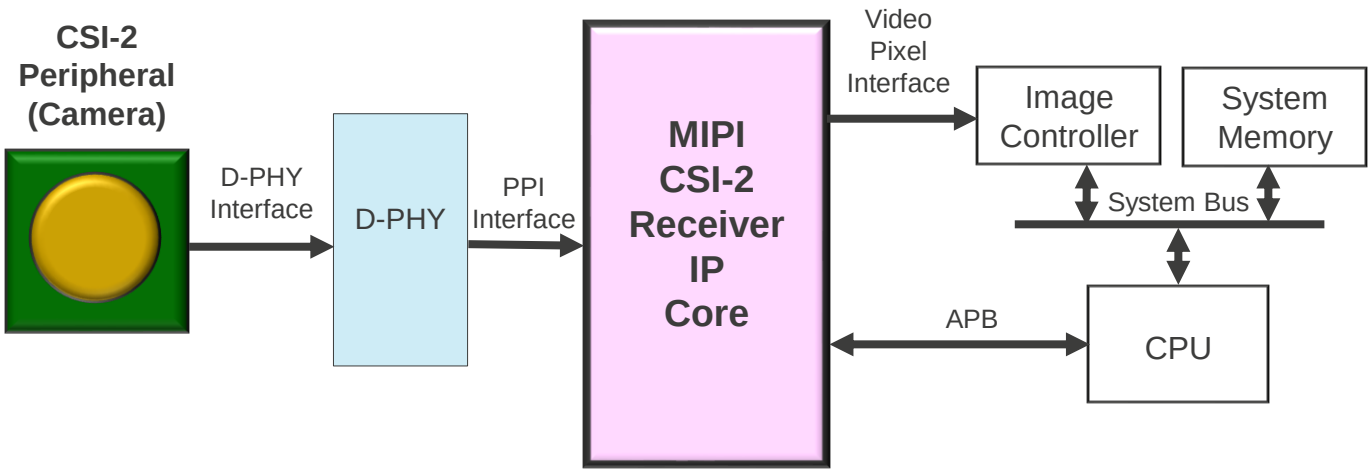
Overview

The Renesas CSI-2® Receiver IP is compliant with the Specification for Camera Serial Interface 2 (CSI-2). This IP can be implemented in CSI-2 host processor (baseband, application engine), act as receiver of image/sensor data.

Features

- Compliant with Specification for Camera Serial Interface 2 (CSI-2®) Version 3.0.
- Compliant with PHY Protocol Interface (PPI) to D-PHY℠ Version 2.5.
- Compliant with AMBA® APB Protocol Version 2.0.
- Support PPI interface for D-PHY physical layer option.
- Support Renesas original Video Pixel Interface.
- Support APB interface for register access.

Block Diagram



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Functions

CSI-2 Receiver function

- Support 1,2,4 D-PHY lanes.
- Support 80 Mbps to 4.5 Gbps per lane.
- Support all primary and secondary CSI-2 data format.
- Support 16 virtual channels.
- Support data interleaving.
  - Data Type Interleaving.
    - Packet Level Interleaved Data Transmission.
    - Frame Level Interleaved Data Transmission.
  - Virtual Channel Identifier Interleaving.
- Support Latency Reduction and Transport Efficiency (LRTE).
  - Support D-PHY EPD option2.
  - Support variable-length Spacer detection under D-PHY EPD option2.
  - Support End-of-Transmission Short Packet (EoTp) detection.
- Support ECC 1bit error correction and 2bit error detection in packet header.
- Support CRC check for payload data.
- Support Data De-Scrambling.
- Support Receiver Error Detection and report.
  - D-PHY Level errors.
  - Packet Level errors.
  - Protocol Decoding Level errors.

APB Slave Function

- Support 32bit data bus.

Sub Block Diagram