2.5V ZERO DELAY CLOCK MULTIPLIER, SPREAD SPECTRUM COMPATIBLE

IDT23S08T
ADVANCE INFORMATION

FEATURES:

- **Phase-Lock Loop Clock Distribution for Applications ranging from 10MHz to 133MHz operating frequency**
- **Distributes one clock input to two banks of four outputs**
- **Separate output enable for each output bank**
- **External feedback (FBK) pin is used to synchronize the outputs to the clock input**
- **Output Skew <200 ps**
- **Low jitter <200 ps cycle-to-cycle**
- **1/2x, 1x, 2x, 4x output options (see table):**
  - *IDT23S08T-1 1x*
  - *IDT23S08T-2 1x, 2x*
  - *IDT23S08T-3 2x, 4x*
  - *IDT23S08T-4 2x*
  - *IDT23S08T-5 1/2x*
- **No external RC network required**
- **Operates at 2.5V VDD**
- **Spread spectrum compatible**
- **Available in SOIC package**

DESCRIPTION:

The IDT23S08T is a high-speed phase-lock loop (PLL) clock multiplier. It is designed to address high-speed clock distribution and multiplication applications. The zero delay is achieved by aligning the phase between the incoming clock and the output clock, operable within the range of 10 to 133MHz.

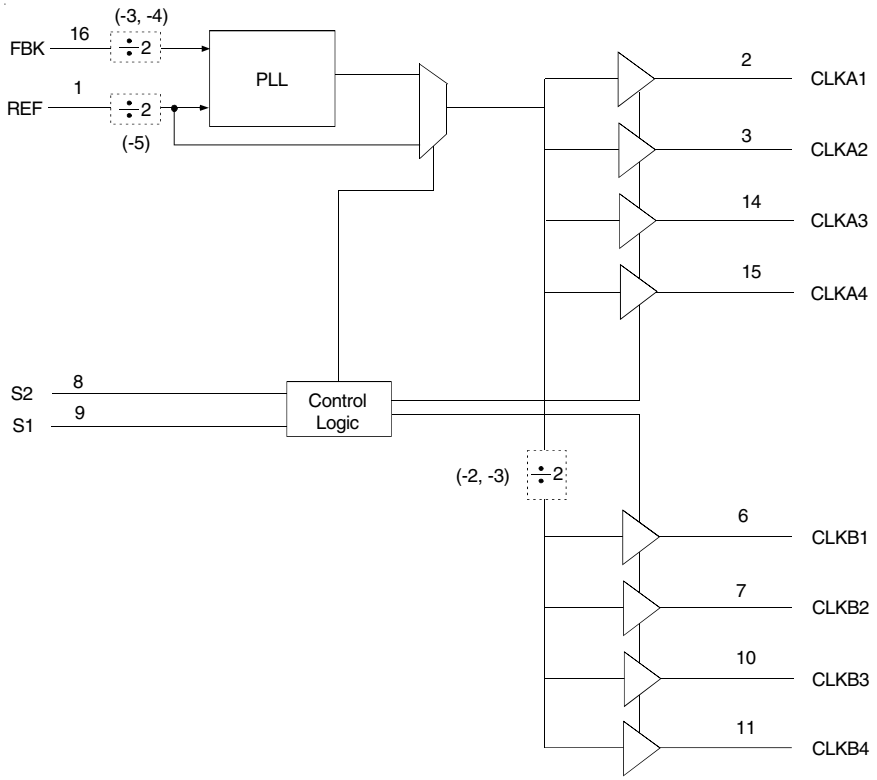
The IDT23S08T has two banks of four outputs each that are controlled via two select addresses. By proper selection of input addresses, both banks can be put in tri-state mode. In test mode, the PLL is turned off, and the input clock directly drives the outputs for system testing purposes. In the absence of an input clock, the IDT23S08T enters power down. In this mode, the device will draw less than 12µA, and the outputs are tri-stated.

The IDT23S08T is available in six unique configurations for both prescaling and multiplication of the Input REF Clock. (See available options table.)

The PLL is closed externally to provide more flexibility by allowing the user to control the delay between the input clock and the outputs.

The IDT23S08T is characterized for Commercial operation.

FUNCTIONAL BLOCK DIAGRAM



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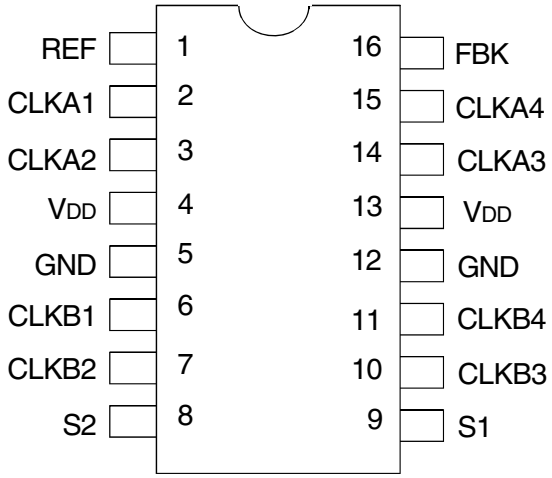
PIN CONFIGURATION



SOIC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Max.	Unit
V_{DD}	Supply Voltage Range	–0.5 to +4.6	V
V_I (2)	Input Voltage Range (REF)	–0.5 to +5.5	V
V_I	Input Voltage Range (except REF)	–0.5 to V_{DD}+0.5	V
I_{IK} (V_I < 0)	Input Clamp Current	–50	mA
I_O (V_O = 0 to V_{DD})	Continuous Output Current	±50	mA
V_{DD} or GND	Continuous Current	±100	mA
T_A = 55°C (in still air)(3)	Maximum Power Dissipation	0.7	W
T_{STG}	Storage Temperature Range	–65 to +150	°C
Operating Temperature	Commercial Temperature Range	0 to +70	°C

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

PIN DESCRIPTION

	Pin Number	Functional Description
REF (1)	1	Input Reference Clock, 3.3V Tolerant Input
CLKA1(2)	2	Clock Output for Bank A
CLKA2(2)	3	Clock Output for Bank A
V_{DD}	4	2.5V Supply
GND	5	Ground
CLKB1(2)	6	Clock Output for Bank B
CLKB2(2)	7	Clock Output for Bank B
S2(3)	8	Select Input, Bit 2
S1(3)	9	Select Input, Bit 1
CLKB3(2)	10	Clock Output for Bank B
CLKB4(2)	11	Clock Output for Bank B
GND	12	Ground
V_{DD}	13	2.5V Supply
CLKA3(2)	14	Clock Output for Bank A
CLKA4(2)	15	Clock Output for Bank A
FBK	16	PLL Feedback Input

NOTES:
1. Weak pull down.
2. Weak pull down on all outputs.
3. Weak pull ups on these inputs.

APPLICATIONS:

- **SDRAM**
- **Telecom**
- **Datacom**
- **PC Motherboards/Workstations**
- **Critical Path Delay Designs**

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FUNCTION TABLE[1] SELECT INPUT DECODING

S2	S1	CLK A	CLK B	Output Source	PLL Shut Down
L	L	Tri-State	Tri-State	PLL	Y
L	H	Driven	Tri-State	PLL	N
H	L	Driven	Driven	REF	Y
H	H	Driven	Driven	PLL	N

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level

AVAILABLE OPTIONS FOR IDT23S08T

Device	Feedback From	Bank A Frequency	Bank B Frequency
IDT23S08T-1	Bank A or Bank B	Reference	Reference
IDT23S08T-2[1]	Bank A	Reference	Reference/2
IDT23S08T-2[1]	Bank B	2 x Reference	Reference
IDT23S08T-3[1]	Bank A	2 x Reference	Reference or $\overline{\text{Reference}}$[2]
IDT23S08T-3[1]	Bank B	4 x Reference	2 x Reference
IDT23S08T-4[1]	Bank A or Bank B	2 x Reference	2 x Reference
IDT23S08T-5[1]	Bank A or Bank B	Reference/2	Reference/2

NOTES:
1. Contact factory for availability.
2. Output phase is indeterminant (0° or 180° from input clock).

SPREAD SPECTRUM COMPATIBLE

Many systems being designed now use a technology called Spread Spectrum Frequency Timing Generation. This product is designed not to filter off the Spread Spectrum feature of the reference input, assuming it exists. When a zero delay buffer is not designed to pass the Spread Spectrum feature through, the result is a significant amount of tracking skew, which may cause problems in systems requiring synchronization.

ZERO DELAY AND SKEW CONTROL

To close the feedback loop of the IDT23S08T, the FBK pin can be driven from any of the eight available output pins. The output driving the FBK pin will be driving a total load of 7pF plus any additional load that it drives. The relative loading of this output (with respect to the remaining outputs) can adjust the input-output delay.

For applications requiring zero input-output delay, all outputs including the one providing feedback should be equally loaded. Ensure the outputs are loaded equally, for zero output-output skew.

OPERATING CONDITIONS

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{DD}	Supply Voltage		2.3	2.7	V
T_A	Operating Temperature (Ambient Temperature)		0	70	°C
C_L	Load Capacitance from 10MHz to 133MHz		—	15	pF
C_{IN}	Input Capacitance[1]		—	7	pF

NOTE:
1. Applies to both REF and FBK.

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions		Min.	Typ.(1)	Max.	Unit
V_{IL}	Input LOW Voltage Level			—	—	0.7	V
V_{IH}	Input HIGH Voltage Level			1.7	—	—	V
I_{IL}	Input LOW Current	V_{IN} = 0V		—	—	50	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}		—	—	100	µA
V_{OL}	Output LOW Voltage	I_{OL} = 8mA		—	—	0.3	V
V_{OH}	Output HIGH Voltage	I_{OH} = -8mA		2	—	—	V
I_{DD_PD}	Power Down Current	REF = 0MHz (S2 = S1 = H)		—	—	12	µA
I_{DD}	Supply Current	Unloaded Outputs Select Inputs at V_{DD} or GND	100MHz CLKA	—	—	45	mA
			66MHz CLKA	—	—	32	
			33MHz CLKA	—	—	18	

SWITCHING CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_1	Output Frequency	15pF Load	10	—	133.3	MHz
	Duty Cycle = $t_2 \div t_1$	Measured at $V_{DD}/2$, F_{OUT} = 66.66MHz, 15pF Load	40	50	60	%
t_3	Rise Time	Measured between 0.7V and 1.7V, 15pF Load	—	—	2.5	ns
t_4	Fall Time	Measured between 0.7V and 1.7V, 15pF Load	—	—	2.5	ns
t_5	Output to Output Skew on same Bank (-1, -2, -3, -4, -5)	All outputs equally loaded	—	—	200	ps
	Output Bank A to Output Bank B (-1, -4, -5)	All outputs equally loaded	—	—	200	ps
	Output Bank A to Output Bank B Skew (-2, -3)	All outputs equally loaded	—	—	400	ps
t_6	Delay, REF Rising Edge to FBK Rising Edge	Measured at $V_{DD}/2$	—	0	±350	ps
t_7	Device to Device Skew	Measured at $V_{DD}/2$ on the FBK pins of devices	—	0	700	ps
t_J	Cycle to Cycle Jitter (-1, -4, -5)	Measured at 66.67 MHz, loaded outputs, 15pF Load	—	—	200	ps
		Measured at 133.3 MHz, loaded outputs, 15pF Load	—	—	200	
t_J	Cycle to Cycle Jitter (-2, -3)	Measured at 66.67 MHz, loaded outputs, 15pF Load	—	—	400	ps
t_{LOCK}	PLL Lock Time	Stable Power Supply, valid clocks presented on REF and FBK pins	—	—	1	ms

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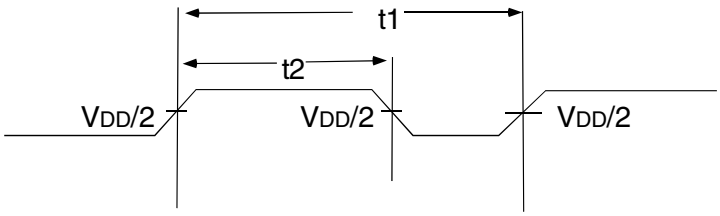
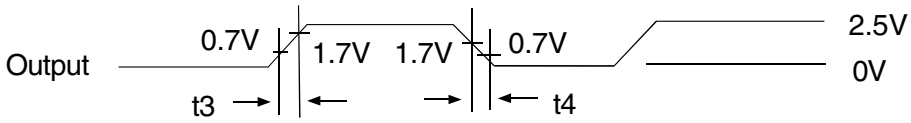
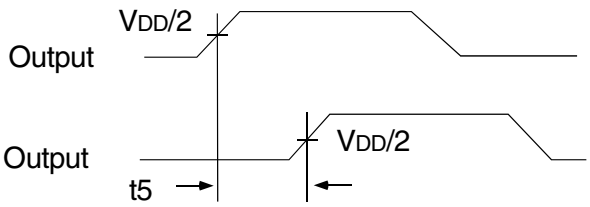
SWITCHING WAVEFORMS



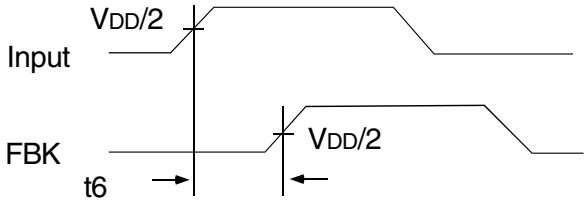
Duty Cycle Timing



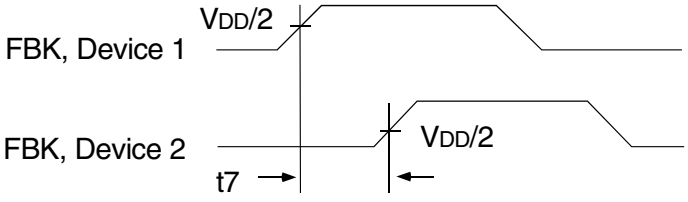
All Outputs Rise/Fall Time



Output to Output Skew

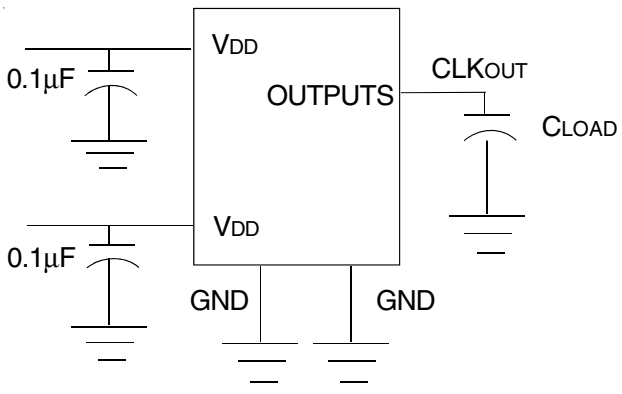


Input to Output Propagation Delay



Device to Device Skew

TEST CIRCUIT



Test Circuit for all Parameters

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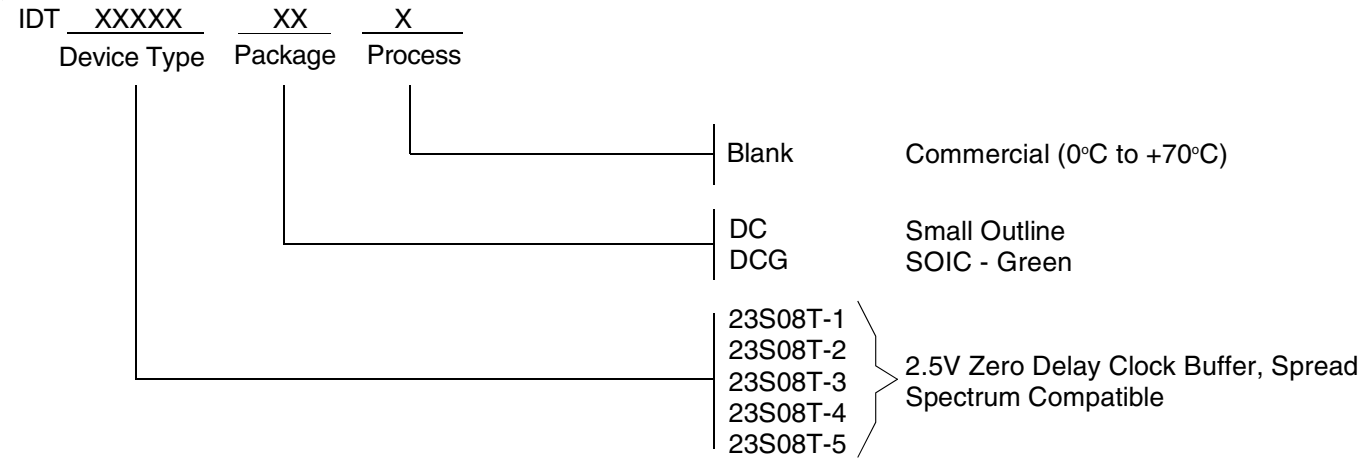
ORDERING INFORMATION



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