DTV, STB CLOCK SOURCE

ICS3771-18

Description

The ICS3771-18 provides clock generation and conversion for clock rates commonly needed in HDTV digital video equipment. The ICS3771-18 uses the latest PLL technology to provide excellent phase noise and long term jitter performance for superior synchronization and S/N ratio.

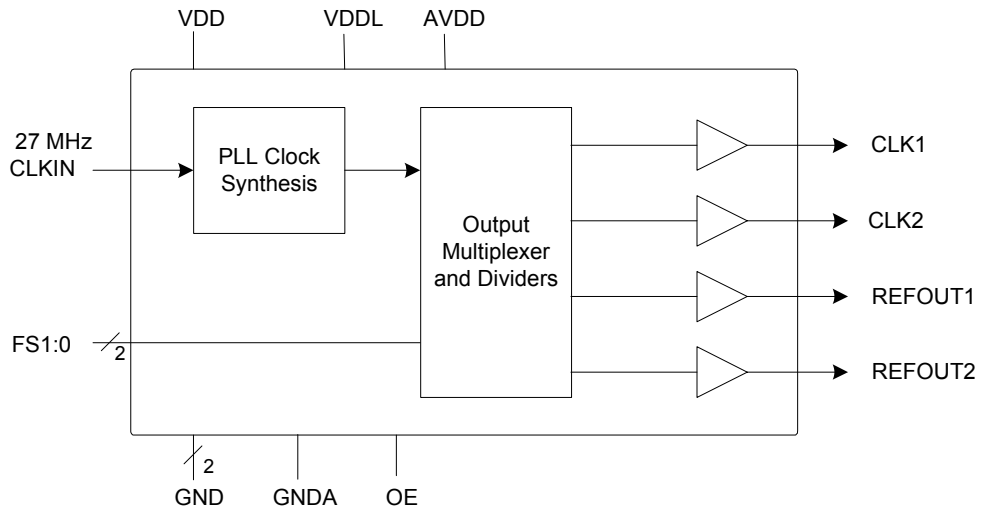
For audio sampling clocks generated from 27 MHz, use the ICS661.

Please contact IDT if you have a requirement for an input and output frequency not included in this document. IDT can rapidly modify this product to meet special requirements.

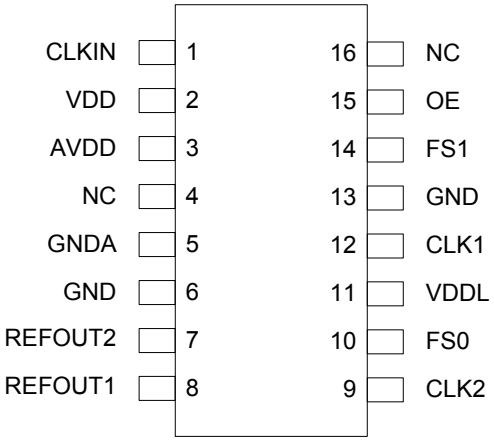
Features

- Integrated Phase-Lock Loop
- Low jitter, high accuracy outputs
- 3.3 V operation
- Packaged in 16-pin TSSOP
- RoHS 6 (green and lead free) compliant packaging
- Exact (0 ppm) multiplication ratios
- Pin compatible to CY24204-3

Block Diagram



Pin Assignment



16-pin TSSOP

Output Clock Selection Table (MHz)

OE	FS1	FS0	CLK1/CLK2	REFOUT1/REFOUT2
0	0	0	OFF*	27
0	0	1	OFF*	27
0	1	0	OFF*	27
0	1	1	OFF*	27
1	0	0	27	27
1	0	1	27.027	27
1	1	0	74.250	27
1	1	1	74.17582418	27

*OFF = output is driven HIGH.

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	CLKIN	Input	Reference clock input. Connect to a 27 MHz external clock.
2	VDD	Power	Power supply.
3	AVDD	Power	Power supply. Connect to 3.3 V.
4	NC	–	No connect. Leave floating.
5	GNDA	Power	Analog ground.
6	GND	Power	Connect to ground.
7	REFOUT	Output	Reference Clock output 2. See table above.
8	REFOUT	Output	Reference Clock output 1. See table above.
9	CLK2	Output	Selectable Clock output 2. See table above.
10	FS0	Input	Frequency select pin 0. Weak internal pull-up. See table above.
11	VDDL	Power	Power supply. Connect to 3.3 V.
12	CLK1	Output	Selectable Clock output 1. See table above
13	GND	Power	Connect to ground.
14	FS1	Input	Frequency select pin 1. Weak internal pull-up. See table above.
15	OE	Output	Output Enable pin. Weak internal pull-up. See table above.
16	NC	–	No connect. Leave floating.

Application Information

Series Termination Resistor

Clock output traces should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

Decoupling Capacitors

As with any high-performance mixed-signal IC, the ICS3771-18 must be isolated from system power supply noise to perform optimally.

Decoupling capacitors of 0.01µF must be connected between each VDD and the PCB ground plane. To further guard against interfering system supply noise, the ICS3771-18 should use one common connection to the PCB power plane as shown in the diagram on the next page. The ferrite bead and bulk capacitor help reduce lower frequency noise in the supply that can lead to output clock phase modulation.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) Each 0.01µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.

2) The external crystal should be mounted next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces, instead they should be separated and away from other traces.

3) To minimize EMI and obtain the best signal integrity, the 33Ω series termination resistor should be placed close to the clock output.

4) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (the ferrite bead and bulk decoupling capacitor can be mounted on the back). Other signal traces should be routed away from the ICS3771-18. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS3771-18. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	5.5 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70° C
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	° C
Power Supply Voltage (measured in respect to GND)	+3.135	3.3	+3.465	V

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply Current	I_{VDD}	AVDD / VDD current			25	mA
	I_{VDDL}	VDDL current (VDDL = 3.47 V)			20	mA
Output High Current	I_{OH}	V_{OH} = VDD-0.5, VDD/VDD = 3.3 V	12	24		mA
Output Low Current	I_{OL}	V_{OL} = 0.5, VDD/VDD = 3.3 V	12	24		mA
Input High Voltage	V_{IH}	CMOS levels, 70% of VDD	0.7			VDD
Input Low Voltage	V_{IL}	CMOS levels, 30% of VDD			0.3	VDD
Max. Load Capacitance	C_{LOAD}				15	pF
Input Capacitance	C_{IN}				7	pF
Internal Pull-up Resistor	R_{UP}			100	150	kΩ

AC Electrical Characteristics

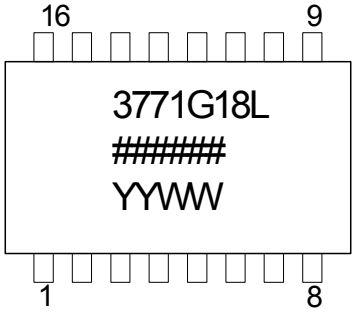
Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Crystal Frequency					27	MHz
Edge Rate Rise Time	t_{OR}	20% to 80%, 15 pF load	0.8	1.4		V/ns
Edge Rate Fall Time	t_{OF}	80% to 20%, 15 pF load	0.8	1.4		V/ns
Output Duty Cycle	t_{OD}		45	50	55	%
Clock Jitter		CLK1, CLK2		120		ps p-p
PLL Lock Time					3	ms

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		78		°C/W
	θ_{JA}	1 m/s air flow		70		°C/W
	θ_{JA}	3 m/s air flow		68		°C/W
Thermal Resistance Junction to Case	θ_{JC}			37		°C/W

Marking Diagram

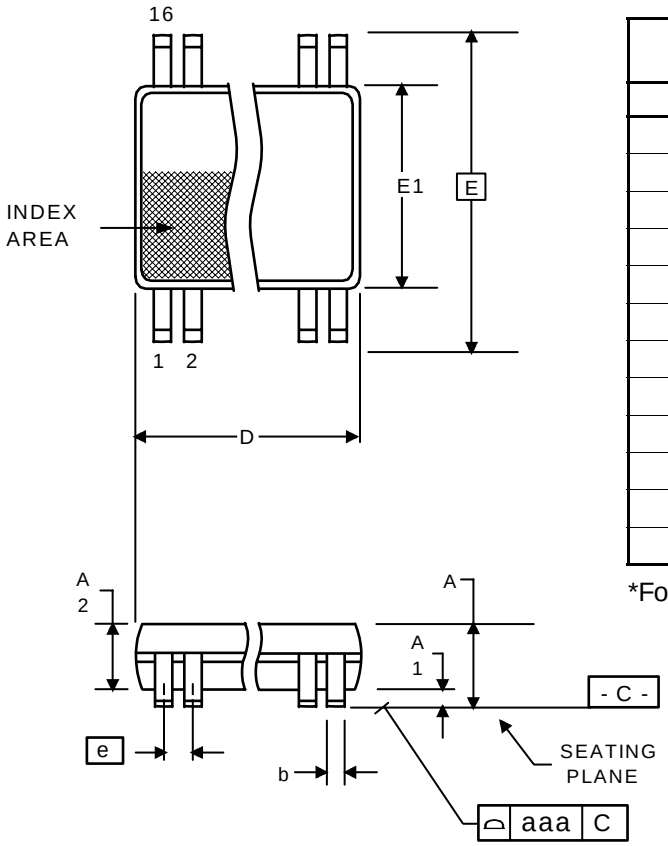


Notes:

1. ###### is the lot number.
2. YYWW is the last two digits of the year and week that the part was assembled.
3. “LF” denotes Pb (lead) free, RoHS compliant package.
4. Bottom marking: country of origin if not USA.

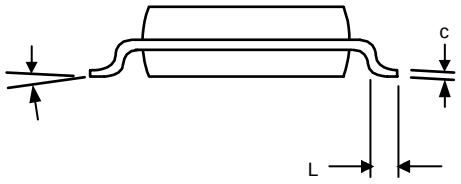
Package Outline and Package Dimensions (16-pin TSSOP, 4.40 mm Body, 0.65 mm Pitch)

Package dimensions are kept current with JEDEC Publication No. 95, MO-153



	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	--	1.20	--	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	4.90	5.1	0.193	0.201
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	0.169	0.177
e	0.65 Basic		0.0256 Basic	
L	0.45	0.75	0.018	0.030
α	0°	8°	0°	8°
aaa	--	0.10	--	0.004

*For reference only. Controlling dimensions in mm.



Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
3771G-18	3771G-18	Tubes	16-pin TSSOP	0 to +70° C
3771G-18T	3771G-18	Tape and Reel	16-pin TSSOP	0 to +70° C
3771G-18LF	3771G18L	Tubes	16-pin TSSOP	0 to +70° C
3771G-18LFT	3771G18L	Tape and Reel	16-pin TSSOP	0 to +70° C

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History

Rev.	Originator	Date	Description of Change
A	R. Willner	04/19/06	Production part number assigned.
B	R. Willner	11/13/07	Clock input support only.

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