## Description

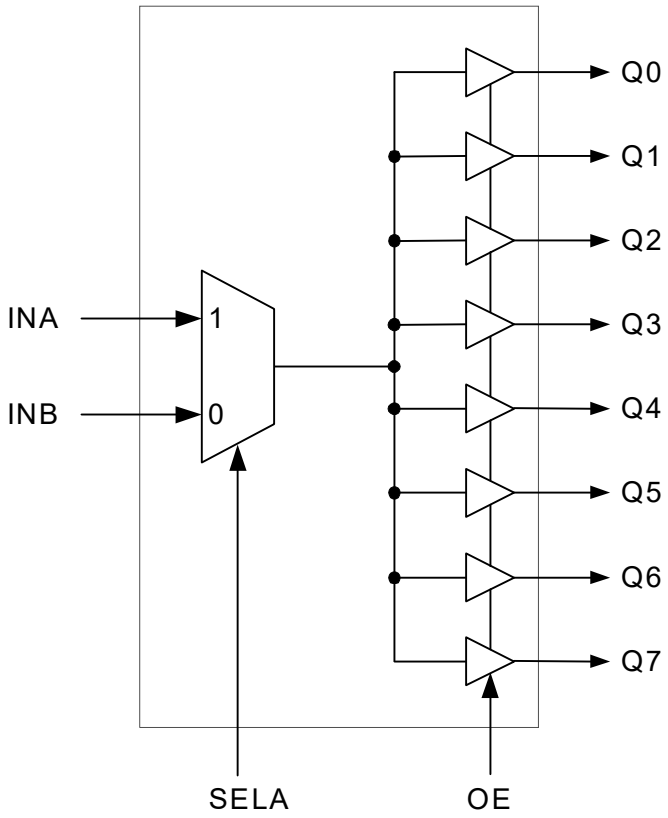
The 552-02S is a low skew, single-input to eight- output clock buffer. The device offers a dual input with pin select for switching between two clock sources. It has best in class Additive Phase Jitter of sub 50fsec

Renesas makes many non-PLL and PLL based low skew output devices as well as Zero Delay Buffers to synchronize clocks. Contact us for all of your clocking needs.

## Features

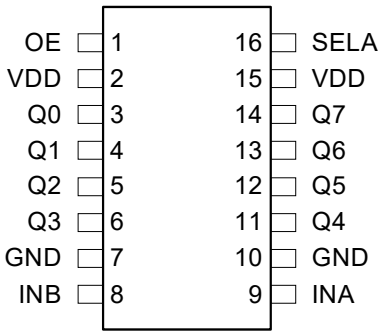
- Low RMS Additive Phase Jitter: 50fs
- Low output skew: 50ps
- Operating Voltages of 1.8V to 3.3V
- Packaged in 16-pin TSSOP and 16-pin VFQFPN, Pb-free
- Input clock multiplexer simplifies clock selection
- Output Enable pin tri-states outputs
- Input/Output clock frequency up to 200MHz
- Low power CMOS technology
- 3.3V tolerant inputs
- Extended temperature (-40°C to +105°C)

## Block Diagram

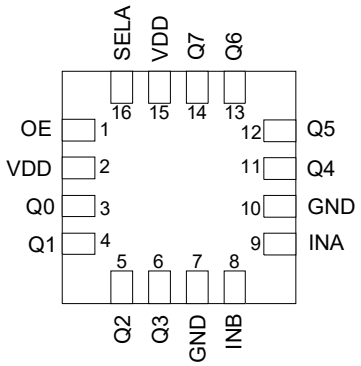


## Pin Assignments




16 Pin TSSOP




16-pin VFQFN

## Input Source Select

| SELA | Input |
|---|---|
| 0 | INB |
| 1 | INA |

## Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description |
|---|---|---|---|
| 1 | OE | Input | Output Enable. Tri-states outputs when low. Internal pull-up resistor. |
| 2 | VDD | Power | Connect to +1.8V, +2.5V or +3.3V. Must be the same as pin 15. |
| 3 | Q0 | Output | Clock Output 0. |
| 4 | Q1 | Output | Clock Output 1. |
| 5 | Q2 | Output | Clock Output 2. |
| 6 | Q3 | Output | Clock Output 3. |
| 7 | GND | Power | Connect to ground. |
| 8 | INB | Input | Clock Input B. 3.3V tolerant. |
| 9 | INA | Input | Clock Input A. 3.3V tolerant. |
| 10 | GND | Power | Connect to ground. |
| 11 | Q4 | Output | Clock Output 4. |
| 12 | Q5 | Output | Clock Output 5. |
| 13 | Q6 | Output | Clock Output 6. |
| 14 | Q7 | Output | Clock Output 7. |
| 15 | VDD | Power | Connect to +1.8V, +2.5V or +3.3V. Must be the same as pin 2. |
| 16 | SELA | Input | Selects either INA or INB. Internal pull-up resistor. |

## External Components

A minimum number of external components are required for proper operation. Decoupling capacitors of 0.01µF should be connected between VDD on pin 2 and GND on pin 7, and between VDD on pin 15 and GND on pin 10, as close to the device as possible. A 33Ω series terminating resistor should be used on each clock output if the trace is longer than 1 inch.

To achieve the low output skews that the 552-02S is capable of, careful attention must be paid to board layout. Essentially, all 8 outputs must have identical terminations, identical loads, and identical trace geometries. If they do not, the output skew will be degraded. For example, using a 30Ω series termination on one output (with 33Ω on the others) will cause at least 15ps of skew.

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 552-02S. These ratings, which are standard values for Renesas commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|---|---|
| Supply Voltage, VDD | 3.465V |
| All Inputs and Outputs | -0.5V to 3.465V |
| Ambient Operating Temperature, Extended | -40 to +105°C |
| Storage Temperature | -65 to +150°C |
| Junction Temperature | 175°C |
| Soldering Temperature | 260°C |

## Recommended Operation Conditions

| Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|
| Ambient Operating Temperature, Extended | -40 | - | +105 | °C |
| Power Supply Voltage (measured in respect to GND) | +1.71 | - | +3.465 | V |

## DC Electrical Characteristics

**VDD = 1.8V ±5%**, Ambient temperature -40°C to +105°C, unless stated otherwise

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| Operating Voltage | VDD | | 1.71 | - | 1.89 | V |
| Input High Voltage, INA, INB | $V_{IH}$ | Note 1 | 0.7xVDD | - | 1.89 | V |
| Input Low Voltage, INA, INB | $V_{IL}$ | Note 1 | - | - | 0.3xVDD | V |
| Input High Voltage, OE, SELA | $V_{IH}$ | | 0.7xVDD | - | VDD | V |
| Input Low Voltage, OE, SELA | $V_{IL}$ | | - | - | 0.3xVDD | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -10mA | 1.3 | - | - | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 10mA | - | - | 0.35 | V |
| Operating Supply Current | IDD | No load, 135MHz | - | 32 | - | mA |

**VDD = 2.5V ±5%**, Ambient temperature -40°C to +105°C, unless stated otherwise

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| Operating Voltage | VDD | | 2.375 | - | 2.625 | V |
| Input High Voltage, INA, INB | $V_{IH}$ | Note 1 | 0.7xVDD | - | 2.625 | V |
| Input Low Voltage, INA, INB | $V_{IL}$ | Note 1 | - | - | 0.3xVDD | V |
| Input High Voltage, OE, SELA | $V_{IH}$ | | 0.7xVDD | - | VDD | V |
| Input Low Voltage, OE, SELA | $V_{IL}$ | | - | - | 0.3xVDD | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -16mA | 1.8 | - | - | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 16mA | - | - | 0.5 | V |
| Operating Supply Current | IDD | No load, 135MHz | - | 43 | - | mA |

**VDD = 3.3V ±5%**, Ambient temperature -40°C to +105°C, unless stated otherwise

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| Operating Voltage | VDD | | 3.135 | - | 3.465 | V |
| Input High Voltage, INA, INB | $V_{IH}$ | Note 1 | 0.7xVDD | - | 3.465 | V |
| Input Low Voltage, INA, INB | $V_{IL}$ | Note 1 | - | - | 0.3xVDD | V |
| Input High Voltage, OE, SELA | $V_{IH}$ | | 0.7xVDD | - | VDD | V |
| Input Low Voltage, OE, SELA | $V_{IL}$ | | - | - | 0.3xVDD | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -25mA | 2.2 | - | - | V |
| Output Low Voltage | $V_{OL}$ | $I_{OH}$ = 25mA | - | - | 0.7 | V |
| Operating Supply Current | IDD | No load, 135MHz | - | 55 | - | mA |

# AC Electrical Characteristics

**VDD = 1.8V ±5%**, Ambient Temperature -40°C to +105°C, unless stated otherwise

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| Input Frequency | | | 0 | - | 200 | MHz |
| Output Rise Time | $t_{OR}$ | 0.36 to 1.44 V, $C_L$ = 5pF | - | 1 | 1.5 | ns |
| Output Fall Time | $t_{OF}$ | 1.44 to 0.36 V, $C_L$ = 5pF | - | 1 | 1.5 | ns |
| Start-up Time | $t_{START-UP}$ | Part start-up time for valid outputs after VDD ramp-up | - | - | 2 | ms |
| Propagation Delay | Note 1 | 135MHz | 2 | 2.5 | 3 | ns |
| Buffer Additive Phase Jitter, RMS | | 125MHz, Integration Range: 12kHz–20MHz | - | 50 | 65 | ps |
| Output to output skew | Note 2 | Rising edges at VDD/2 | - | 0 | 65 | ps |
| Input A to Input B skew | Note 3 | | - | 0 | 50 | ps |

**VDD = 2.5V ±5%**, Ambient Temperature -40°C to +105°C, unless stated otherwise

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| Input Frequency | | | 0 | - | 200 | MHz |
| Output Rise Time | $t_{OR}$ | 0.5 to 2.0 V, $C_L$ = 5pF | - | 0.6 | 1.0 | ns |
| Output Fall Time | $t_{OF}$ | 2.0 to 0.5 V, $C_L$ = 5pF | - | 0.6 | 1.0 | ns |
| Start-up Time | $t_{START-UP}$ | Part start-up time for valid outputs after VDD ramp-up | - | - | 2 | ms |
| Propagation Delay | Note 1 | 135MHz | 2 | 2.7 | 3.5 | ns |
| Buffer Additive Phase Jitter, RMS | | 125MHz, Integration Range: 12kHz–20MHz | - | 50 | 65 | ps |
| Output to output skew | Note 2 | Rising edges at VDD/2 | - | 0 | 65 | ps |
| Input A to Input B skew | Note 3 | | - | 0 | 50 | ps |

**VDD = 3.3V ±5%**, Ambient Temperature -40°C to +105°C, unless stated otherwise

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| Input Frequency | | | 0 | | 200 | MHz |
| Output Rise Time | $t_{OR}$ | 0.66 to 2.64 V, $C_L$ = 5pF | - | 0.6 | 1.0 | ns |
| Output Fall Time | $t_{OF}$ | 2.64 to 0.66 V, $C_L$ = 5pF | - | 0.6 | 1.0 | ns |
| Start-up Time | $t_{START-UP}$ | Part start-up time for valid outputs after VDD ramp-up | - | - | 2 | ms |
| Propagation Delay | Note 1 | 135MHz | 2 | 2.5 | 3 | ns |
| Buffer Additive Phase Jitter, RMS | | 125MHz, Integration Range: 12kHz–20MHz | - | 50 | 65 | ps |
| Output to output skew | Note 2 | Rising edges at VDD/2 | - | 0 | 65 | ps |
| Input A to Input B skew | Note 3 | | - | 0 | 50 | ps |

Notes:
1. With rail-to-rail input clock.
2. Between any two outputs with equal loading.
3. Propagation delay matching through the part.
4. Duty cycle on outputs will match incoming clock duty cycle. Consult Renesas for tight duty cycle clock generators.

## Package Outline Drawings

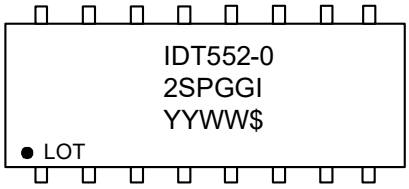
The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document

## Ordering Information

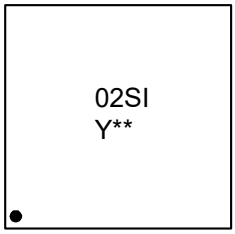
| Part Number | Carrier Type | Package | Temperature Range |
|---|---|---|---|
| 552-02SPGGI | Tubes | 4.4mm body 16-TSSOP | -40°C to +105°C |
| 552-02SPGGI8 | Tape & Reel | 4.4mm body 16-TSSOP | -40°C to +105°C |
| 552-02SCMGI | Cut Tape | 2.5 × 2.5 mm 16-VFQFPN | -40°C to +105°C |
| 552-02SCMGI8 | Tape & Reel | 2.5 × 2.5 mm 16-VFQFPN | -40°C to +105°C |

**“G” after the two-letter package code denotes Pb-Free configuration, RoHS compliant.**

## Marking Diagrams




16-pin TSSOP




16-pin QFN

Notes:

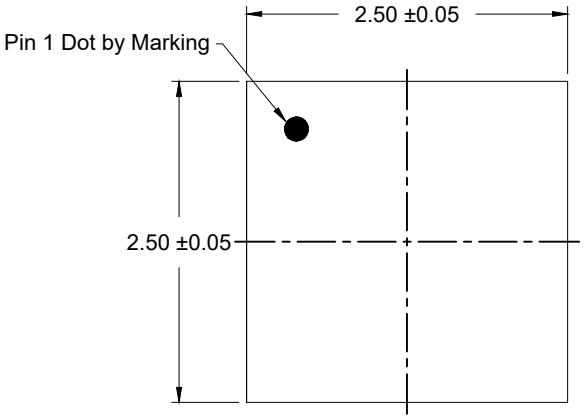
1. “**” is the lot sequence.
2. “YYWW” or “Y” is the last digit(s) of the year and week that the part was assembled.
3. “$” denotes the mark code.
4. “LOT” denotes lot number.
5. “G” after the two-letter package code denotes RoHS compliant package.
6. “I” denotes extended temperature range device.
7. Bottom marking: country of origin (TSSOP only).

## Revision History

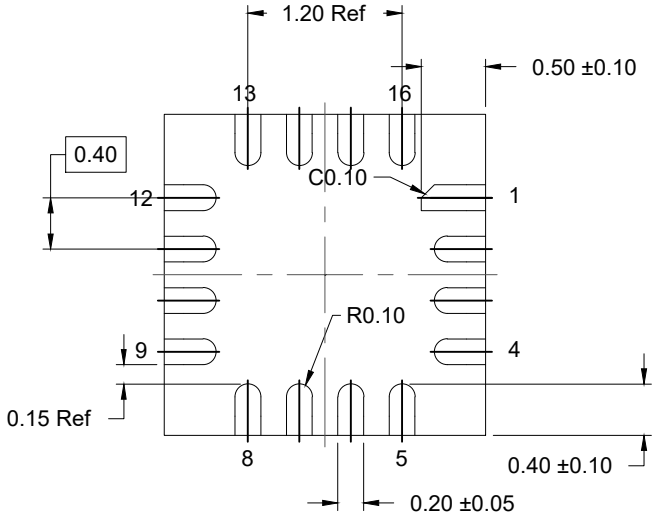
| Date | Description of Change |
|---|---|
| Apr 9, 2024 | • Changed Carrier Type in Ordering Information for CMG packages to Cut Tape from Tubes.<br>• Removed package outline drawings from document and replaced them with dynamic links in Ordering Information.<br>• Updated Package Outline Drawings section. |
| Apr 18, 2017 | • Replaced package outline drawings with latest CMG16 and PGG16 versions.<br>• Updated legal disclaimer. |
| Jul 11, 2016 | Release to final. |

# Package Outline Drawing

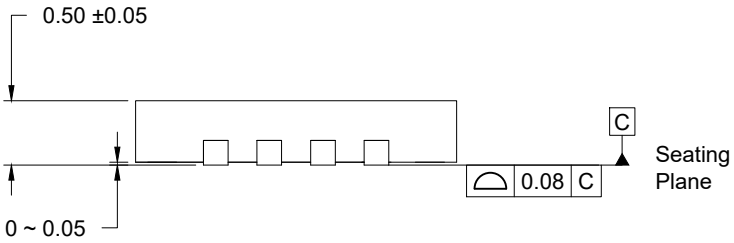
Package Code:CMG16D1
16-VFQFPN 2.5 x 2.5 x 0.5 mm Body, 0.4mm Pitch
PSC-4478-01, Revision: 00, Date Created: Jun 16, 2022



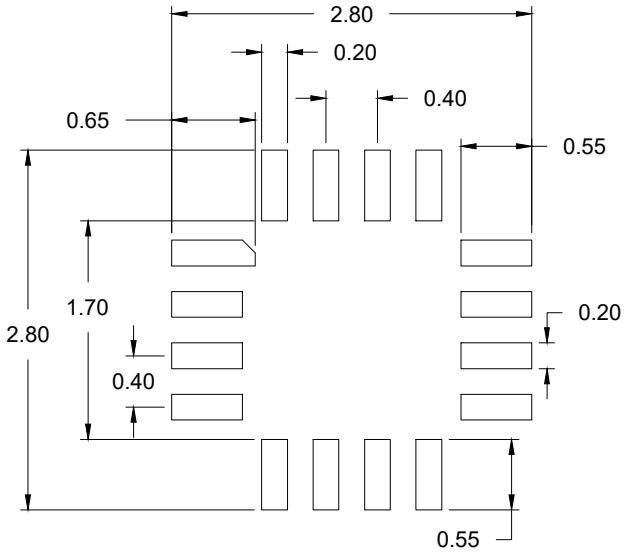

TOP VIEW




BOTTOM VIEW



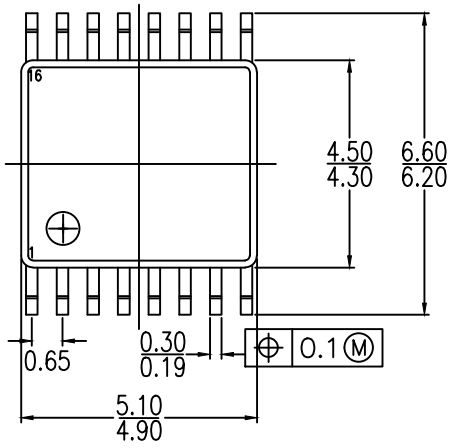

SIDE VIEW

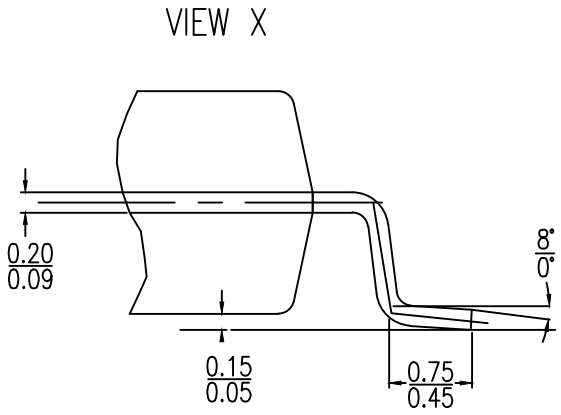


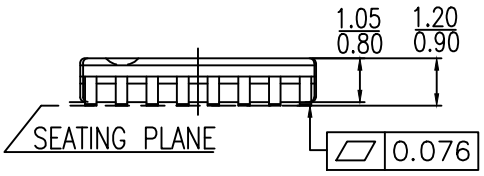

RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

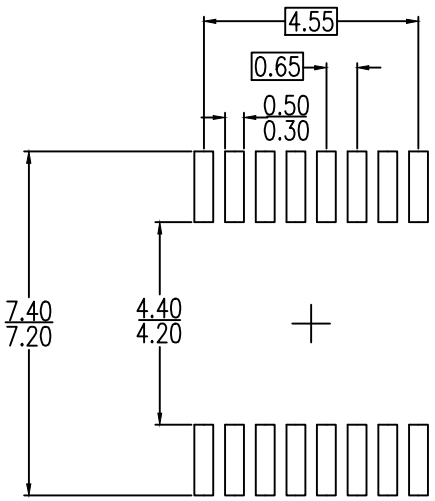
1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.




NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS




LAND PATTERN DIMENSIONS

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS

| Package Revision History | | |
|---|---|---|
| Date Created | Rev No. | Description |
| | | |
| Jan 26, 2018 | Rev 00 | Revised from PSC-4056-02 PGG16 |

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