# LOW EMI CLOCK GENERATOR

IDT5V50013

## Description

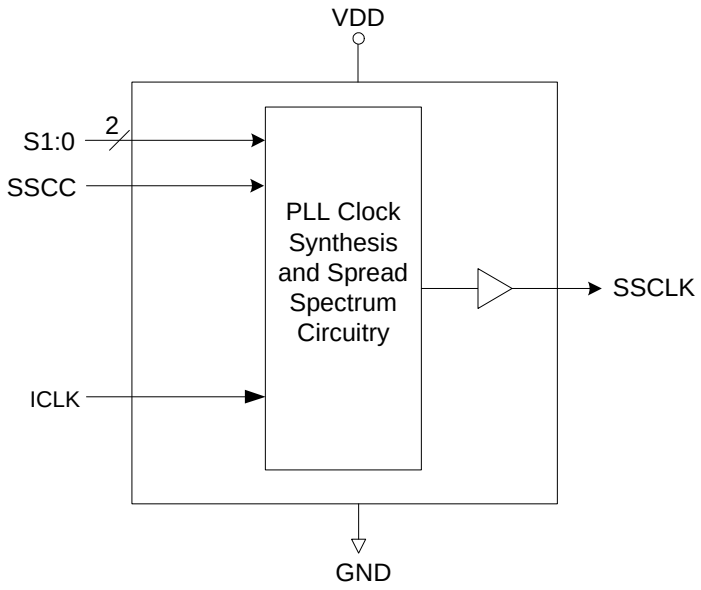
The IDT5V50013 generates a low EMI output clock from a clock input. The part is designed to dither the LCD interface clock for PDAs, printers, scanners, modems, copiers, and others. Using IDT's proprietary mix of analog and digital Phase-Locked Loop (PLL) technology, the device spreads the frequency spectrum of the output, reducing the frequency amplitude peaks by several dB.

IDT offers many other clocks for computers and computer peripherals. Consult IDT when you need to remove crystals and oscillators from your board.

## Features

- Packaged in 8-pin SOIC
- Provides a spread spectrum output clock
- 50 MHz to 140 MHz operation
- Accepts a clock input (provides same frequency dithered output)
- Center spread modulation
- Peak reduction by 8 dB to 16 dB typical on 3rd through 19th odd harmonics
- Low EMI feature can be disabled
- Operating voltage of 3.3 V
- Advanced, low-power CMOS process

## Block Diagram





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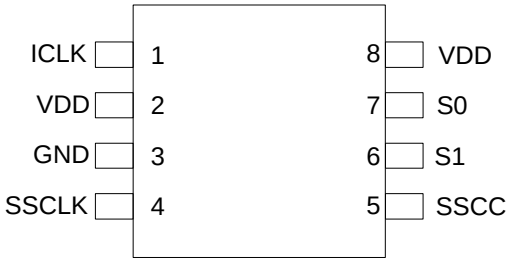
## Pin Assignment




8 pin (150 mil) SOIC

## Spread Direction and Percentage Select Table

| S1 Pin 6 | S0 Pin 7 | Spread Direction | Spread Percentage |
|---|---|---|---|
| 0 | 0 | Center | ±0.5 |
| 0 | 1 | Center | ±1.0 |
| 1 | 0 | Center | ±1.5 |
| 1 | 1 | Center | ±2.0 |

0 = connect to GND
1 = connect directly to VDD

## Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description |
|---|---|---|---|
| 1 | ICLK | Input | Connect to a 50-140 MHz clock input. |
| 2 | VDD | Power | Connect to +3.3 V. |
| 3 | GND | Power | Connect to ground. |
| 4 | SSCLK | Output | Clock output with spread spectrum. |
| 5 | SSCC | Input | Spread spectrum enable/disable function. SSCC function is enabled when input is high and disabled when input is low. This pin is pulled high internally. |
| 6 | S1 | Input | Function select 1 input. Selects spread amount and direction per table above. Internal pull-down. |
| 7 | S0 | Input | Function select 0 input. Selects spread amount and direction per table above. Internal pull-down. |
| 8 | VDD | Power | Connect to +3.3 V. |



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## External Components

The IDT5V50013 requires a minimum number of external components for proper operation.

### Decoupling Capacitor

A decoupling capacitor of 0.01µF must be connected between VDD and GND on pins 2 and 3, as close to these pins as possible. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

### Series Termination Resistor

When the PCB trace between the clock output and the load is over 1 inch, series termination should be used. To series terminate a 50Ω trace (a commonly used trace impedance) place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

## PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

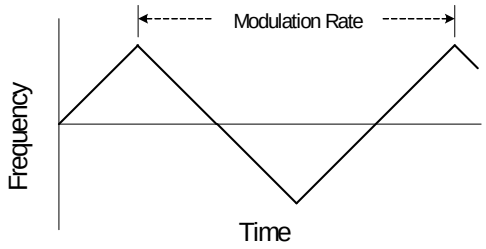
1) The 0.01µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via.

2) To minimize EMI, the 33Ω series termination resistor (if needed) should be placed close to the clock output.

3) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the IDT5V50013. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

## Spread Spectrum Profile

The IDT5V50013 low EMI clock generator uses an optimized frequency slew rate algorithm to facilitate down stream tracking of zero delay buffers and other PLL devices. The frequency modulation amplitude is constant with variations of the input frequency.



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## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the IDT5V50013. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|---|---|
| Supply Voltage, VDD | 7 V |
| All Inputs and Outputs | -0.5 V to VDD+0.5 V |
| Ambient Operating Temperature | 0 to +70° C |
| Storage Temperature | -65 to +150° C |
| Junction Temperature | 125° C |
| Soldering Temperature | 260° C |

## Recommended Operation Conditions

| Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|
| Ambient Operating Temperature | 0 | | +70 | ° C |
| Power Supply Voltage (measured in respect to GND) | +3.0 | | 3.63 | V |



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## DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V**, Ambient Temperature 0 to +70° C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Operating Voltage | VDD | | 2.97 | 3.3 | 3.63 | V |
| Supply Current | IDD | ICLK=65 MHz, Note 1 | | 17 | 20 | mA |
| Input High Voltage | $V_{IH}$ | S1: S0 | 2.0 | | | V |
| Input Low Voltage | $V_{IL}$ | S1: S0 | | | 0.8 | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -6 mA | 2.4 | | | V |
| | | $I_{OH}$ =- 20 mA | 2.0 | | | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 6 mA | | | 0.4 | V |
| | | $I_{OL}$ = 20 mA | | | 1.2 | V |
| Input Capacitance | $C_{IN1}$ | All inputs | 3 | 4 | 5 | pF |
| Pull-down Resistance | $R_{PD}$ | S1, S0 | | 240 | | kΩ |
| Pull-up Resistance | $R_{PU}$ | SSCC | | 240 | | kΩ |

**Note 1**: CL = 15 pF.

## AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V**, Ambient Temperature 0 to +70° C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Input Clock Frequency | | | 50 | | 140 | MHz |
| Output Clock Frequency | | | 50 | | 140 | MHz |
| Output Clock Duty Cycle | | All outputs | 45 | 50 | 55 | % |
| Cycle to cycle Jitter | | ICLK=50 MHz, SS on | | 100 | 150 | ps |
| | | ICLK=140 MHz, SS on | | 100 | 150 | ps |
| Output Rise Time | $t_R$ | 20% to 80%, CL=15 pF, 100 MHz | | 0.9 | | ns |
| Output Fall Time | $t_F$ | 80% to 20%, CL=15 pF, 100 MHz | | 0.9 | | ns |
| Modulation Frequency | | ICLK=70 MHz | | 30 | | kHz |



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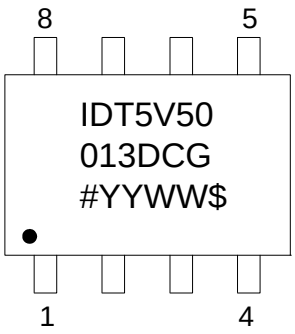
## Thermal Characteristics for 8SOIC

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Thermal Resistance Junction to Ambient | $\theta_{JA}$ | Still air | | 150 | | °C/W |
| | $\theta_{JA}$ | 1 m/s air flow | | 140 | | °C/W |
| | $\theta_{JA}$ | 3 m/s air flow | | 120 | | °C/W |
| Thermal Resistance Junction to Case | $\theta_{JC}$ | | | 40 | | °C/W |
| Thermal Resistance Junction to Top of Case | $\Psi_{JT}$ | Still air | | 20 | | °C/W |

## Marking Diagram (8SOIC)




Notes:

1. YYWW or YWW is the digits of the year and week that the part was assembled.
2. “$” is the assembly mark code.
3. “G” designates RoHS compliant package.
4. “#” is the lot code.
5. Bottom marking: country of origin if not USA.



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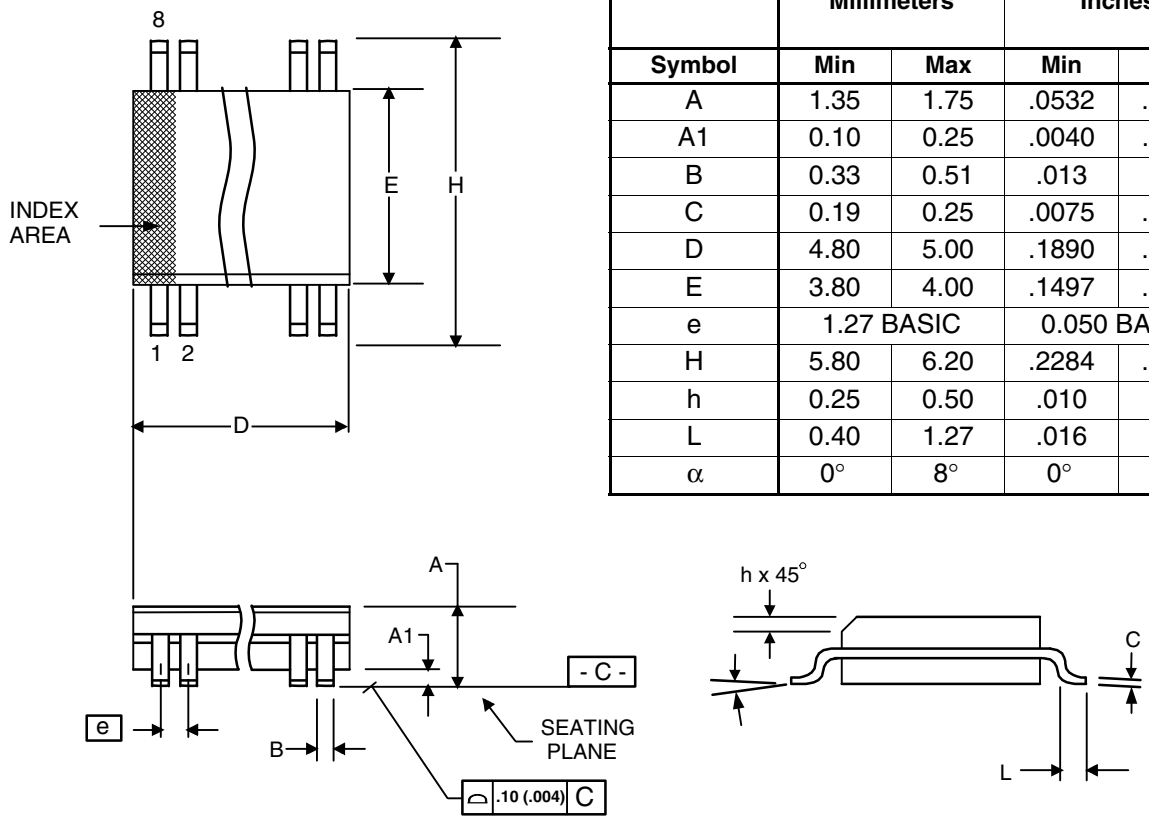
## Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95




| | Millimeters | | Inches | |
|---|---|---|---|---|
| **Symbol** | **Min** | **Max** | **Min** | **Max** |
| A | 1.35 | 1.75 | .0532 | .0688 |
| A1 | 0.10 | 0.25 | .0040 | .0098 |
| B | 0.33 | 0.51 | .013 | .020 |
| C | 0.19 | 0.25 | .0075 | .0098 |
| D | 4.80 | 5.00 | .1890 | .1968 |
| E | 3.80 | 4.00 | .1497 | .1574 |
| e | 1.27 BASIC | | 0.050 BASIC | |
| H | 5.80 | 6.20 | .2284 | .2440 |
| h | 0.25 | 0.50 | .010 | .020 |
| L | 0.40 | 1.27 | .016 | .050 |
| α | 0° | 8° | 0° | 8° |

## Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---|---|---|---|---|
| 5V50013DCG | see page 6 | Tubes | 8-pin SOIC | 0 to +70° C |
| 5V50013DCG8 | | Tape and Reel | 8-pin SOIC | 0 to +70° C |

**"G" after the two-letter package code denotes Pb-Free configuration, RoHS compliant.**

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### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com


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