NETWORKING AND PCI CLOCK SOURCE
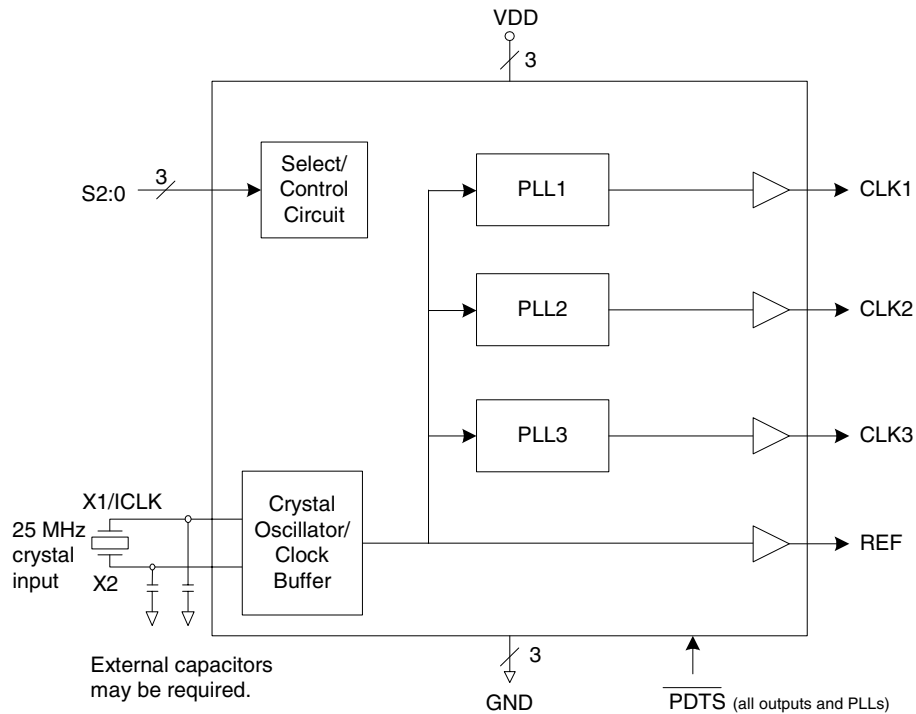
ICS650-36

Description

The ICS650-36 is a low cost frequency generator designed to support networking and PCI applications. Using analog/digital Phase Locked-Loop (PLL) techniques, the device uses a standard fundamental mode, inexpensive crystal input of 25 MHz to produce four output clocks supporting LAN, PCI, and 100M SDRAM functions.

The device also has a power down feature that tri-states the clock outputs and turns off the PLL when the $\overline{PDTS}$ pin is taken low.
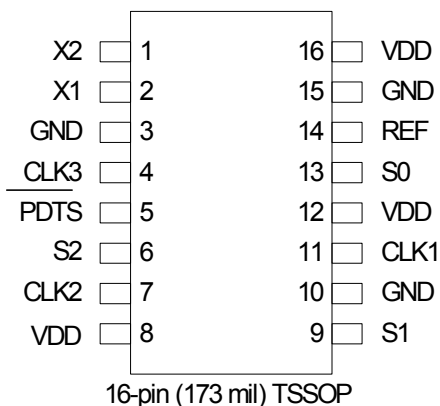
Features

- Packaged in 16-pin TSSOP
- Pb (lead) free package
- Replaces multiple crystals and oscillators
- Input crystal or clock frequency of 25 MHz
- Fixed reference output frequency of 25 MHz
- Selectable output frequencies of 33.3, 33.333, 50, 66.666, 100, and 125 MHz
- Duty cycle of 40/60
- Operating voltage of 3.3 V
- Advanced, low-power CMOS process
- Industrial and commercial temperature ranges

Block Diagram

External capacitors may be required.

$\overline{PDTS}$ (all outputs and PLLs)

Pin Assignment

```
         ┌──────────┐
   X2 ☐ 1│          │16 ☐ VDD
   X1 ☐ 2│          │15 ☐ GND
  GND ☐ 3│          │14 ☐ REF
 CLK3 ☐ 4│          │13 ☐ S0
 PDTS ☐ 5│          │12 ☐ VDD
   S2 ☐ 6│          │11 ☐ CLK1
 CLK2 ☐ 7│          │10 ☐ GND
  VDD ☐ 8│          │ 9 ☐ S1
         └──────────┘
```

16-pin (173 mil) TSSOP

CLK Output Selection Table

S2	S1	S0	REF	CLK1	CLK2	CLK3
0	0	0	OFF	33.30	50	125
0	0	1	ON	33.333	33.333	125
0	1	0	ON	33.333	66.666	125
0	1	1	ON	66.666	66.666	125
1	0	0	ON	33.333	50	125
1	0	1	ON	33.333	50	100
1	1	0	ON	33.333	66.666	100
1	1	1	ON	33.30	50	125

Note: All frequencies are in MHz.

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X2	Output	Crystal connection. Connect to 25 MHz crystal input or float for clock.
2	X1	Input	Crystal connection. Connect to 25 MHz crystal or clock input.
3	GND	Power	Connect to ground.
4	CLK3	Output	Selectable clock output. See table above for frequency. Weak internal pull-down when tri-state.
5	$\overline{\text{PDTS}}$	Input	Powers down entire chip and tri-states outputs when low. Internal pull-up resistor.
6	S2	Input	Select pin. Selects clock output frequency from table above. Internal pull-up resistor.
7	CLK2	Output	Selectable clock output. See table above for frequency. Weak internal pull-down when tri-state.
8	VDD	Power	Connect to +3.3 V.
9	S1	Input	Select pin. Selects clock output frequency from table above. Internal pull-up resistor.
10	GND	Power	Connect to ground.
11	CLK1	Output	Selectable clock output. See table above for frequency. Weak internal pull-down when tri-state.
12	VDD	Power	Connect to +3.3 V.
13	S0	Input	Select pin. Selects clock output frequency from table above. Internal pull-up resistor.

Pin Number	Pin Name	Pin Type	Pin Description
14	REF	Output	Reference 25 MHz clock output. Weak internal pull-down when tri-state.
15	GND	Power	Connect to ground.
16	VDD	Power	Connect to +3.3 V.

External Components

Decoupling Capacitor

As with any high performance mixed-signal IC, the ICS650-36 must be isolated from system power supply noise to perform optimally.

A decoupling capacitor of 0.01µF must be connected between each VDD and the PCB ground plane.

Series Termination Resistor

Clock output traces over one inch should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

Crystal Load Capacitors

The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors must be connected from each of the pins X1 and X2 to ground.

The value (in pF) of these crystal caps should equal (C_L -6 pF)*2. In this equation, C_L= crystal load capacitance in pF.

Example: For a crystal with a 16 pF load capacitance, each crystal capacitor would be 20 pF [(16-6) x 2 = 20].

PCB Layout Recommendations

Observed the following guidelines for optimum device performance and lowest output phase noise:

1) The 0.01µF decoupling capacitors should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitors and VDD pins. The PCB trace to VDD pins should be kept as short as possible, as should the PCB trace to the ground via.

2) The external crystal should be mounted just next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces, instead they should be separated and away from other traces.

3) Place the 33Ω series termination resistor (if needed) close to the clock output to minimize EMI.

4) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the ICS650-36. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS650-36. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	-0.5 V to 7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature (commercial)	0 to +70° C
Ambient Operating Temperature (industrial)	-40 to +85° C
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature (commercial)	0		+70	° C
Ambient Operating Temperature (industrial)	-40		+85	° C
Power Supply Voltage (measured in respect to GND)	+3.135	+3.3	+3.465	V

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.135	3.3	3.465	V
Supply Current	IDD	No load, $\overline{\text{PDTS}}$=1		25		mA
Power Down Current	IDDPD	No load, $\overline{\text{PDTS}}$=0		100		μA
Input High Voltage	V_{IH}	$\overline{\text{PDTS}}$, S2:0	2			V
Input Low Voltage	V_{IL}	$\overline{\text{PDTS}}$, S2:0			0.8	V
Output High Voltage	V_{OH}	I_{OH} = -4 mA	VDD-0.3			V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.4	V
Short Circuit Current	I_{OS}	Clock outputs		±65		mA
Input Capacitance, inputs	C_{IN}			5		pF
Nominal Output Impedance	Z_{OUT}			20		Ω
Internal Pull-up Resistor	R_{PU}	$\overline{\text{PDTS}}$, S2:0		500		kΩ
Internal Pull-down Resistor	R_{PD}	Outputs		250		kΩ

AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature -40 to +85° C

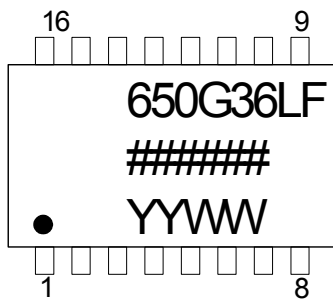| Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	f_{IN}			25		MHz
Output Rise Time	t_{OR}	20% to 80%, Note 1		0.8		ns
Output Fall Time	t_{OF}	80% to 20%, Note 1		0.7		ns
Output Clock Duty Cycle		at VDD/2, Note 1	40		60	%
Absolute Clock Period Jitter		Note 1		±125		ps
Clock Jitter, Cycle-to-Cycle		33.333M, 66.666M, Note 1		150		ps
Clock Jitter, Long Term		25M, n=1000, Note1		900		ps
Frequency Synthesis Error				0		ppm
Output Enable Time	t_{OE}	$\overline{\text{PDTS}}$ high to output locked to ±1%		350		μs
Output Disable Time	t_{OD}	$\overline{\text{PDTS}}$ low to tri-state		25		ns

Note 1: Measured with a 15 pF load.
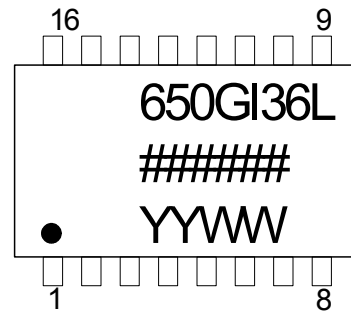
Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		78		$^\circ$C/W
	θ_{JA}	1 m/s air flow		70		$^\circ$C/W
	θ_{JA}	3 m/s air flow		68		$^\circ$C/W
Thermal Resistance Junction to Case	θ_{JC}			37		$^\circ$C/W

Marking Diagrams

(ICS650G-36LF)

16   9

650G36LF
######
● YYWW

1   8

(ICS650GI-36LF)

16   9

650GI36L
######
● YYWW

1   8

Notes:

1. ###### is the lot code.

2. YYWW is the last two digits of the year, and the week number that the part was assembled.

3. "LF" or "L" designates Pb free packaging.

4. "I" designates industrial temperature range.

5. Bottom marking: (origin). Origin = country of origin if not USA.

Package Outline and Package Dimensions (16-pin TSSOP, 173 Mil. Narrow Body)
Package dimensions are kept current with JEDEC Publication No. 95
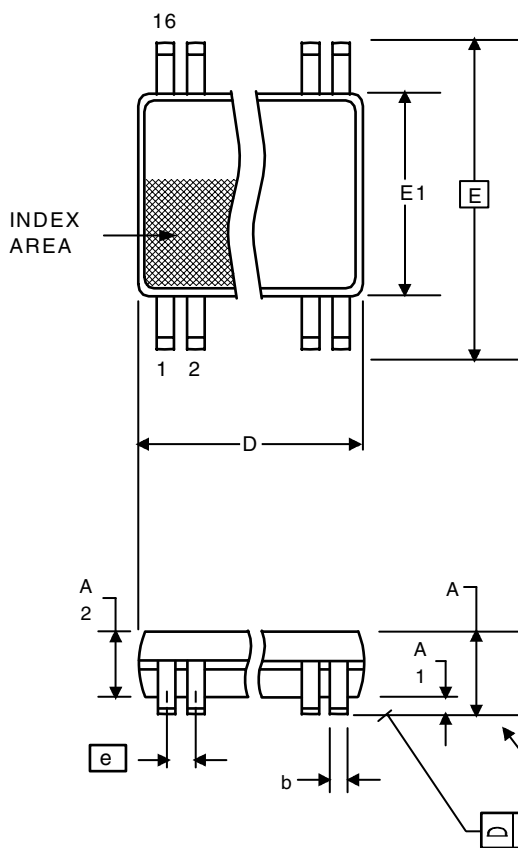
	Millimeters		Inches*	
Symbol	**Min**	**Max**	**Min**	**Max**
A	--	1.20	--	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	4.90	5.1	0.193	0.201
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	0.169	0.177
e	0.65 Basic		0.0256 Basic	
L	0.45	0.75	0.018	0.030
α	0°	8°	0°	8°
aaa	--	0.10	--	0.004

*For reference only. Controlling dimensions in mm.
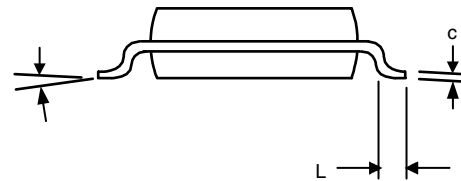
Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
650G-36LF		Tubes	16-pin TSSOP	0 to +70 °C
650G-36LFT	see page 6	Tape and Reel	16-pin TSSOP	0 to +70 °C
650GI-36LF		Tubes	16-pin TSSOP	-40 to +85 °C
650GI-36LFT		Tape and Reel	16-pin TSSOP	-40 to +85 °C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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