

Description

The ICS664-02 provides clock generation and conversion for clock rates commonly needed in HDTV digital video equipment. The ICS664-02 uses the latest Phase-Locked Loop (PLL) technology to provide excellent phase noise and long-term jitter performance for superior synchronization and S/N ratio.

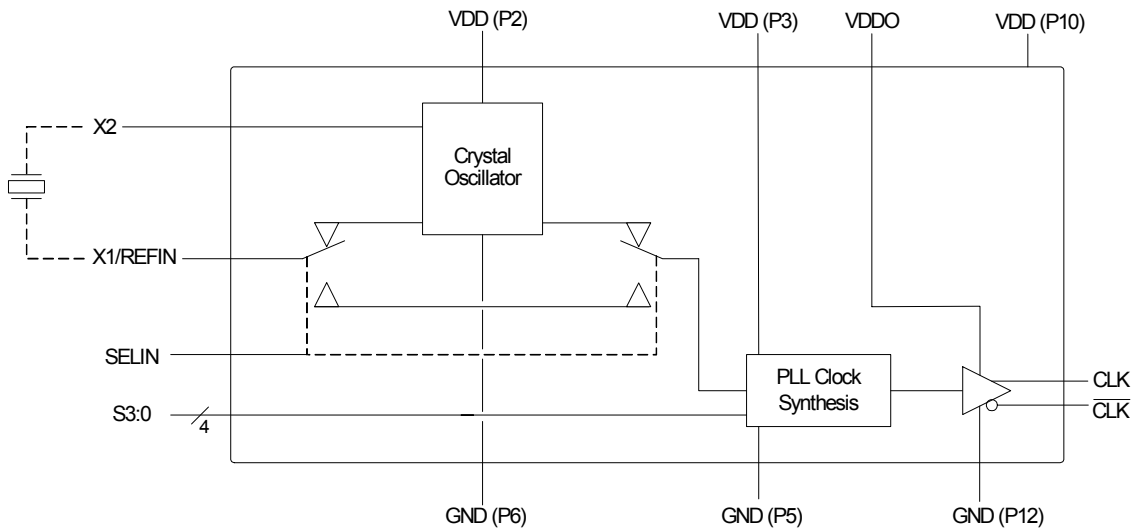
For audio sampling clocks generated from 27 MHz, use the ICS661.

Please contact IDT if you have a requirement for an input and output frequency not included in this document. IDT can rapidly modify this product to meet special requirements.

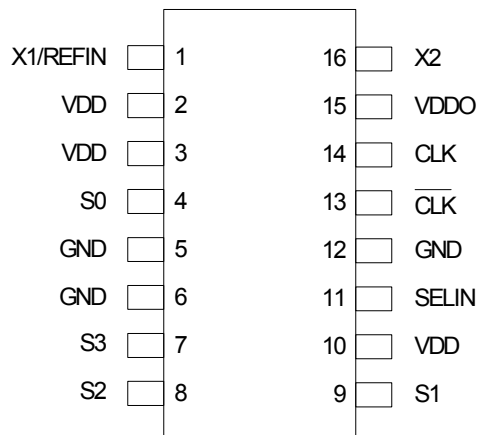
Features

- Packaged in 16-pin TSSOP
- Pb (lead) free package, RoHS compliant
- Clock or crystal input
- Low phase noise
- Low jitter
- Exact (0 ppm) multiplication ratios
- Power-down control
- Improved phase noise over ICS660
- Differential outputs
- Supports SMTE 292M HD-SDI standard for HDTV broadcast

Block Diagram



Pin Assignment



16-pin 4.40 mil body, 0.65 mm pitch TSSOP

Output Clock Selection Table

| S3 | S2 | S1 | S0 | Input Frequency (MHz) | Output Frequency (MHz) |
|----|----|----|----|-----------------------|------------------------|
| 0 | 0 | 0 | 0 | | Power down |
| 0 | 0 | 0 | 1 | Pass thru | Input Freq |
| 0 | 0 | 1 | 0 | 27 | 74.25 |
| 0 | 0 | 1 | 1 | 27 | 74.175824 |
| 0 | 1 | 0 | 0 | 13.5 | 74.25 |
| 0 | 1 | 0 | 1 | 13.5 | 74.175824 |
| 0 | 1 | 1 | 0 | RESERVED | RESERVED |
| 0 | 1 | 1 | 1 | RESERVED | RESERVED |
| 1 | 0 | 0 | 0 | 74.25 | 54 |
| 1 | 0 | 0 | 1 | 74.175824 | 54 |
| 1 | 0 | 1 | 0 | RESERVED | RESERVED |
| 1 | 0 | 1 | 1 | RESERVED | RESERVED |
| 1 | 1 | 0 | 0 | 54 | 74.25 |
| 1 | 1 | 0 | 1 | 54 | 74.175824 |
| 1 | 1 | 1 | 0 | 54 | 13.5 |
| 1 | 1 | 1 | 1 | 27 | 13.5 |

Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description |
|------------|----------|----------|---|
| 1 | X1/REFIN | Input | Connect this pin to a crystal or clock input |
| 2 | VDD | Power | Power supply for crystal oscillator. |
| 3 | VDD | Power | Power supply for PLL. |
| 4 | S0 | Input | Output frequency selection. Determines output frequency per table above. On chip pull-up. |
| 5 | GND | Power | Ground for PLL. |
| 6 | GND | Power | Ground for oscillator. |
| 7 | S3 | Input | Output frequency selection. Determines output frequency per table above. On chip pull-up. |
| 8 | S2 | Input | Output frequency selection. Determines output frequency per table above. On chip pull-up. |
| 9 | S1 | Input | Output frequency selection. Determines output frequency per table above. On chip pull-up. |
| 10 | VDD | Power | Power supply. |
| 11 | SELIN | Input | Low for clock input, high for crystal. On chip pull-up. |
| 12 | GND | Power | Ground for output stage |
| 13 | CLK | Output | Complimentary clock output. |
| 14 | CLK | Output | Clock output. |
| 15 | VDDO | Power | Power supply for output stage. |
| 16 | X2 | Input | Connect this pin to a crystal. Leave open if using a clock input. |

Application Information

Termination Resistor

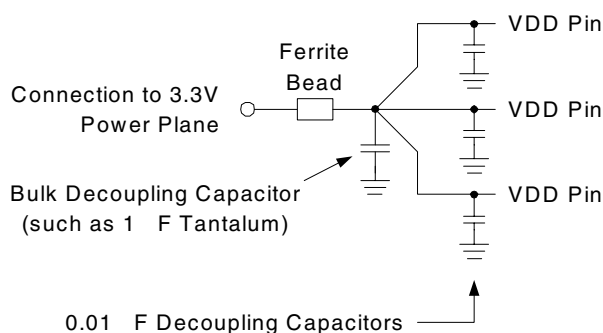
Terminate the outputs with 50Ω to ground.

Decoupling Capacitors

As with any high-performance mixed-signal IC, the ICS664-02 must be isolated from system power supply noise to perform optimally.

Decoupling capacitors of 0.01μF must be connected between each VDD and the PCB ground plane. To further guard against interfering system supply noise, the ICS664-02 should use one common connection to the PCB power plane as shown in the diagram on the next page. The ferrite bead and bulk capacitor help reduce lower frequency noise in the supply that can lead to output clock phase modulation.

Recommended Power Supply Connection for Optimal Device Performance



All power supply pins must be connected to the same voltage, except VDDO, which may be connected to a lower voltage in order to change the output level.

To achieve the absolute minimum jitter, power the part with a dedicated LDO regulator, which will provide high isolation from power supply noise. Many companies produce very small, inexpensive regulators; an example is the National Semiconductor LP2985.

Crystal Load Capacitors

If a crystal is used, the device crystal connections should include pads for capacitors from X1 to ground and from X2

to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. To reduce possible noise pickup, use very short PCB traces (and no vias) between the crystal and device.

The value of the load capacitors can be roughly determined by the formula $C = 2(C_L - 6)$ where C is the load capacitor connected to X1 and X2, and C_L is the specified value of the load capacitance for the crystal. A typical crystal C_L is 18 pF, so $C = 2(18 - 6) = 24$ pF. Because these capacitors adjust the stray capacitance of the PCB, check the output frequency using your final layout to see if the value of C should be changed.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

- 1) Each 0.01μF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.
- 2) The external crystal should be mounted next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces, instead they should be separated and away from other traces.
- 3) To minimize EMI, and obtain the best signal integrity, the 50Ω series termination resistor should be placed close to the clock output.
- 4) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (the ferrite bead and bulk decoupling capacitor can be mounted on the back). Other signal traces should be routed away from the ICS664-02. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS664-02. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|-------------------------------|--------------------|
| Supply Voltage, VDD | 5.5 V |
| All Inputs and Outputs | -0.5V to VDD+0.5 V |
| Ambient Operating Temperature | 0 to +70° C |
| Storage Temperature | -65 to +150° C |
| Junction Temperature | 125° C |
| Soldering Temperature | 260° C |

Recommended Operation Conditions

| Parameter | Min. | Typ. | Max. | Units |
|---|------|------|------|-------|
| Ambient Operating Temperature | 0 | | +70 | °C |
| Power Supply Voltage (measured in respect to GND) | +3.0 | | +3.6 | V |

DC Electrical Characteristics

Unless stated otherwise, VDD = 3.3 V ±10%, Ambient Temperature 0 to +70° C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---------------------------|-----------------|------------|----------|------|----------|-------|
| Operating Voltage | VDD | | 3.0 | | 3.6 | V |
| | VDDO | | 2.5 | | VDD | V |
| Supply Current | IDD | No Load | | 25 | | mA |
| Standby Supply Current | IDDPD | | | 75 | | μA |
| Input High Voltage | V _{IH} | | 2 | | | V |
| Input Low Voltage | V _{IL} | | | | 0.8 | V |
| Output High Voltage | V _{OH} | | VDDO-1.5 | | VDDO-1.1 | V |
| Output Low Voltage | V _{OL} | | VDDO-2.0 | | VDDO-1.8 | V |
| Input Capacitance | C _{IN} | input pins | | 7 | | pF |
| Internal Pull-up Resistor | R _{PU} | | | 120 | | kΩ |

AC Electrical Characteristics

Unless stated otherwise, $V_{DD} = 3.3\text{ V} \pm 10\%$, Ambient Temperature 0 to $+70^{\circ}\text{C}$

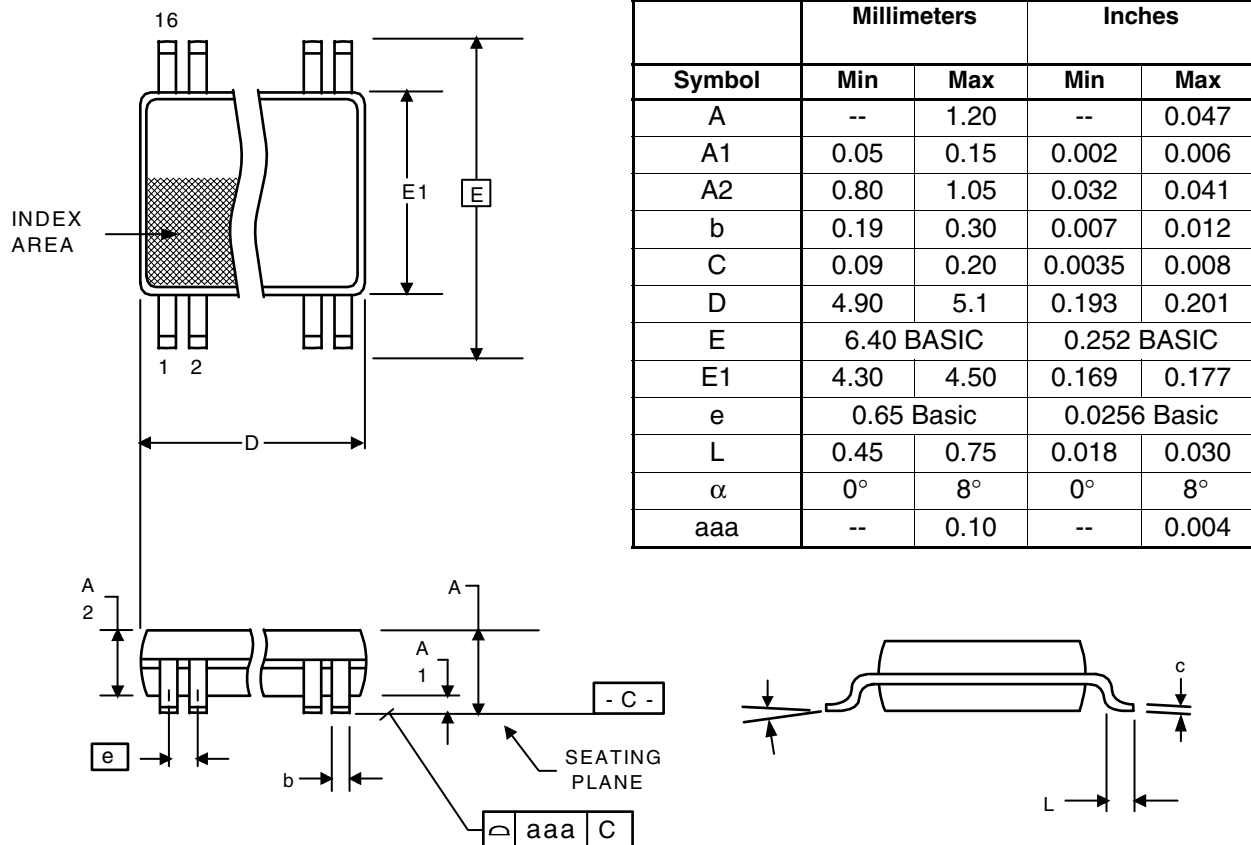
| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|----------|---|------|----------|------|---------------|
| Crystal Frequency | | | | | 28 | MHz |
| Output Clock Rise Time | t_{OR} | 20% to 80%, 15 pF load | | | 1.5 | ns |
| Output Clock Fall Time | t_{OF} | 80% to 20%, 15 pF load | | | 1.5 | ns |
| Output Duty Cycle | t_{OD} | at $V_{DD}/2$, 15 pF load | 40 | 49 to 51 | 60 | % |
| Power-up Time | t_{PU} | Inputs out of PD state to clocks stable | | | 10 | ms |
| Power-down Time | t_{PD} | Inputs in PD state to clocks off | | | 1 | μs |
| Jitter, Short term | | | | 70 | | ps p-p |
| Jitter, Long term | | 10 μs delay | | 300 | | ps p-p |
| Single Sideband Phase Noise | | 10 kHz offset | | -120 | | dBc |
| Actual Mean Frequency Error versus Target | | | | 0 | | ppm |

Thermal Characteristics

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|---------------|----------------|------|------|------|----------------------|
| Thermal Resistance Junction to Ambient | θ_{JA} | Still air | | 78 | | $^{\circ}\text{C/W}$ |
| | θ_{JA} | 1 m/s air flow | | 70 | | $^{\circ}\text{C/W}$ |
| | θ_{JA} | 3 m/s air flow | | 68 | | $^{\circ}\text{C/W}$ |
| Thermal Resistance Junction to Case | θ_{JC} | | | 37 | | $^{\circ}\text{C/W}$ |

Package Outline and Package Dimensions (16-pin TSSOP, 4.40 mm Body, 0.65 mm Pitch)

Package dimensions are kept current with JEDEC Publication No. 95, MO-153



Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---------------------|----------|--------------------|--------------|-------------|
| 664G-02LF | 664G02LF | Tubes | 16-pin TSSOP | 0 to +70° C |
| 664G-02LFT | 664G02LF | Tape and Reel | 16-pin TSSOP | 0 to +70° C |

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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