HIGH-SPEED 36K (4K x 9-BIT) SYNCHRONOUS PIPELINED DUAL-PORT SRAM

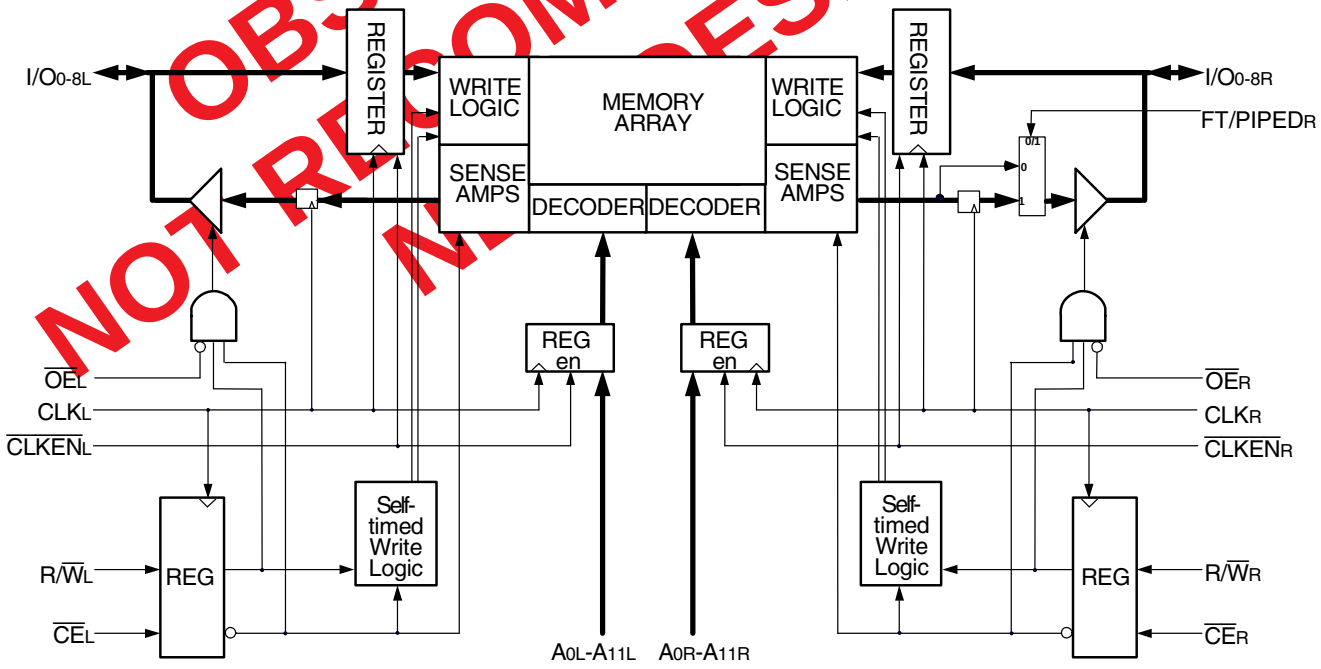
IDT709149S
OBSOLETE PART

LEAD FINISH (SnPb) ARE IN EOL PROCESS - LAST TIME BUY EXPIRES JUNE 15, 2018

Features

- **Architecture based on Dual-Port SRAM cells**
  - *Allows full simultaneous access from both ports*
- **High-speed clock-to-data output times**
  - *Commercial: 8/10/12ns (max.)*
  - *Industrial: 10ns (max.)*
- **Low-power operation**
  - *IDT709149S*
    Active: 1500mW (typ.)
    Standby: 75mW (typ.)
- **4K X 9 bits**
- **13ns cycle time, 76MHz operation in pipeline mode**
  - *Self-timed write allows for fast cycle times*
- **Synchronous operation**
  - *4ns setup to clock, 1ns hold on all control, data, and address inputs*
  - *Data input, address, and control registers*
  - *Fast 8ns clock to data out*
- **TTL-compatible, single 5V (±10%) power supply**
- **Clock Enable feature**
- **Guaranteed data output hold times**
- **Industrial temperature range (–40°C to +85°C) is available for selected speeds**
- **Green parts available, see ordering information**

Functional Block Diagram



3494 drw 01

FEBRUARY 2018

Description

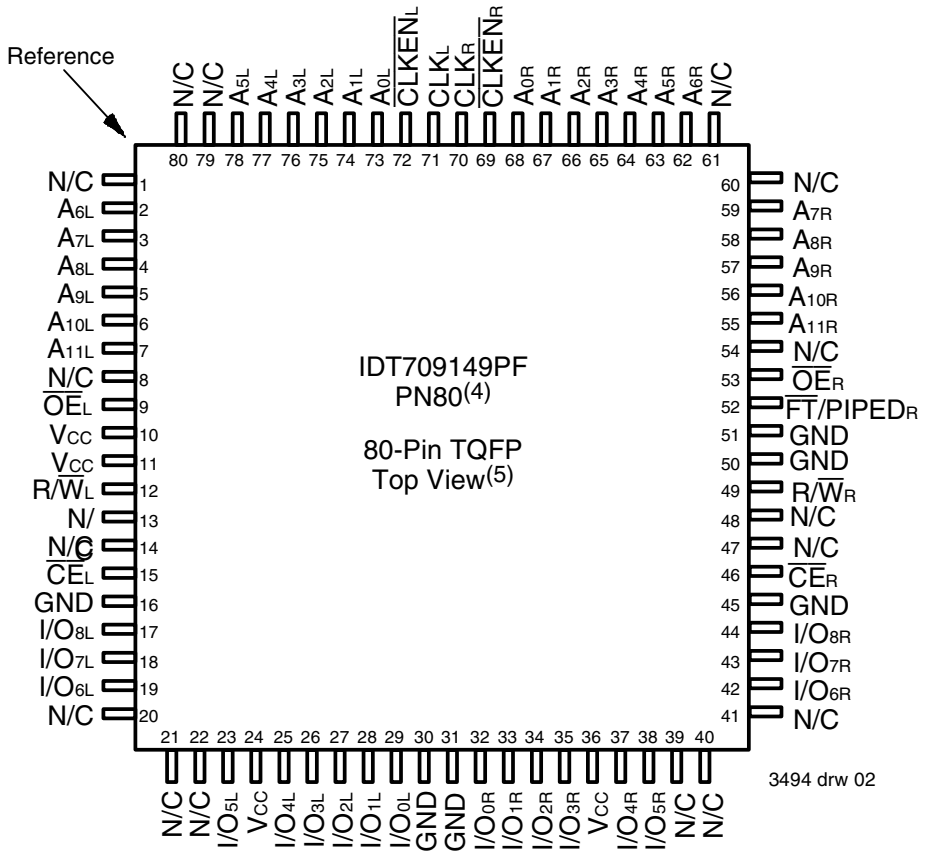
The IDT709149 is a high-speed 4K x 9 bit synchronous Dual-Port SRAM. The memory array is based on Dual-Port memory cells to allow simultaneous access from both ports. Registers on control, data, and address inputs provide low set-up and hold times. The timing latitude provided by this approach will allow systems to be designed with very short cycle times. This device has been optimized for applications having unidirectional data flow or bi-directional data flow in bursts, by utilizing input data registers.

The IDT709149 utilizes a 9-bit wide data path to allow for parity at the user's option. This feature is especially useful in data communication applications where it is necessary to use a parity bit for transmission/ reception error checking.

Fabricated using CMOS high-performance technology, these Dual-Ports typically operate on only 800mW of power at maximum high-speed clock-to-data output times as fast as 8ns. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

The IDT709149 is packaged in an 80-pin TQFP.

Pin Configurations[1,2,3]



NOTES:

1. All V_{CC} pins must be connected to power supply.
2. All ground pins must be connected to ground supply.
3. Package body is approximately 14mm x 14mm x 1.4mm.
4. This package code is used to reference the package diagram.
5. This text does not indicate the orientaion of the actual part-marking.

Absolute Maximum Ratings(1)

Symbol	Rating	Commercial & Industrial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
V_{TERM}(2)	Terminal Voltage	-0.5 to V_{CC}	V
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
I_{OUT}	DC Output Current	50	mA

3494 tbl 01

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} + 10% for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of $V_{TERM} \geq V_{CC}$ + 10%.

Capacitance (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	9	pF

3494 tbl 04

NOTES:
1. These parameters are determined by device characterization, but are not production tested.
2. 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.

Maximum Operating Temperature and Supply Voltage(1)

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%

3494 tbl 02

NOTES:
1. This is the parameter T_A. This is the "instant on" case temperature.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0(2)	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

3494 tbl 03

NOTES:
1. $V_{IL} \geq$ -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed V_{CC} + 10%.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	709149S		Unit
			Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current(1)	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	V_{OUT} = 0V to V_{CC}	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = +4mA	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	V

3494 tbl 05

NOTE:
1. At $V_{CC} \leq$ 2.0V, input leakages are undefined

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[4] (V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Version	709149S8 Com'l Only		709149S10 Com'l & Ind		709149S12 Com'l Only		Unit
				Typ.	Max.	Typ.	Max.	Typ.	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R$ = V_{IL}, Outputs Disabled, f = f_{MAX}[1]	COM'L	200	320	190	310	180	300	mA
			IND	—	—	190	340	—	—	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R$ = V_{IH}, f = f_{MAX}[1]	COM'L	100	150	90	150	85	140	mA
			IND	—	—	90	175	—	—	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH}[3] Active Port Outputs Disabled, f=f_{MAX}[1]	COM'L	180	230	170	220	160	210	mA
			IND	—	—	170	250	—	—	
I_{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ - 0.2V, $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V, f = 0[2]	COM'L	5	15	5	15	5	15	mA
			IND	—	—	5	20	—	—	
I_{SB4}	Full Standby Current (One Port - All CMOS Level Inputs)	$\overline{CE}_{"A"} \leq$ 0.2V and $\overline{CE}_{"B"} \geq V_{CC}$ - 0.2V[3] $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V Active Port Outputs Disabled, f = f_{MAX}[1]	COM'L	170	220	160	210	150	200	mA
			IND	—	—	160	240	—	—	

3494 tbl 06

NOTES:
1. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of 1/t_{CLK}, using "AC TEST CONDITIONS" at input levels of GND to 3V.
2. f = 0 means no address, clock, or control lines change. Applies only to input at CMOS level standby.
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
4. Vcc = 5V, T_A = 25°C for Typ, and are not production tested. $I_{CC\,DC}$ = 150mA (Typ).

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1,2 and 3

3494 tbl 07

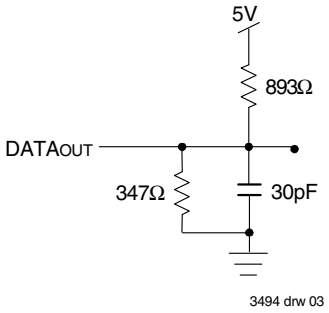


Figure 1. AC Output Test load.

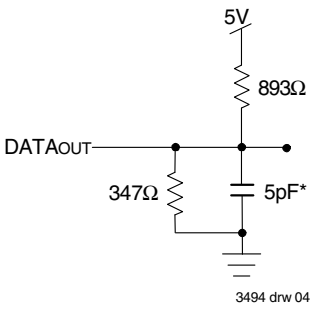


Figure 2. Output Test Load
(For t_{CKLZ}, t_{CKHZ}, t_{OLZ}, and t_{OHZ}).
*Including scope and jig.

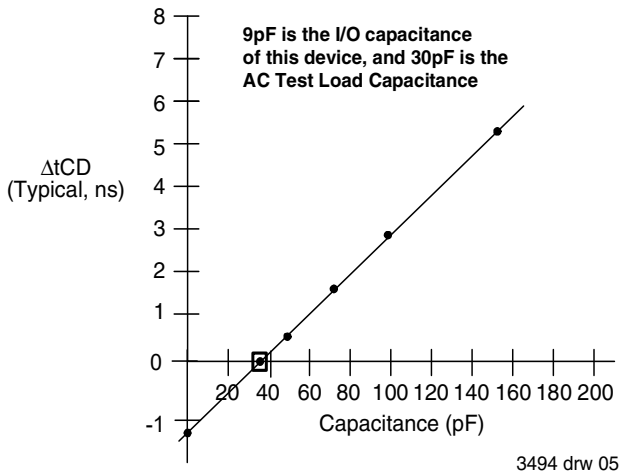


Figure 3. Typical Output Derating (Lumped Capacitive Load).

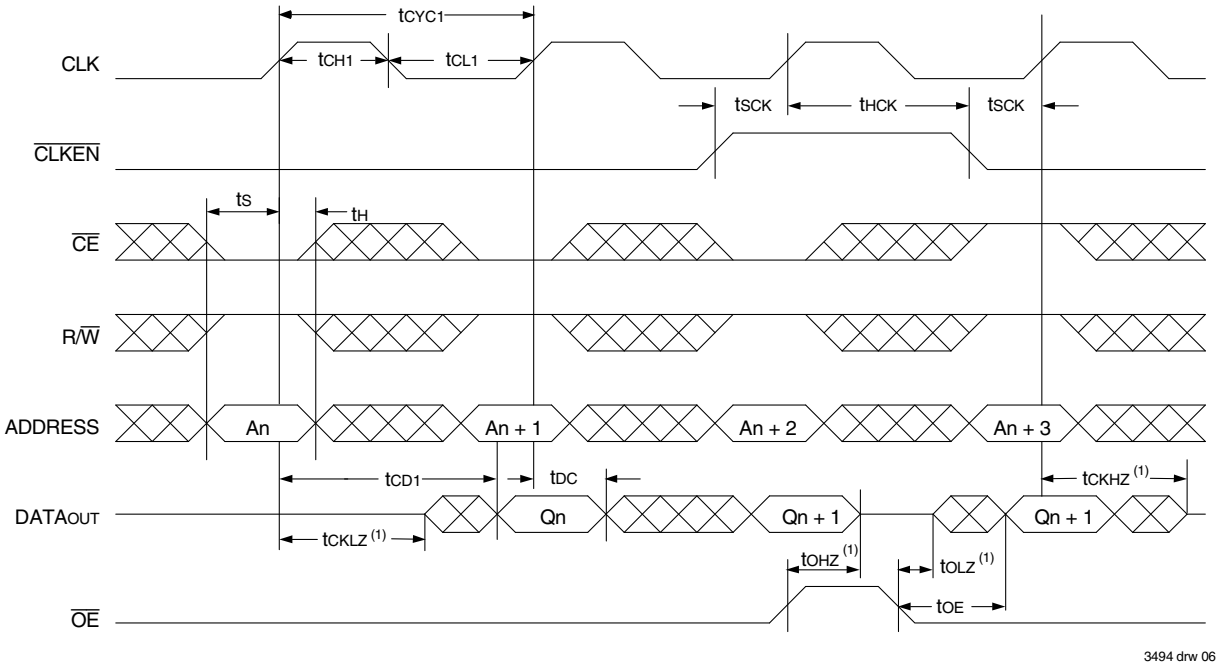
AC Electrical Characteristics Over the Operating Temperature Range— (Read and Write Cycle Timing)

Symbol	Parameter	709149S8 Com'l Only		709149S10 Com'l & Ind		709149S12 Com'l Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC1}	Clock Cycle Time (Flow-Through)[3]	16	—	20	—	20	—	ns
t_{CYC2}	Clock Cycle Time (Pipelined)[3]	13	—	15	—	16	—	ns
t_{CH1}	Clock High Time (Flow-Through)[3]	6	—	7	—	8	—	ns
t_{CL1}	Clock Low Time (Flow-Through)[3]	6	—	7	—	8	—	ns
t_{CH2}	Clock High Time (Pipelined)[3]	6	—	6	—	6	—	ns
t_{CL2}	Clock Low Time (Pipelined)[3]	6	—	6	—	6	—	ns
t_{CD1}	Clock to Data Valid (Flow-Through)[3]	—	12	—	15	—	20	ns
t_{CD2}	Clock to Data Valid (Pipelined)[3]	—	8	—	10	—	12	ns
t_S	Registered Signal Set-up Time	4	—	4	—	5	—	ns
t_H	Registered Signal Hold Time	1	—	1	—	1	—	ns
t_{DC}	Data Output Hold After Clock High	1	—	1	—	1	—	ns
t_{CKLZ}	Clock High to Output Low-Z[1,2]	2	—	2	—	**2**	—	ns
t_{CKHZ}	Clock High to Output High-Z[1,2]	—	7	—	7	—	9	ns
t_{OE}	Output Enable to Output Valid	—	8	—	8	—	10	ns
t_{OLZ}	Output Enable to Output Low-Z[1,2]	0	—	0	—	0	—	ns
t_{OHZ}	Output Disable to Output High-Z[1,2]	—	7	—	7	—	9	ns
t_{SCK}	Clock Enable, Disable Set-Up Time	4	—	4	—	5	—	ns
t_{HCK}	Clock Enable, Disable Hold Time	1	—	1	—	1	—	ns
t_{CWDD}	Write Port Clock High to Read Data Delay	—	25	—	30	—	35	ns

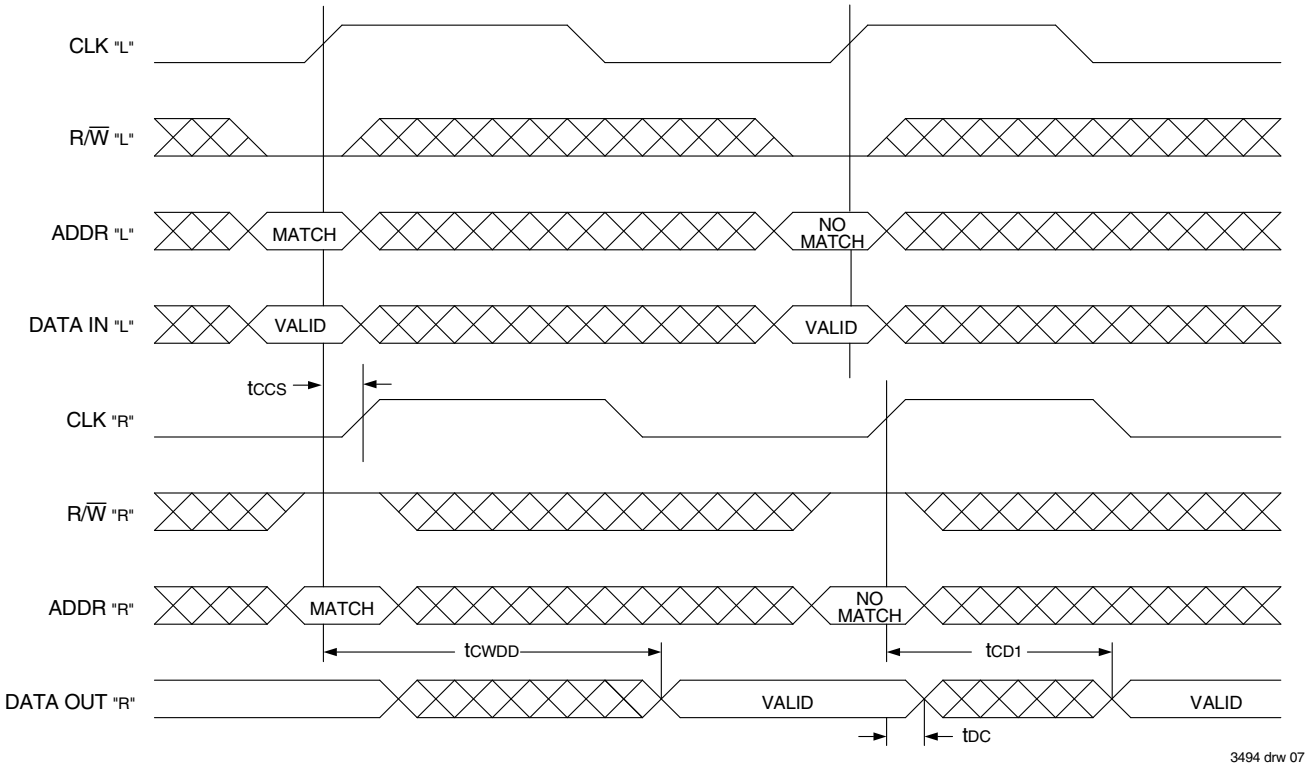
3494 tbl 08

NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. The Pipelined output parameters (t_{CYC2}, t_{CD2}) always apply to the Left Port. The Right Port uses the Pipelined t_{CYC2} and t_{CD2} when $\overline{FT}$/PIPED$_R$ = V_{IH} and the Flow-Through parameters (t_{CYC1}, t_{CD1}) when $\overline{FT}$/PIPED$_R$ = V_{IL}.

Timing Waveform of Read Cycle for Flow-Through Output on Right Port ($\overline{FT}$/Piped$_R$ = V$_{IL}$)

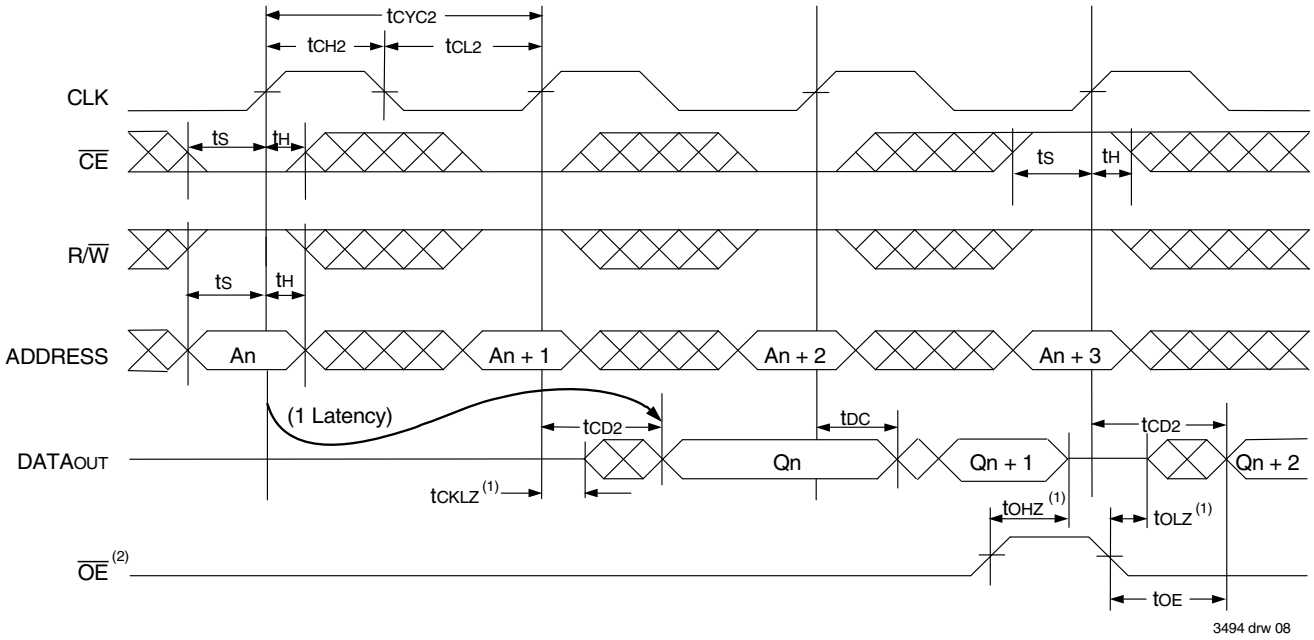


Timing Waveform of Left Port Write to Flow-Through Right Port Read ($\overline{FT}$/Piped$_R$ = V$_{IL}$)(2,3)



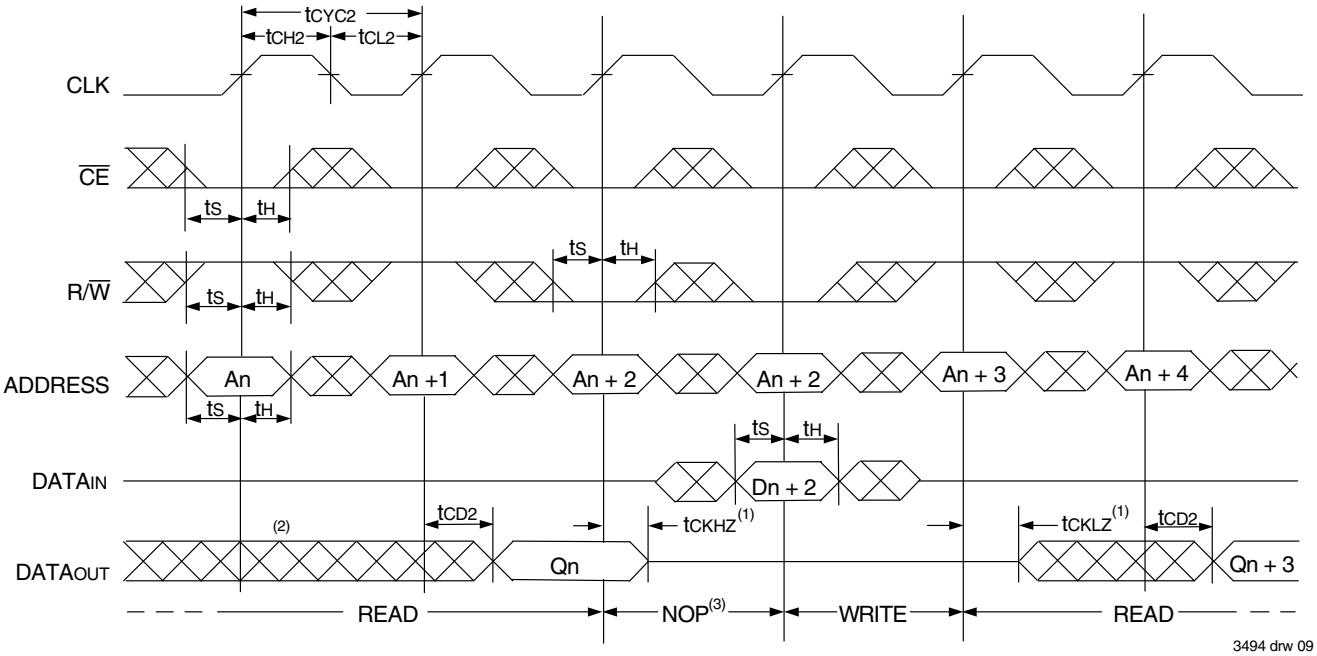
NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. $\overline{CE}_L$ = $\overline{CE}_R$ = V$_{IL}$, $\overline{CLKEN}_L$ = $\overline{CLKEN}_R$ = V$_{IL}$
3. $\overline{OE}$ = V$_{IL}$ for the reading port, port 'R'.

Timing Waveform of Read Cycle for Pipelined Operation (Left Port; Right Port when $\overline{FT}$/Piped$_R$ = V_{IH})(3)



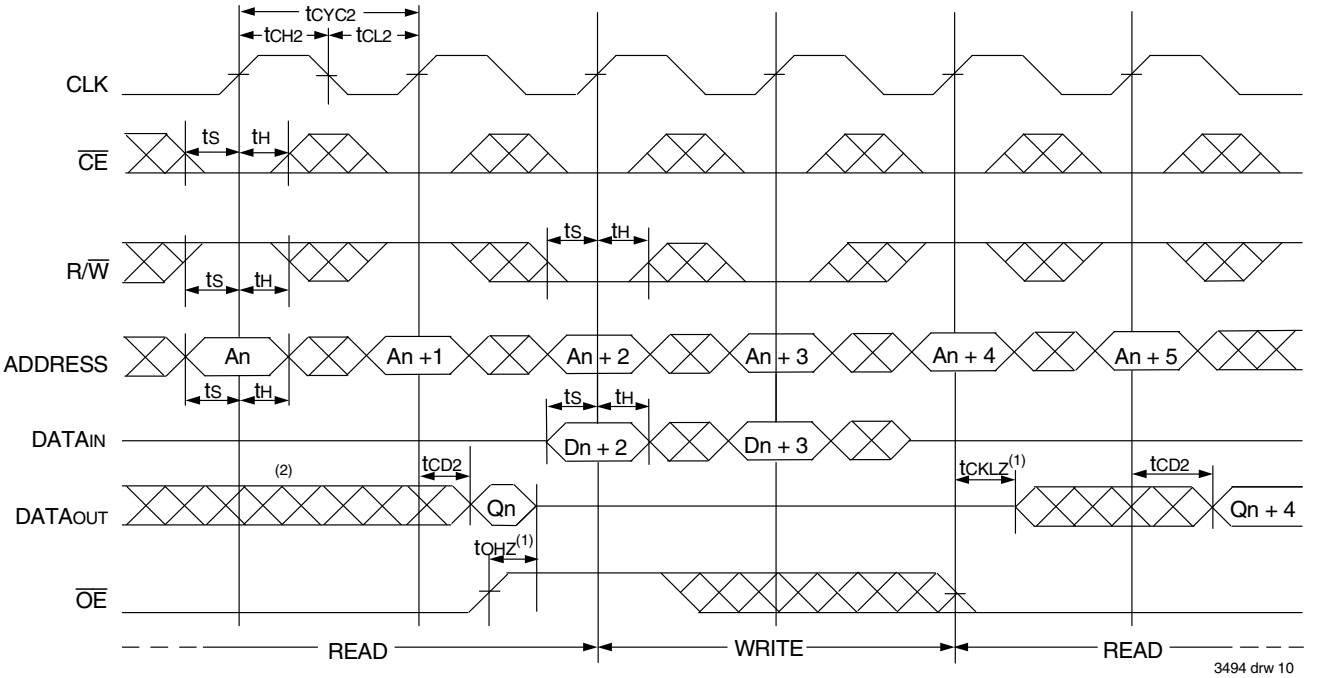
NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. $\overline{OE}$ is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
3. $\overline{CLKEN}_L$ and $\overline{CLKEN}_R$ = V_{IL}.

Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE}$ = VIL)



3494 drw 09

Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE}$ Controlled)



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NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
3. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

Functional Description

The IDT709149 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide very short set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal. An asynchronous output enable is provided to ease asynchronous bus interfacing.

The internal write pulse width is dependent only on the low to high transitions of the clock signal to initiate a write allowing the shortest possible realized cycle times. Clock enable inputs are provided to stall the operation of the address and data input registers without introducing clock skew for very fast interleaved memory applications.

A HIGH on the $\overline{CE}$ input for one clock cycle will power down the internal circuitry to reduce static power consumption.

When piplelined mode is enabled, two cycles are required with $\overline{CE}$ LOW to reactivate the outputs.

Truth Table I: Read/Write Control(1)

Inputs				Outputs	Mode
Synchronous(3)			Asynchronous		
CLK	$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	I/O_{0-8}	
↑	H	X	X	High-Z	Deselected—Power Down
↑	L	L	X	$DATA_{IN}$	Selected and Write Enable
↑	L	H	L	$DATA_{OUT}$	Read Selected and Data Output Enabled Read (1 Latency)
↑	X	X	H	High-Z	Data I/O Disabled

3494 tbl 09

Truth Table II: Clock Enable Function Table(1)

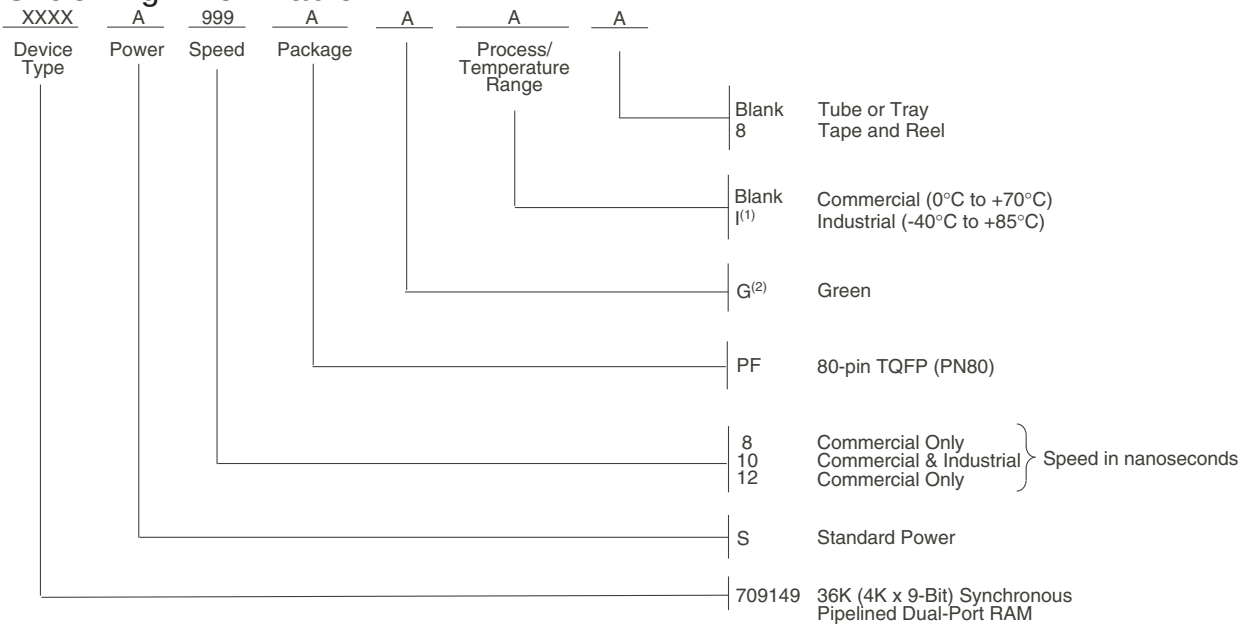
Operating Mode	Inputs		Register Inputs		Register Outputs(4)	
	CLK(3)	$\overline{CLKEN}$(2)	ADDR	$DATA_{IN}$	ADDR	$DATA_{OUT}$
Load "1"	↑	L	H	H	H	H
Load "0"	↑	L	L	L	L	L
Hold (do nothing)	↑	H	X	X	NC	NC
	X	H	X	X	NC	NC

3494 tbl 10

NOTES:

1. 'H' = HIGH voltage level steady state, 'h' = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition, 'L' = LOW voltage level steady state 'l' = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition, 'X' = Don't care, 'NC' = No change
2. $\overline{CLKEN}$ = V_{IL} must be clocked in during Power-Up.
3. Control signals are initialted and terminated on the rising edge of the CLK, depending on their input level. When R/W and $\overline{CE}$ are LOW, a write cycle is initiated on the LOW-to-HIGH transition of the CLK. Termination of a write cycle is done on the next LOW-to-HIGH transistion of the CLK.
4. The register outputs are internal signals from the register inputs being clocked in or disabled by $\overline{CLKEN}$.

Ordering Information



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NOTES:

1. Contact your local sales office for industrial temp range for other speeds, packages and powers.
2. Green parts available. For specific speeds, packages and powers contact your local sales office.
   LEAD FINISH (SnPb) parts are in EOL process. Product Discontinuation Notice - PDN# SP-17-02

Datasheet Document History

3/8/99:	Initiated datasheet document history
	Converted to new format
	Cosmetic and typographical corrections
	Added additional notes to pin configurations
6/3/99:	Changed drawing format
9/1/99:	Removed Preliminary
11/10/99:	Replaced IDT logo
5/24/00:	Page 3 Increased storage temperature parameter
	Clarified T_A parameter
	Page 5 DC Electrical parameters–changed wording from "open" to "disabled"
	Changed ±200mV to 0mV in notes
01/24/02:	Page 2 Added date revision for pin configuration
	Page 3, 4 & 5 Removed Industrial temp footnote from all tables
	Page 4 Added Industrial temp to 10ns speed in the column heading and values of DC Electrical Characteristics
	Page 5 Corrected a typo in the column heading of AC Electrical Characteristics
	Page 5 Added Industrial temp to 10ns speed in the column heading of AC Electrical Characteristics
	Page 10 Added Industrial temp to 10ns offering in ordering information
	Pages 1& 10 Replaced ™ logo with ® logo
01/29/09:	Page 10 Removed "IDT" from orderable part number
04/08/15:	Page 2 Removed IDT in reference to fabrication
	Page 2 &10 The package code PN80-1 changed to PN80 to match standard package codes
	Page 4 Corrected typo in the Typical Output Derating(Lumped Capitive Load) diagram
02/02/18:	Page 10 Added Tape and Reel and Green indicators with their footnote annotations to the Ordering Information
	Product Discontinuation Notice - PDN# SP-17-02
	Last time buy expires June 15, 2018
03/05/20:	709149 Datasheet changed to Obsolete Status

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