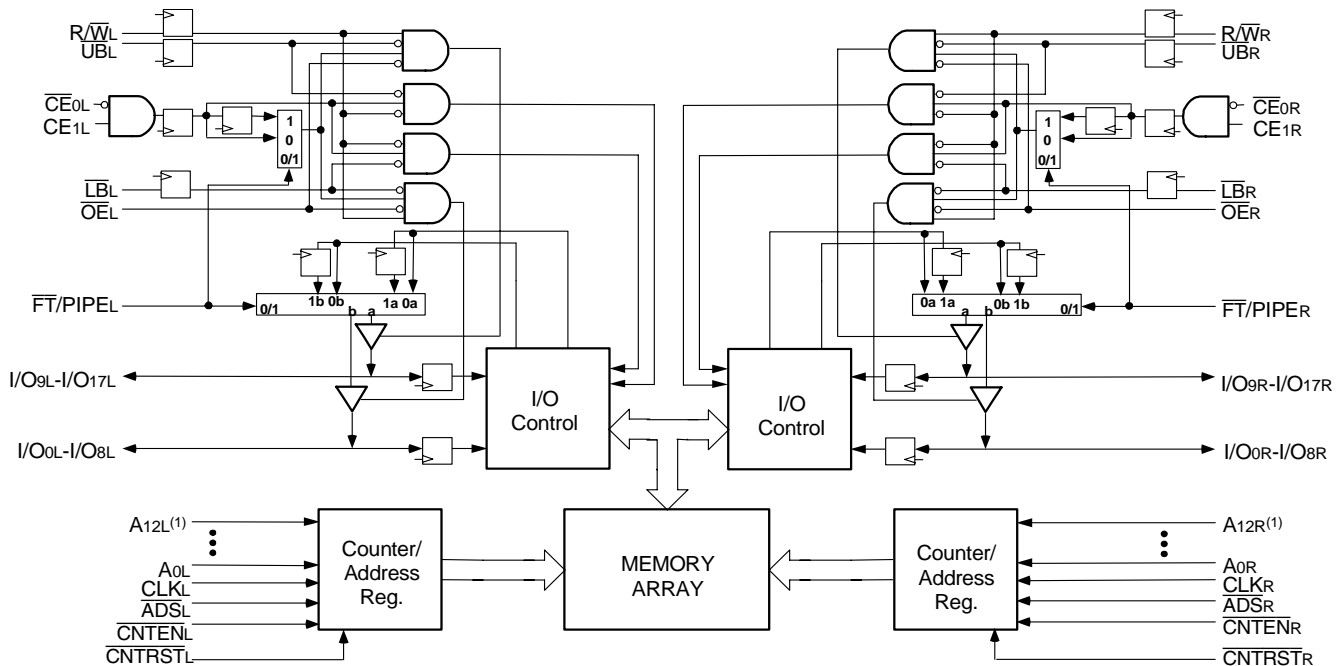


LEAD FINISH (SnPb) ARE IN EOL PROCESS - LAST TIME BUY EXPIRES JUNE 15, 2018

Features

- ◆ True Dual-Ported memory cells which allow simultaneous access of the same memory location
- ◆ High-speed clock to data access
 - Commercial: 6.5/7.5/9ns (max.)
 - Industrial: 7.5ns (max.)
- ◆ Low-power operation
 - IDT709359/49L
 - Active: 925mW (typ.)
 - Standby: 2.5mW (typ.)
- ◆ Flow-Through or Pipelined output mode on either Port via the FT/PIPEL pins
- ◆ Counter enable and reset features
- ◆ Dual chip enables allow for depth expansion without additional logic
- ◆ Full synchronous operation on both ports
 - 3.5ns setup to clock and 0ns hold on all control, data, and address inputs
 - Data input, address, and control registers
 - Fast 6.5ns clock to data out in the Pipelined output mode
 - Self-timed write allows fast cycle time
 - 10ns cycle time, 100MHz operation in Pipelined output mode
- ◆ Separate upper-byte and lower-byte controls for multiplexed bus and bus matching compatibility
- ◆ TTL-compatible, single 5V (±10%) power supply
- ◆ Industrial temperature range (-40°C to +85°C) is available for 83 MHz
- ◆ Available in a 100-pin Thin Quad Flatpack (TQFP) package
- ◆ Green parts available, see ordering information

Functional Block Diagram



5633 drw 01

NOTE:

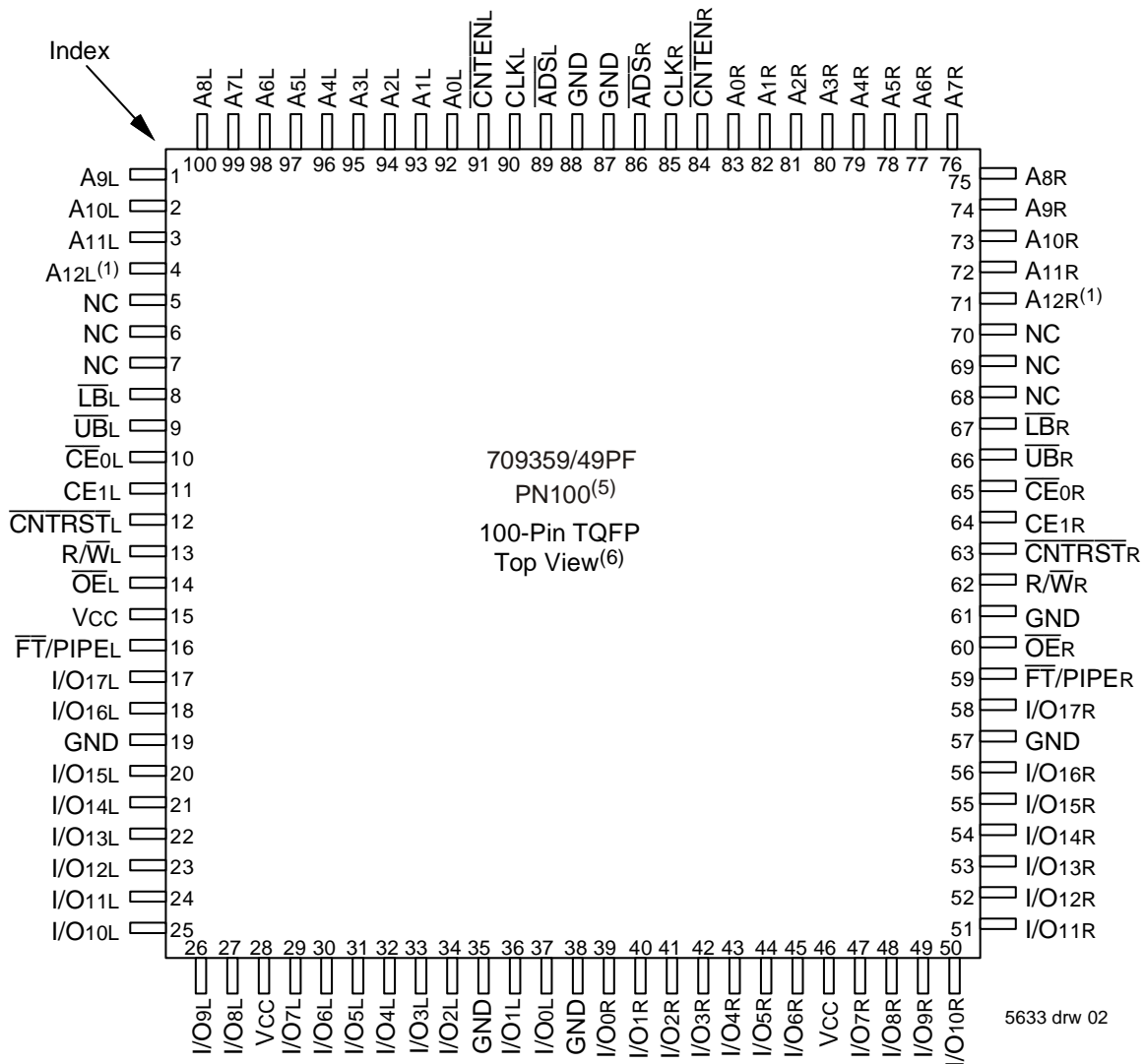
1. A12 is a NC for IDT709349.

Description

The IDT709359/49 is a high-speed 8/4K x 18 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times.

With an input data register, the IDT709359/49 has been optimized for applications having unidirectional or bidirectional data flow in bursts. An automatic power down feature, controlled by \overline{CE}_0 and CE_1 , permits the on-chip circuitry of each port to enter a very low standby power mode. Fabricated using CMOS high-performance technology, these devices typically operate on only 925mW of power.

Pin Configurations^(1,2,3,4)



NOTES:

1. A12 is a NC for IDT709349.
2. All Vcc pins must be connected to power supply.
3. All GND pins must be connected to ground.
4. Package body is approximately 14mm x 14mm x 1.4mm
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

Pin Names

Left Port	Right Port	Names
\overline{CE}_{0L} , CE_{1L}	\overline{CE}_{0R} , CE_{1R}	Chip Enables ⁽³⁾
R/\overline{W}_L	R/\overline{W}_R	Read/Write Enable
\overline{OE}_L	\overline{OE}_R	Output Enable
$A_{0L} - A_{12L}^{(1)}$	$A_{0R} - A_{12R}^{(1)}$	Address
$I/O_{0L} - I/O_{17L}$	$I/O_{0R} - I/O_{17R}$	Data Input/Output
CLK_L	CLK_R	Clock
\overline{UB}_L	\overline{UB}_R	Upper Byte Select ⁽²⁾
\overline{LB}_L	\overline{LB}_R	Lower Byte Select ⁽²⁾
\overline{ADS}_L	\overline{ADS}_R	Address Strobe
\overline{CNTEN}_L	\overline{CNTEN}_R	Counter Enable
\overline{CNTRST}_L	\overline{CNTRST}_R	Counter Reset
$\overline{FT}/PIPE_L$	$\overline{FT}/PIPE_R$	Flow-Through/Pipeline
Vcc		Power (5V)
GND		Ground (0V)

NOTES:

1. A12 is a NC for IDT709349.
2. \overline{LB} and \overline{UB} are single buffered regardless of state of $\overline{FT}/PIPE$.
3. \overline{CE}_0 and CE_1 are single buffered when $\overline{FT}/PIPE = V_{IL}$, \overline{CE}_0 and CE_1 are double buffered when $\overline{FT}/PIPE = V_{IH}$, i.e. the signals take two cycles to deselect.

5633 tbl 01

Truth Table I—Read/Write and Enable Control^(1,2,3)

\overline{OE}	CLK	$\overline{CE}_0^{(5)}$	$CE_1^{(5)}$	$\overline{UB}^{(4)}$	$\overline{LB}^{(4)}$	R/ \overline{W}	Upper Byte I/O ₉₋₁₇	Lower Byte I/O ₀₋₈	Mode
X	↑	H	X	X	X	X	High-Z	High-Z	Deselected—Power Down
X	↑	X	L	X	X	X	High-Z	High-Z	Deselected—Power Down
X	↑	L	H	H	H	X	High-Z	High-Z	Both Bytes Deselected
X	↑	L	H	L	H	L	DATA _{IN}	High-Z	Write to Upper Byte Only
X	↑	L	H	H	L	L	High-Z	DATA _{IN}	Write to Lower Byte Only
X	↑	L	H	L	L	L	DATA _{IN}	DATA _{IN}	Write to Both Bytes
L	↑	L	H	L	H	H	DATA _{OUT}	High-Z	Read Upper Byte Only
L	↑	L	H	H	L	H	High-Z	DATA _{OUT}	Read Lower Byte Only
L	↑	L	H	L	L	H	DATA _{OUT}	DATA _{OUT}	Read Both Bytes
H	X	L	H	X	X	X	High-Z	High-Z	Outputs Disabled

NOTES:

1. "H" = V_{IH} , "L" = V_{IL} , "X" = Don't Care.
2. \overline{ADS} , \overline{CNTEN} , $\overline{CNTRST} = X$.
3. \overline{OE} is an asynchronous input signal.
4. \overline{LB} and \overline{UB} are single buffered regardless of state of $\overline{FT}/PIPE$.
5. \overline{CE}_0 and CE_1 are single buffered when $\overline{FT}/PIPE = V_{IL}$. \overline{CE}_0 and CE_1 are double buffered when $\overline{FT}/PIPE = V_{IH}$, i.e. the signals take two cycles to deselect.

5633 tbl 02

Truth Table II—Address Counter Control^(1,2)

External Address	Previous Internal Address	Internal Address Used	CLK	\overline{ADS}	\overline{CNTEN}	\overline{CNRST}	I/O ⁽³⁾	MODE
An	X	An	↑	L ⁽⁴⁾	X	H	Dvo (n)	External Address Used
X	An	An + 1	↑	H	L ⁽⁵⁾	H	Dvo(n+1)	Counter Enabled—Internal Address generation
X	An + 1	An + 1	↑	H	H	H	Dvo(n+1)	External Address Blocked—Counter disabled (An + 1 reused)
X	X	A0	↑	X	X	L ⁽⁴⁾	Dvo(0)	Counter Reset to Address 0

NOTES:

- "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
- $\overline{CE0}$, \overline{LB} , \overline{UB} , and \overline{OE} = V_{IL}; CE₁ and \overline{RW} = V_{IH}.
- Outputs configured in Flow-Through Output mode: if outputs are in Pipelined mode the data out will be delayed by one cycle.
- \overline{ADS} and \overline{CNRST} are independent of all other signals including $\overline{CE0}$, CE₁, \overline{UB} and \overline{LB} .
- The address counter advances if \overline{CNTEN} = V_{IL} on the rising edge of CLK, regardless of all other signals including $\overline{CE0}$, CE₁, \overline{UB} and \overline{LB} .

5633 tbl 03

Recommended Operating Temperature and Supply Voltage⁽¹⁾

Grade	Ambient Temperature ⁽¹⁾	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%

5633 tbl 04

NOTES:

- Industrial temperature: for specific speeds, packages and powers contact your sales office.
- This is the parameter T_A. This is the "instant on" case temperature.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V _{IH}	Input High Voltage	2.2	—	6.0 ⁽¹⁾	V
V _{IL}	Input Low Voltage	-0.5 ⁽²⁾	—	0.8	V

5633 tbl 05

NOTES:

- V_{TERM} must not exceed Vcc + 10%.
- V_{IL} ≥ -1.5V for pulse width less than 10ns.

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Commercial & Industrial	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
T _{STG}	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	50	mA

5633 tbl 06

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{TERM} must not exceed Vcc + 10% for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of V_{TERM} ≥ Vcc + 10%.

Capacitance⁽¹⁾(T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions ⁽²⁾	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 3dV	9	pF
C _{OUT} ⁽³⁾	Output Capacitance	V _{OUT} = 3dV	10	pF

5633 tbl 07

NOTES:

- These parameters are determined by device characterization, but are not production tested.
- 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
- C_{OUT} also references C_{I/O}.

DC Electrical Characteristics Over the Operating Temperature Supply Voltage Range ($V_{CC} = 5.0V \pm 10\%$)

Symbol	Parameter	Test Conditions	709359/49L		Unit
			Min.	Max.	
$ I_{LI} $	Input Leakage Current ⁽¹⁾	$V_{CC} = 5.5V, V_{IN} = 0V$ to V_{CC}	—	5	μA
$ I_{LO} $	Output Leakage Current	$\overline{CE}_0 = V_{IH}$ or $CE_1 = V_{IL}, V_{OUT} = 0V$ to V_{CC}	—	5	μA
V_{OL}	Output Low Voltage	$I_{OL} = +4mA$	—	0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -4mA$	2.4	—	V

5633 tbl 08

NOTE:

- At $V_{CC} \leq 2.0V$ input leakages are undefined.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range⁽³⁾ ($V_{CC} = 5V \pm 10\%$)

Symbol	Parameter	Test Condition	Version	709359/49L6 Com'l Only		709359/49L7 Com'l & Ind		709359/49L9 Com'l Only		Unit
				Typ. ⁽⁴⁾	Max.	Typ. ⁽⁴⁾	Max.	Typ. ⁽⁴⁾	Max.	
ICC	Dynamic Operating Current (Both Ports Active)	\overline{CE}_L and $\overline{CE}_R = V_{IL}$ Outputs Disabled $f = f_{MAX}^{(1)}$	COM'L L	230	430	210	400	185	360	mA
			IND L	—	—	210	440	—	—	
ISB1	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L = \overline{CE}_R = V_{IH}$ $f = f_{MAX}^{(1)}$	COM'L L	45	115	40	105	35	95	mA
			IND L	—	—	40	120	—	—	
ISB2	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}^A = V_{IL}$ and $\overline{CE}^B = V_{IH}^{(3)}$ Active Port Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L L	150	235	135	220	120	205	mA
			IND L	—	—	135	235	—	—	
ISB3	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports CE_R and $CE_L \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V, f = 0^{(2)}$	COM'L L	0.5	3.0	0.5	3.0	0.5	3.0	mA
			IND L	—	—	0.5	3.0	—	—	
ISB4	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}^A \leq 0.2V$ and $\overline{CE}^B \geq V_{CC} - 0.2V^{(5)}$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, Active Port Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L L	160	210	130	190	110	170	mA
			IND L	—	—	130	205	—	—	

5633 tbl 09

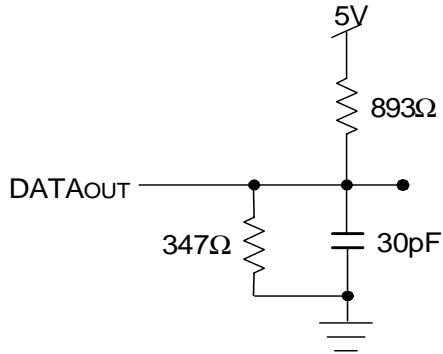
NOTES:

- At $f = f_{MAX}$, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of $1/t_{cvc}$, using "AC TEST CONDITIONS" at input levels of GND to 3V.
- $f = 0$ means no address, clock, or control lines change. Applies only to input at CMOS level standby.
- Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- $V_{CC} = 5V, TA = 25^\circ C$ for Typ, and are not production tested. $I_{CC DC}(f=0) = 150mA$ (Typ).
- $CE_X = V_{IL}$ means $\overline{CE}_{0X} = V_{IL}$ and $CE_{1X} = V_{IH}$
 $CE_X = V_{IH}$ means $\overline{CE}_{0X} = V_{IH}$ or $CE_{1X} = V_{IL}$
 $CE_X \leq 0.2V$ means $\overline{CE}_{0X} \leq 0.2V$ and $CE_{1X} \geq V_{CC} - 0.2V$
 $CE_X \geq V_{CC} - 0.2V$ means $\overline{CE}_{0X} \geq V_{CC} - 0.2V$ or $CE_{1X} \leq 0.2V$
"X" represents "L" for left port or "R" for right port.

AC Test Conditions

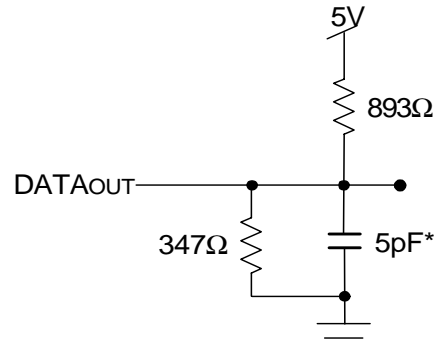
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	2ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1, 2 and 3

5633 tbl 10



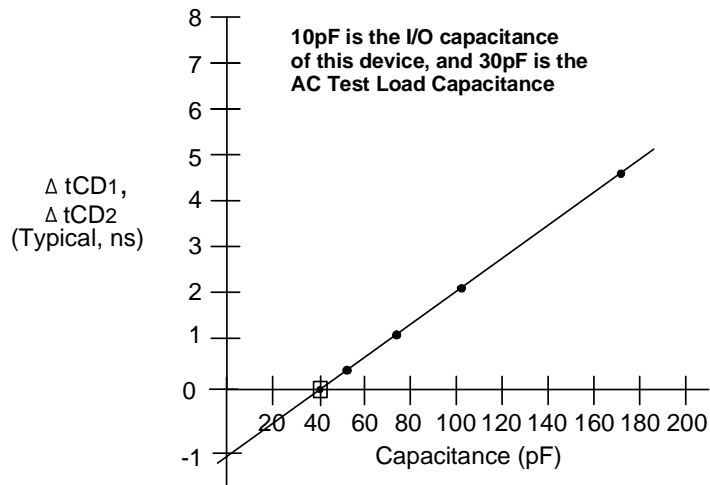
5633 drw 04

Figure 1. AC Output Test load.



5633 drw 05

Figure 2. Output Test Load
(For tCKLZ, tCKHZ, tOLZ, and tOHZ).
*Including scope and jig.



5633 drw 06

Figure 3. Typical Output Derating (Lumped Capacitive Load).

AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)⁽³⁾ (V_{CC} = 5V ± 10%)

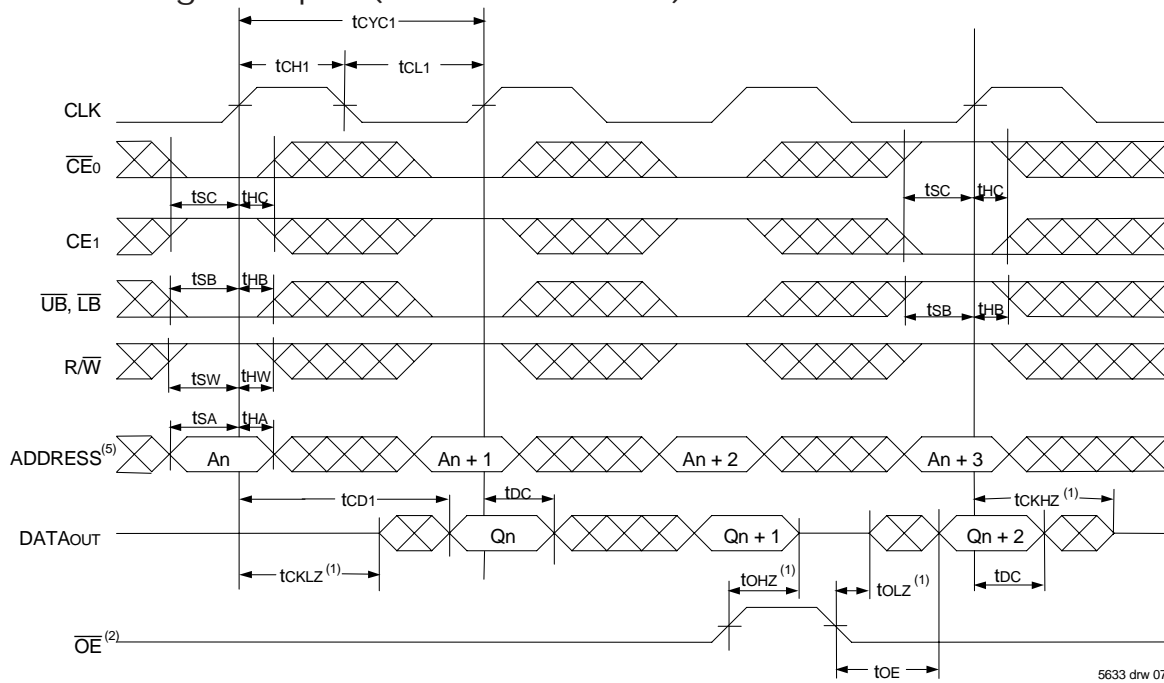
Symbol	Parameter	709359/49L6 Com'l Only		709359/49L7 Com'l & Ind		709359/49L9 Com'l Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{CYC1}	Clock Cycle Time (Flow-Through) ⁽²⁾	19	—	22	—	25	—	ns
t _{CYC2}	Clock Cycle Time (Pipelined) ⁽²⁾	10	—	12	—	15	—	ns
t _{CH1}	Clock High Time (Flow-Through) ⁽²⁾	6.5	—	7.5	—	12	—	ns
t _{CL1}	Clock Low Time (Flow-Through) ⁽²⁾	6.5	—	7.5	—	12	—	ns
t _{CH2}	Clock High Time (Pipelined) ⁽²⁾	4	—	5	—	6	—	ns
t _{CL2}	Clock Low Time (Pipelined) ⁽²⁾	4	—	5	—	6	—	ns
t _r	Clock Rise Time	—	3	—	3	—	3	ns
t _f	Clock Fall Time	—	3	—	3	—	3	ns
t _{SA}	Address Setup Time	3.5	—	4	—	4	—	ns
t _{HA}	Address Hold Time	0	—	0	—	1	—	ns
t _{SC}	Chip Enable Setup Time	3.5	—	4	—	4	—	ns
t _{HC}	Chip Enable Hold Time	0	—	0	—	1	—	ns
t _{SB}	Byte Enable Setup Time	3.5	—	4	—	4	—	ns
t _{HB}	Byte Enable Hold Time	0	—	0	—	1	—	ns
t _{SW}	R/W Setup Time	3.5	—	4	—	4	—	ns
t _{HW}	R/W Hold Time	0	—	0	—	1	—	ns
t _{SD}	Input Data Setup Time	3.5	—	4	—	4	—	ns
t _{HD}	Input Data Hold Time	0	—	0	—	1	—	ns
t _{SAD}	$\overline{\text{ADS}}$ Setup Time	3.5	—	4	—	4	—	ns
t _{HAD}	$\overline{\text{ADS}}$ Hold Time	0	—	0	—	1	—	ns
t _{SCN}	$\overline{\text{CNTEN}}$ Setup Time	3.5	—	4	—	4	—	ns
t _{HCN}	$\overline{\text{CNTEN}}$ Hold Time	0	—	0	—	1	—	ns
t _{SRST}	$\overline{\text{CNTRST}}$ Setup Time	3.5	—	4	—	4	—	ns
t _{HRST}	$\overline{\text{CNTRST}}$ Hold Time	0	—	0	—	1	—	ns
t _{OE}	Output Enable to Data Valid	—	6.5	—	7.5	—	9	ns
t _{OLZ}	Output Enable to Output Low-Z ⁽¹⁾	2	—	2	—	2	—	ns
t _{OHZ}	Output Enable to Output High-Z ⁽¹⁾	1	7	1	7	1	7	ns
t _{CD1}	Clock to Data Valid (Flow-Through) ⁽²⁾	—	15	—	18	—	20	ns
t _{CD2}	Clock to Data Valid (Pipelined) ⁽²⁾	—	6.5	—	7.5	—	9	ns
t _{DC}	Data Output Hold After Clock High	2	—	2	—	2	—	ns
t _{CKHZ}	Clock High to Output High-Z ⁽¹⁾	2	9	2	9	2	9	ns
t _{CKLZ}	Clock High to Output Low-Z ⁽¹⁾	2	—	2	—	2	—	ns
Port-to-Port Delay								
t _{CWDD}	Write Port Clock High to Read Data Delay	—	24	—	28	—	35	ns
t _{CCS}	Clock-to-Clock Setup Time	—	9	—	10	—	15	ns

NOTES:

- Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2). This parameter is guaranteed by device characterization, but is not production tested.
- The Pipelined output parameters (t_{CYC2}, t_{CD2}) to either the Left or Right ports when $\overline{\text{FT}}/\text{PIPE} = \text{V}_{\text{IH}}$. Flow-Through parameters (t_{CYC1}, t_{CD1}) apply when $\overline{\text{FT}}/\text{PIPE} = \text{V}_{\text{IL}}$ for that port.
- All input signals are synchronous with respect to the clock except for the asynchronous Output Enable ($\overline{\text{OE}}$), $\overline{\text{FT}}/\text{PIPER}$ and $\overline{\text{FT}}/\text{PIPEL}$.

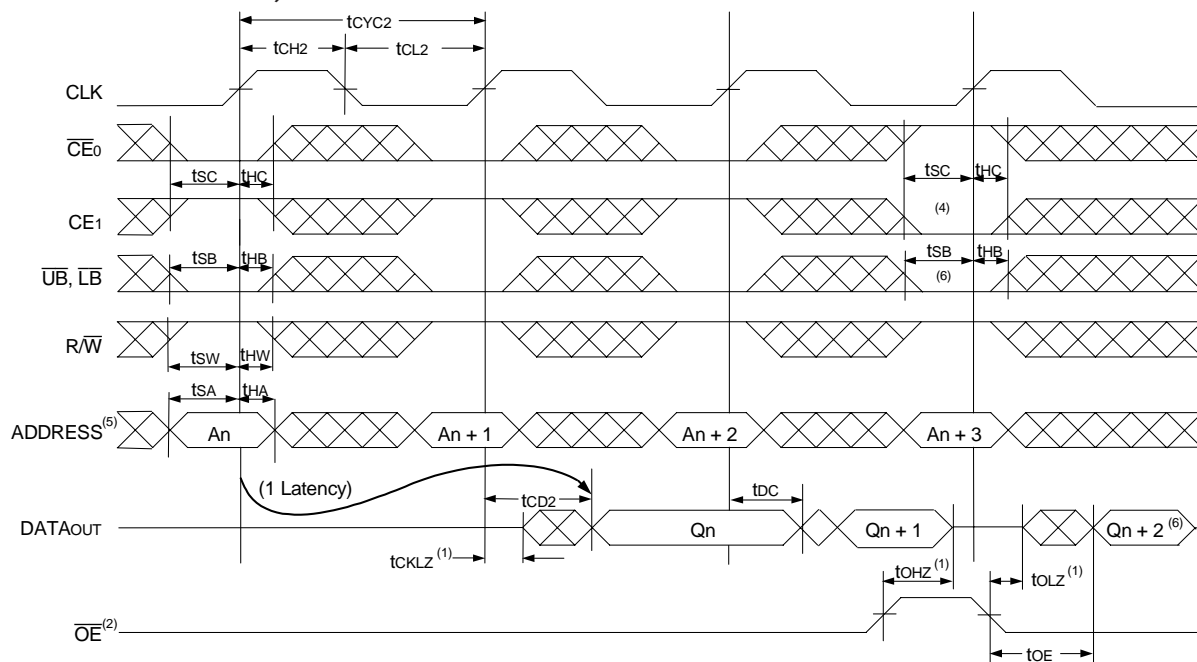
5633 tbl 11

Timing Waveform of Read Cycle for Flow-Through Output ($\overline{\text{FT}}/\text{PIPE} \text{ "X" } = \text{V}_{\text{IL}}$)^(3,7)



5633 drw 07

Timing Waveform of Read Cycle for Pipelined Operation ($\overline{\text{FT}}/\text{PIPE} \text{ "X" } = \text{V}_{\text{IH}}$)^(3,7)

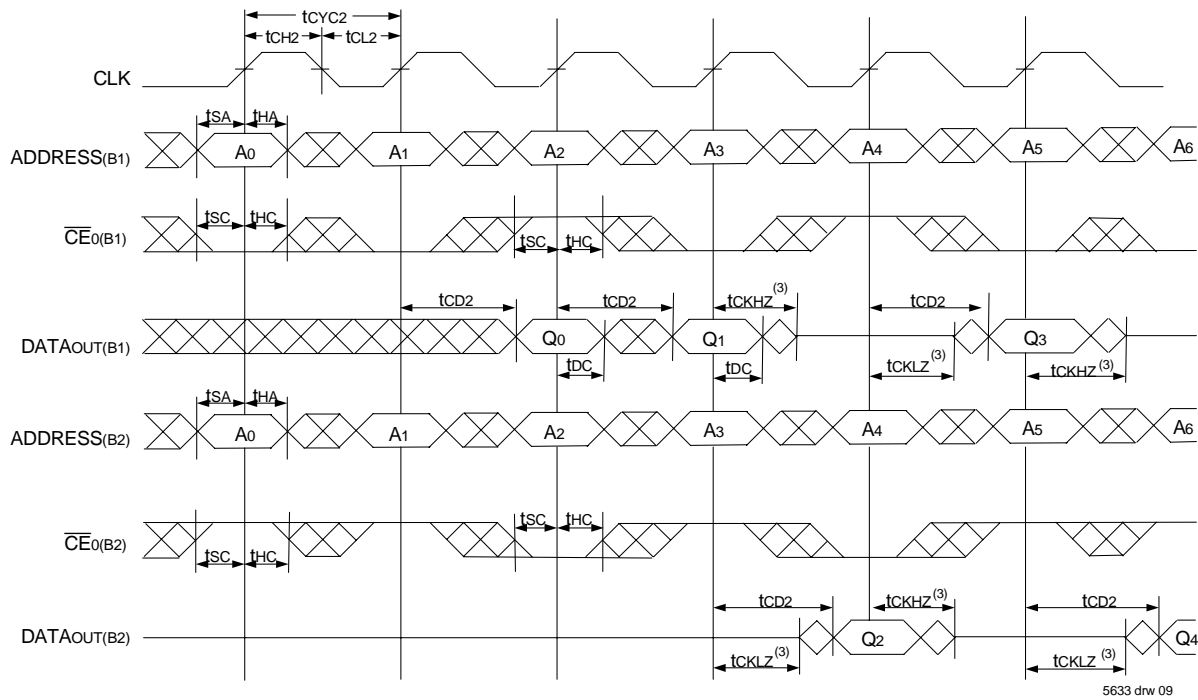


5633 drw 08

NOTES:

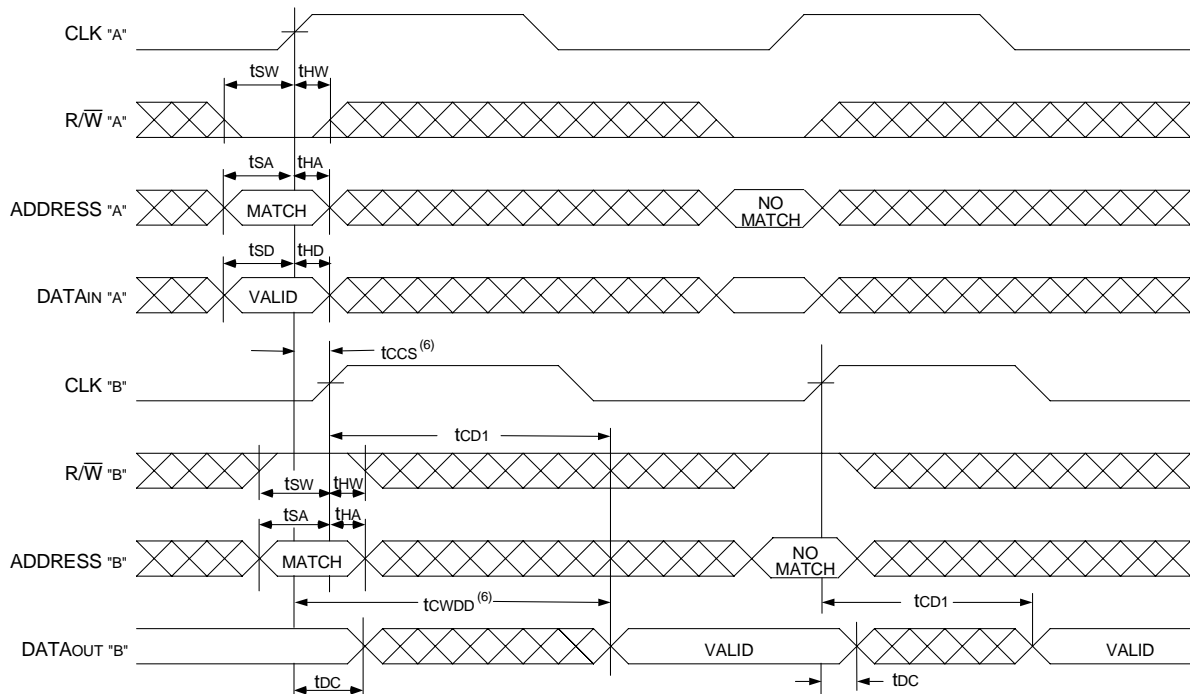
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. $\overline{\text{OE}}$ is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
3. $\overline{\text{ADS}} = \text{V}_{\text{IL}}$, $\overline{\text{CNTEN}}$ and $\overline{\text{CNTRST}} = \text{V}_{\text{IH}}$.
4. The output is disabled (High-Impedance state) by $\overline{\text{CE}}_0 = \text{V}_{\text{IH}}$, $\text{CE}_1 = \text{V}_{\text{IL}}$, following the next rising edge of the clock. Refer to Truth Table 1.
5. Addresses do not have to be accessed sequentially since $\overline{\text{ADS}} = \text{V}_{\text{IL}}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
6. If $\overline{\text{UB}}$ or $\overline{\text{LB}}$ was HIGH, then the Upper Byte and/or Lower Byte of DATAout for Qn + 2 would be disabled (High-Impedance state).
7. "X" here denotes Left or Right port. The diagram is with respect to that port.

Timing Waveform of a Bank Select Pipelined Read^(1,2)



5633 drw 09

Timing Waveform of Write with Port-to-Port Flow-Through Read^(4,5,7)

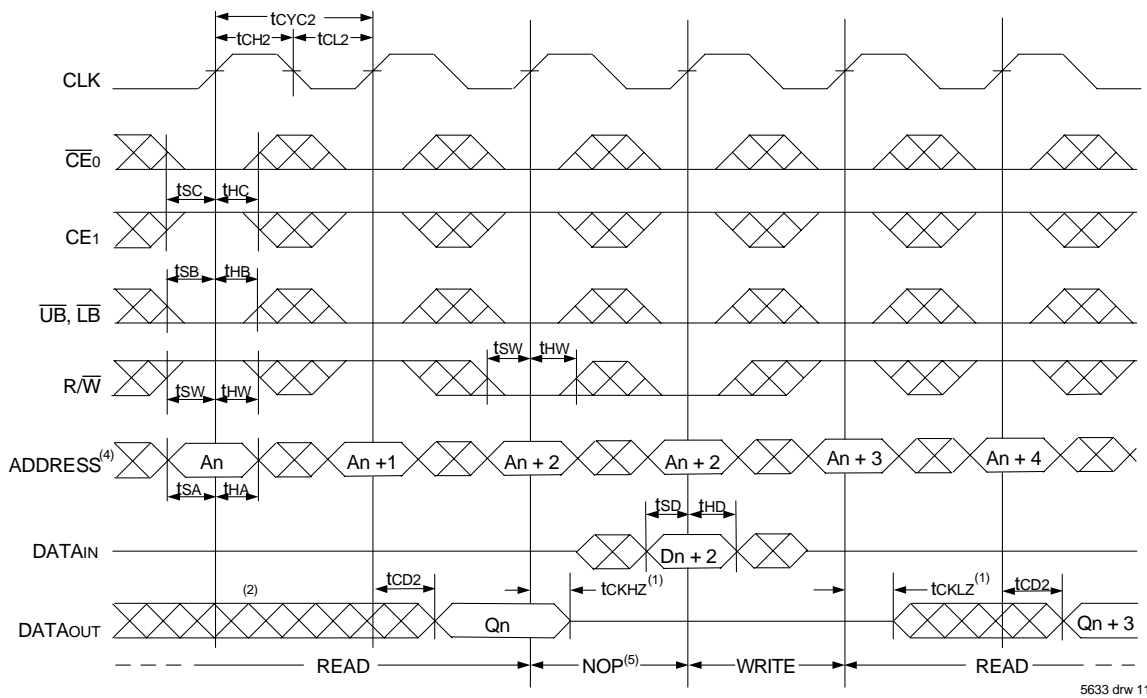


5633 drw 10

NOTES:

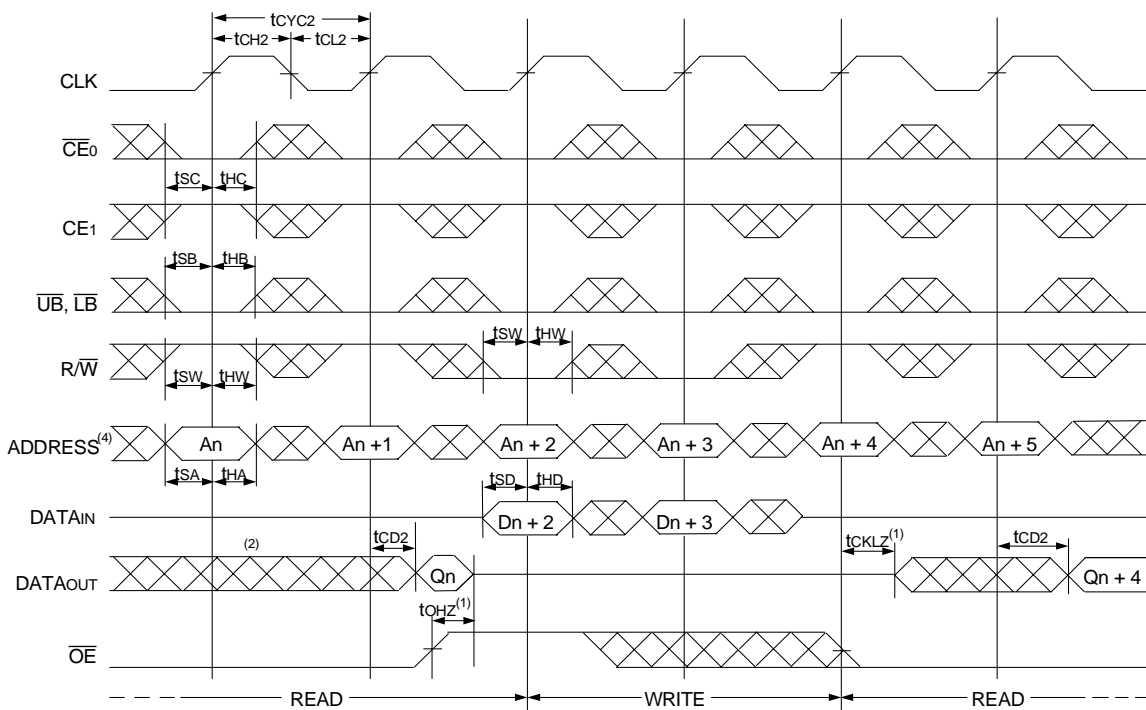
1. B1 Represents Bank #1; B2 Represents Bank #2. Each Bank consists of one IDT709359/49 for this waveform, and are setup for depth expansion in this example. ADDRESS(B1) = ADDRESS(B2) in this situation.
2. \overline{UB} , \overline{LB} , \overline{OE} , and $\overline{ADS} = V_{IL}$; $CE_{1(B1)}$, $CE_{1(B2)}$, R/\overline{W} , \overline{CNTEN} , and $\overline{CNRST} = V_{IH}$.
3. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
4. \overline{CE}_0 , \overline{UB} , \overline{LB} , and $\overline{ADS} = V_{IL}$; CE_1 , \overline{CNTEN} , and $\overline{CNRST} = V_{IH}$.
5. $\overline{OE} = V_{IL}$ for the Right Port, which is being read from. $\overline{OE} = V_{IH}$ for the Left Port, which is being written to.
6. If $t_{CCS} \leq$ maximum specified, then data from right port READ is not valid until the maximum specified for t_{CWDD} . If $t_{CCS} >$ maximum specified, then data from right port READ is not valid until $t_{CCS} + t_{CD1}$. t_{CWDD} does not apply in this case.
7. All timing is the same for both Left and Right ports. Port "A" may be either Left or Right port. Port "B" is the opposite from Port "A".

Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE} = V_{IL}$)⁽³⁾



5633 drw 11

Timing Waveform of Pipelined Read-to-Write-to-Read (\overline{OE} Controlled)⁽³⁾

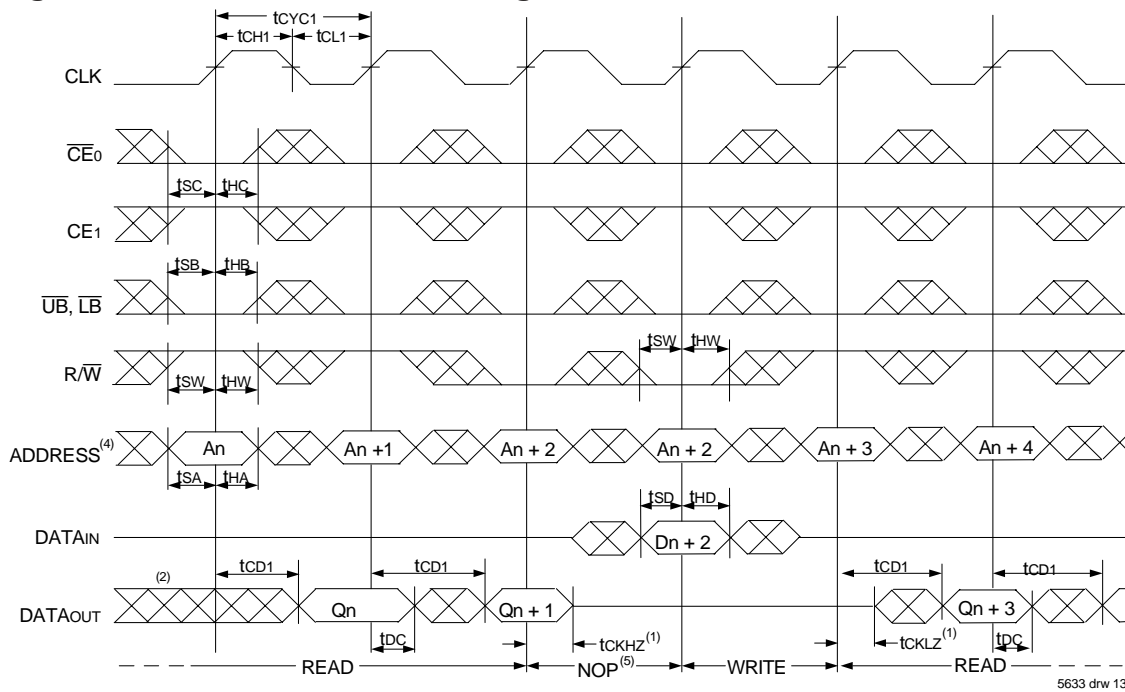


5633 drw 12

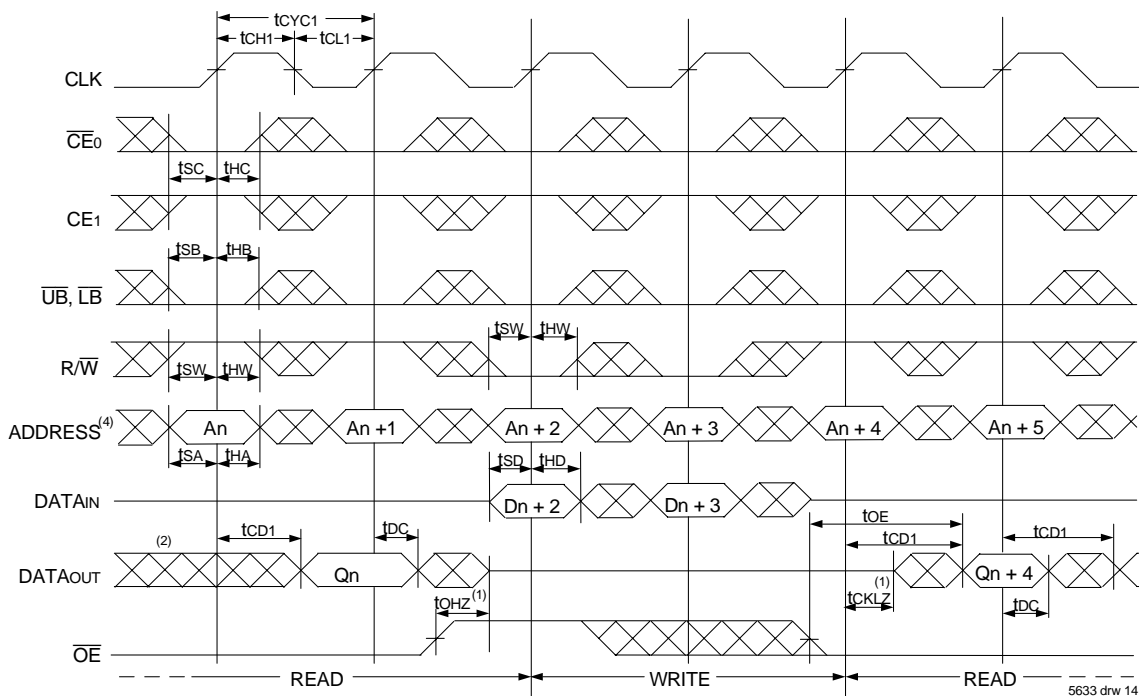
NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
3. \overline{CE}_0 , \overline{UB} , \overline{LB} , and $\overline{ADS} = V_{IL}$; CE_1 , \overline{CNTEN} , and $\overline{CNTRST} = V_{IH}$. "NOP" is "No Operation".
4. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

Timing Waveform of Flow-Through Read-to-Write-to-Read ($\overline{OE} = V_{IL}$)⁽³⁾



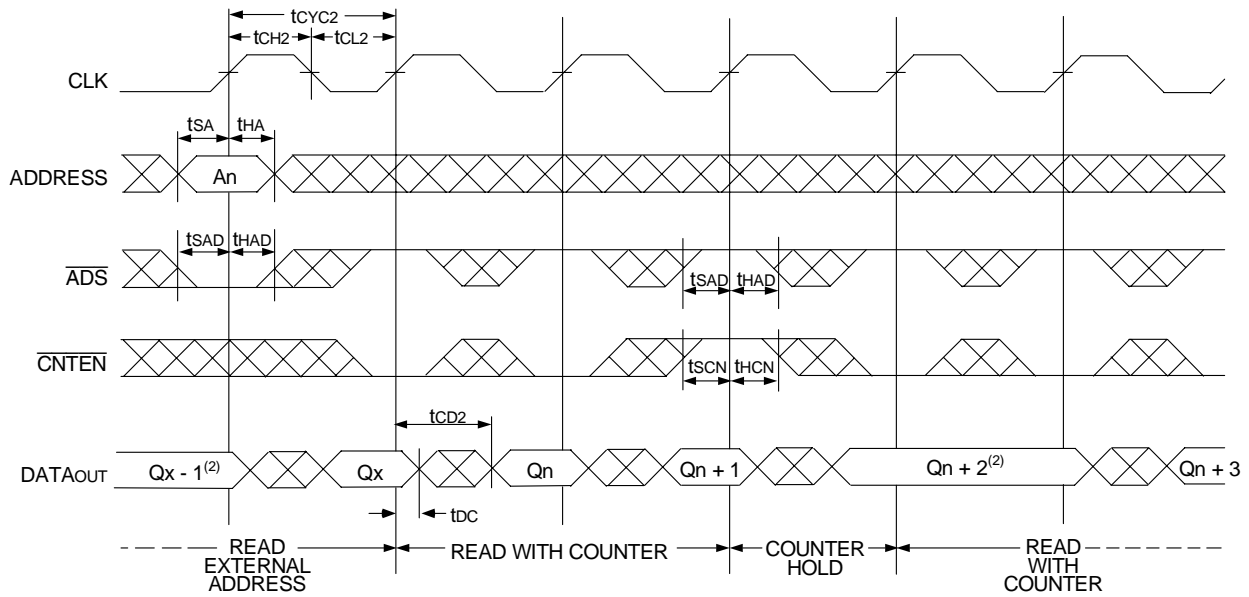
Timing Waveform of Flow-Through Read-to-Write-to-Read (\overline{OE} Controlled)⁽³⁾



NOTES:

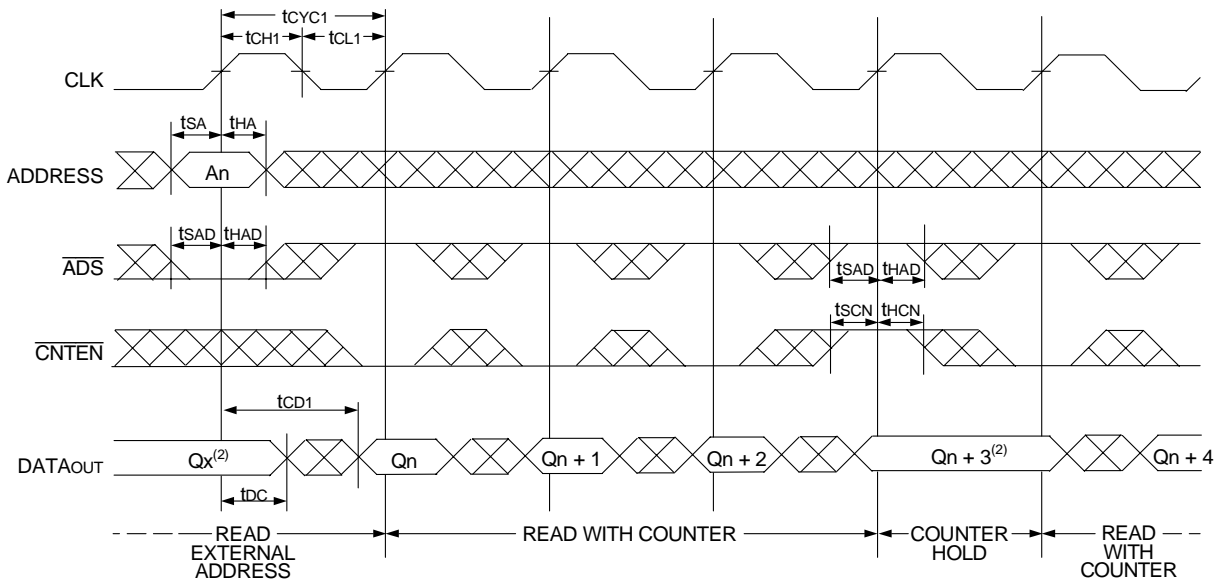
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or High-impedance) is determined by the previous cycle's control signals.
3. \overline{CE}_0 , \overline{UB} , \overline{LB} , and $\overline{ADS} = V_{IL}$; CE_1 , \overline{CNTEN} , and $\overline{CNRST} = V_{IH}$. "NOP" is "No Operation".
4. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

Timing Waveform of Pipelined Read with Address Counter Advance⁽¹⁾



5633 drw 15

Timing Waveform of Flow-Through Read with Address Counter Advance⁽¹⁾

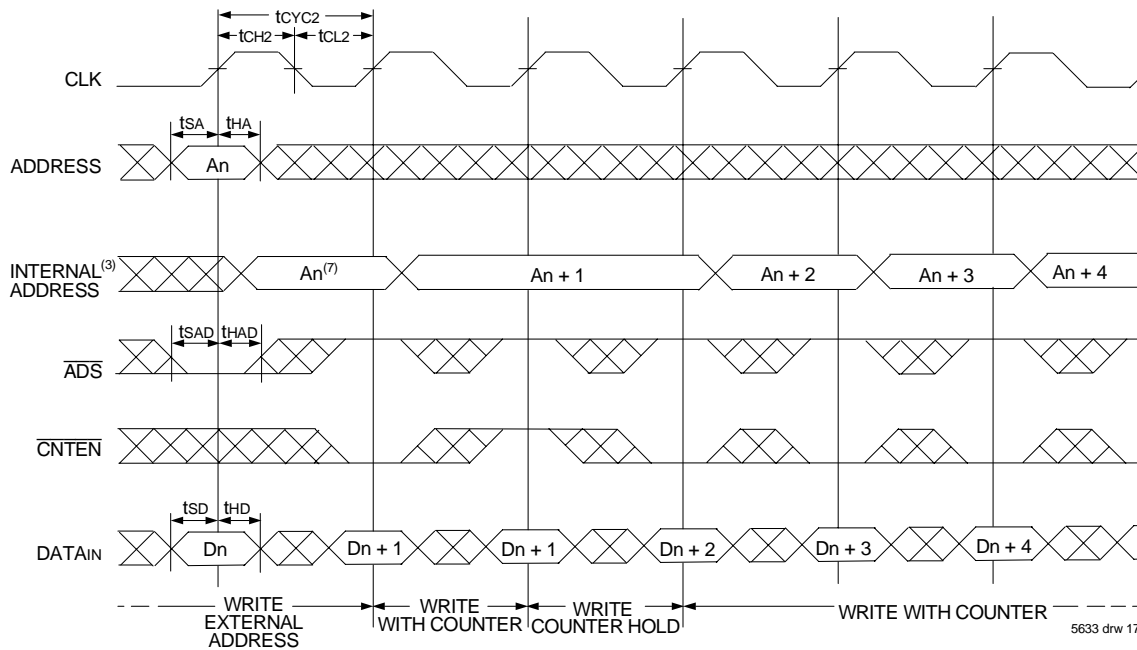


5633 drw 16

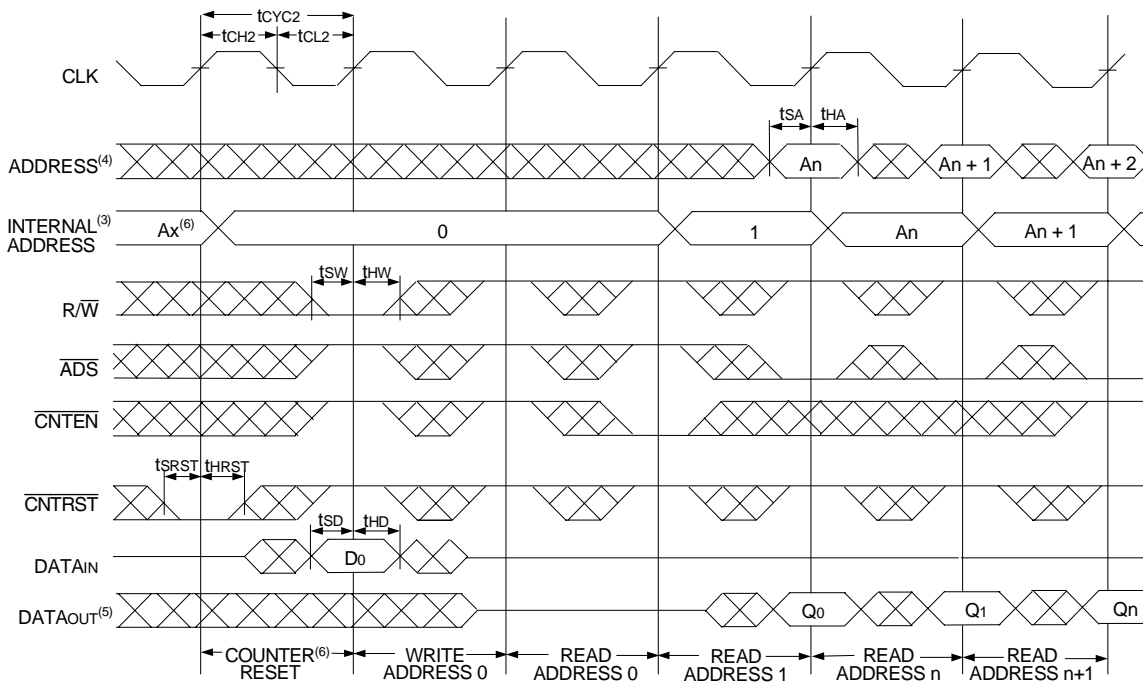
NOTES:

- \overline{CE}_0 , \overline{OE} , \overline{UB} , and $\overline{LB} = V_{IL}$; CE_1 , R/\overline{W} , and $\overline{CNTRST} = V_{IH}$.
- If there is no address change via $\overline{ADS} = V_{IL}$ (loading a new address) or $\overline{CNTEN} = V_{IL}$ (advancing the address), i.e. $\overline{ADS} = V_{IH}$ and $\overline{CNTEN} = V_{IH}$, then the data output remains constant for subsequent clocks.

Timing Waveform of Write with Address Counter Advance (Flow-Through or Pipelined Outputs)⁽¹⁾



Timing Waveform of Counter Reset (Pipelined Outputs)⁽²⁾



NOTES:

1. $\overline{CE}_0, \overline{UB}, \overline{LB}$ and $R/\overline{W} = V_{IL}$; CE_1 and $\overline{CNTRST} = V_{IH}$.
2. $\overline{CE}_0, \overline{UB}, \overline{LB} = V_{IL}$; $CE_1 = V_{IH}$.
3. The "Internal Address" is equal to the "External Address" when $\overline{ADS} = V_{IL}$ and equals the counter output when $\overline{ADS} = V_{IH}$.
4. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
6. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset cycle.
7. $\overline{CNTEN} = V_{IL}$ advances Internal Address from 'An' to 'An + 1'. The transition shown indicates the time required for the counter to advance. The 'An + 1' Address is written to during this cycle.

A Functional Description

The IDT709359/49 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse is independent of the LOW to HIGH transition of the clock signal.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the address counters for fast interleaved memory applications.

$\overline{CE}_0 = V_{IH}$ or $CE_1 = V_{IL}$ for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT709359/49's for depth expansion configurations. When the Pipelined output mode is enabled, two cycles are required with $\overline{CE}_0 = V_{IL}$ and $CE_1 = V_{IH}$ to re-activate the outputs.

Depth and Width Expansion

The IDT709359/49 features dual chip enables (refer to Truth Table 1) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT709359/49 can also be used in applications requiring expanded width, as indicated in Figure 4. Since the banks are allocated at the discretion of the user, the external controller can be set up to drive the input signals for the various devices as required to allow for 36-bit or wider applications.

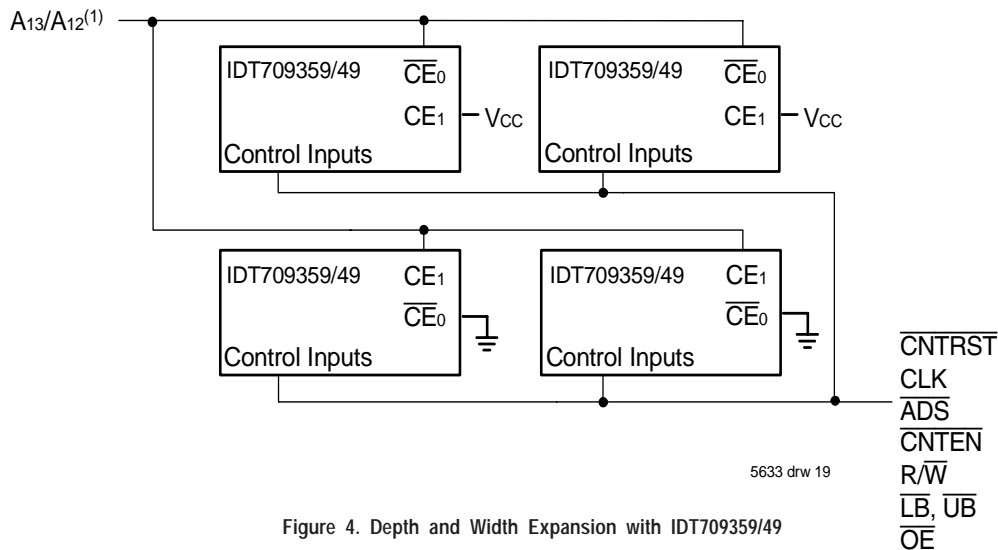
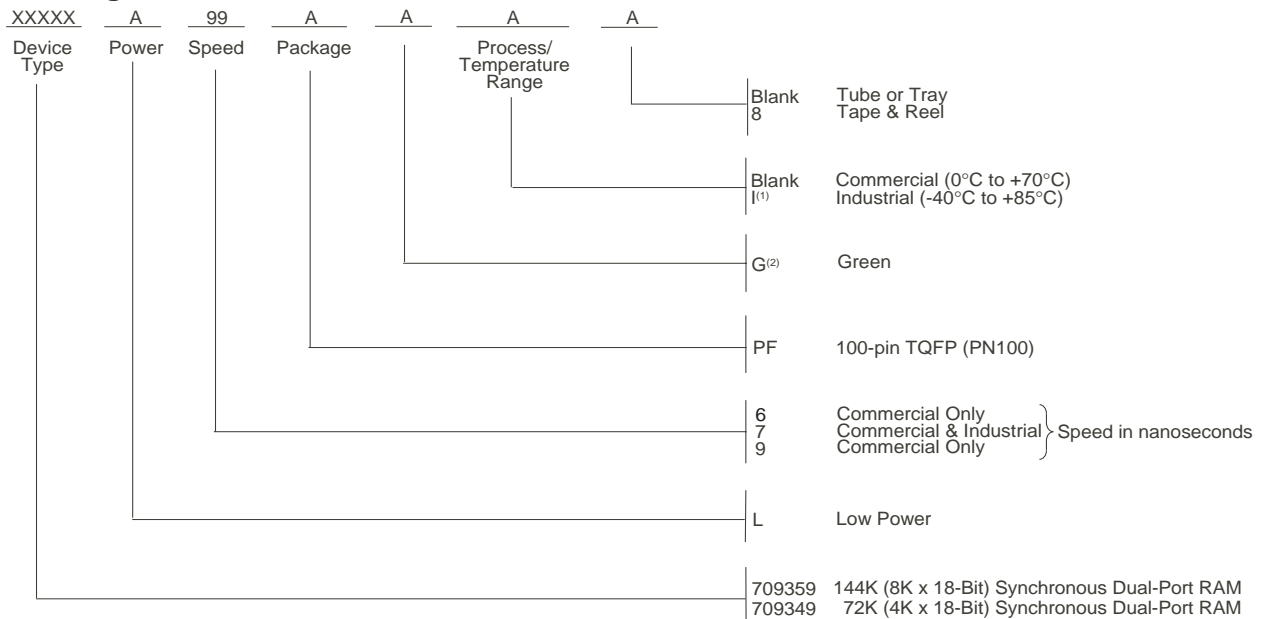


Figure 4. Depth and Width Expansion with IDT709359/49

NOTE:

1. A13 is for IDT709359, A12 is for IDT709349.

Ordering Information



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NOTES:

- Contact your local sales office for industrial temp range for other speeds, packages and powers.
- Green parts available. For specific speeds, packages and powers contact your sales office.

LEAD FINISH (SnPb) parts are in EOL process. Product Discontinuation Notice - PDN# SP-17-02

Datasheet Document History

07/08/02:	Initial Public Release
08/18/03:	Removed Preliminary status Page 16 Added IDT Clock Solution Table
10/21/08:	Page 16 Removed "IDT" from orderable part number
05/21/15:	Page 1 Added green availability to Features Page 1 Removed 100-pin fine pitch Ball Grid Array fpBGA offering from Features Page 2 Removed IDT in reference to fabrication Page 3 The package code PN100-1 changed to PN100 to match standard package codes Page 3 Removed the date for the PN100-pin TQFP configuration Page 4 Removed the 100-pin fine pitch Ball Grid Array fpBGA configuration and corresponding footnotes Page 5 Corrected typo in footnote text Page 7 Corrected typo in the Typical Output Derating drawing Page 8 Removed the commercial temp range from the AC Elec Chars Read & Write Cycle Timing table title Page 15 Added Tape & Reel and Green indicators with their footnote annotations to the Ordering Information Page 15 Removed the 100-pin TQFP fpBGA from the Ordering Information Page 15 Removed IDT Clock table
02/08/18:	Product Discontinuation Notice - PDN# SP-17-02 Last time buy expires June 15, 2018