

Features

- ◆ High-speed address/chip select time
 - Commercial: 20/25/35ns (max.)
 - Industrial: 20/25/35ns (max.)
 - Military: 25/35/45/55/70/85/100ns (max.)
- ◆ Low-power operation
- ◆ Battery Backup operation – 2V data retention
- ◆ Produced with advanced high-performance CMOS technology
- ◆ Input and output directly TTL-compatible
- ◆ Available in standard 28-pin (300 or 600 mil) ceramic DIP, 28-pin (300 mil) SOJ
- ◆ Military product compliant to MIL-STD-883, Class B
- ◆ Industrial temperature range (–40°C to +85°C) is available for selected speeds
- ◆ Green parts available, see ordering information

Description

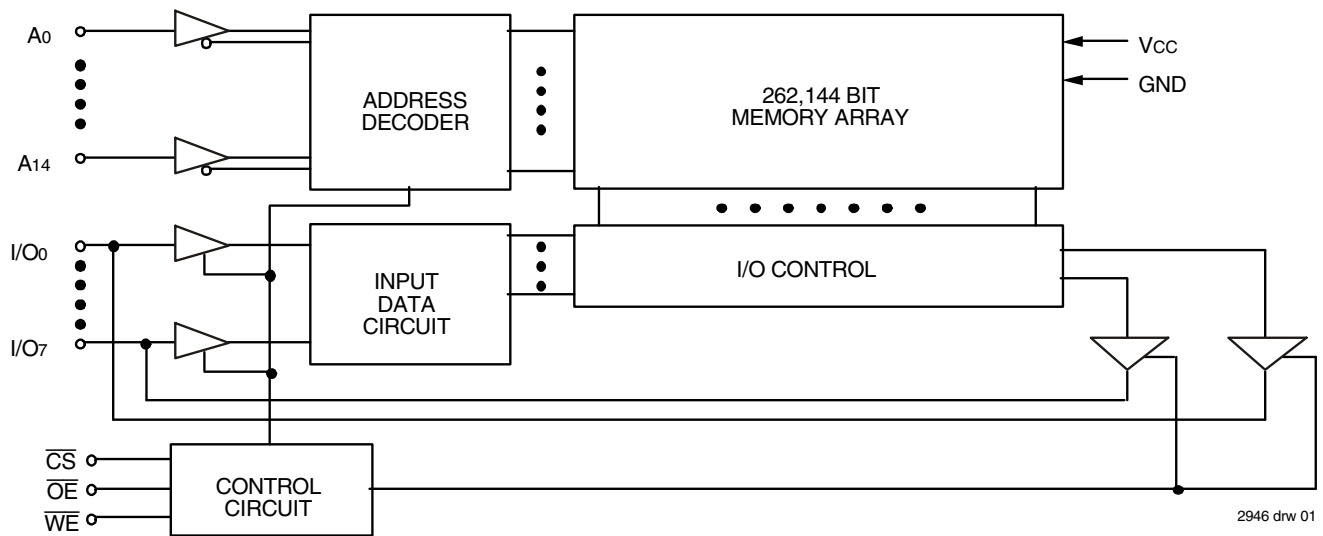
The IDT71256 is a 262,144-bit high-speed static RAM organized as 32K x 8. It is fabricated using high-performance, high-reliability CMOS technology.

Address access times as fast as 20ns are available with power consumption of only 350mW (typ.). The circuit also offers a reduced power standby mode. When \overline{CS} goes HIGH, the circuit will automatically go to and remain in, a low-power standby mode as long as \overline{CS} remains HIGH. This capability provides significant system level power and cooling savings. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 5µW when operating off a 2V battery.

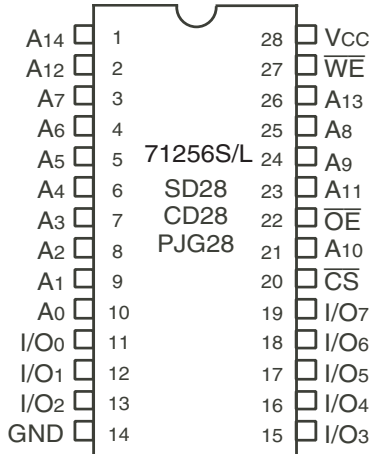
The IDT71256 is packaged in a 28-pin (300 or 600 mil) ceramic DIP, a 28-pin 300 mil SOJ providing high board level packing densities.

The IDT71256 military RAM is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

Functional Block Diagram



Pin Configurations⁽¹⁾



2946 drw 02

DIP/SOJ Top View

NOTE:

- This text does not indicate orientation of actual part-marking.

Pin Descriptions

| Name | Description |
|-------------------------------------|-------------------|
| A ₀ - A ₁₄ | Address Inputs |
| I/O ₀ - I/O ₇ | Data Input/Output |
| \overline{CS} | Chip Select |
| \overline{WE} | Write Enable |
| \overline{OE} | Output Enable |
| GND | Ground |
| V _{CC} | Power |

2946 tbl 01

Truth Table⁽¹⁾

| \overline{WE} | \overline{CS} | \overline{OE} | I/O | Function |
|-----------------|-----------------|-----------------|--------|-----------------|
| X | H | X | High-Z | Standby (ISB) |
| X | V _{HC} | X | High-Z | Standby (ISB1) |
| H | L | H | High-Z | Output Disabled |
| H | L | L | DOUT | Read Data |
| L | L | X | DIN | Write Data |

2946 tbl 02

NOTE:

- H = V_{IH}, L = V_{IL}, X = Don't care.

Absolute Maximum Ratings⁽¹⁾

| Symbol | Rating | Com'l. | Ind. | Mil. | Unit |
|-------------------|--------------------------------------|--------------|--------------|--------------|------|
| V _{TERM} | Terminal Voltage with Respect to GND | -0.5 to +7.0 | -0.5 to +7.0 | -0.5 to +7.0 | V |
| T _A | Operating Temperature | 0 to +70 | -40 to +85 | -55 to +125 | °C |
| T _{BIAS} | Temperature Under Bias | -55 to +125 | -55 to +125 | -65 to +135 | °C |
| T _{STG} | Storage Temperature | -55 to +125 | -55 to +125 | -65 to +150 | °C |
| P _T | Power Dissipation | 1.0 | 1.0 | 1.0 | W |
| I _{OUT} | DC Output Current | 50 | 50 | 50 | mA |

2946 tbl 03

NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Capacitance (T_A = +25°C, f = 1.0MHz)

| Symbol | Parameter ⁽¹⁾ | Conditions | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 11 | pF |
| C _{I/O} | I/O Capacitance | V _{OUT} = 0V | 11 | pF |

2946 tbl 04

NOTE:

- This parameter is determined by device characterization, but is not production tested.

Recommended Operating Temperature and Supply Voltage

| Grade | Temperature | GND | Vcc |
|------------|-----------------|-----|----------|
| Military | -55°C to +125°C | 0V | 5V ± 10% |
| Industrial | -40°C to +85°C | 0V | 5V ± 10% |
| Commercial | 0°C to +70°C | 0V | 5V ± 10% |

2946 tbl 05

Recommended DC Operating Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|-----------------|--------------------|---------------------|------|------|------|
| Vcc | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| GND | Ground | 0 | 0 | 0 | V |
| V _{IH} | Input High Voltage | 2.2 | — | 6.0 | V |
| V _{IL} | Input Low Voltage | -0.5 ⁽¹⁾ | — | 0.8 | V |

2946 tbl 06

NOTE:

- V_{IL} (min.) = -3.0V for pulse width less than 20ns, once per cycle.

DC Electrical Characteristics^(1,2) (Vcc = 5.0V ± 10%, V_{Lc} = 0.2V, V_{Hc} = Vcc - 0.2V)

| Symbol | Parameter | Power | 71256S/L20 | 71256S/L25 | 71256S/L35 | 71256S/L45 | Unit | | |
|--------|--|-------|--------------|--------------|------------|--------------|------|------|------|
| | | | Com'l. & Ind | Com'l. & Ind | Mil. | Com'l. & Ind | | Mil. | Mil. |
| ICC | Dynamic Operating Current CS ≤ V _{IL} , Outputs Open Vcc = Max., f _{MAX} ⁽²⁾ | S | — | — | 150 | — | 140 | 135 | mA |
| | | L | 135 | 125 | 130 | 115 | 120 | 115 | |
| ISB | Standby Power Supply Current (TTL Level), CS ≥ V _{IH} , Vcc = Max., Outputs Open, f = f _{MAX} ⁽²⁾ | S | — | — | 20 | — | 20 | 20 | mA |
| | | L | 3 | 3 | 3 | 3 | 3 | 3 | |
| ISB1 | Full Standby Power Supply Current (CMOS Level), CS ≥ V _{Hc} , Vcc = Max., f = 0 | S | — | — | 20 | — | 20 | 20 | mA |
| | | L | 0.6 | 0.6 | 1.5 | 0.6 | 1.5 | 1.5 | |

2946 tbl 07

| Symbol | Parameter | Power | 71256S/L55 | 71256S/L70 | 71256S/L85 | 71256S/L100 | Unit |
|--------|--|-------|------------|------------|------------|-------------|------|
| | | | Mil. | Mil. | Mil. | Mil. | |
| ICC | Dynamic Operating Current CS ≤ V _{IL} , Outputs Open Vcc = Max., f _{MAX} ⁽²⁾ | S | 135 | 135 | 135 | 135 | mA |
| | | L | 115 | 115 | 115 | 115 | |
| ISB | Standby Power Supply Current (TTL Level), CS ≥ V _{IH} , Vcc = Max., Outputs Open, f = f _{MAX} ⁽²⁾ | S | 20 | 20 | 20 | 20 | mA |
| | | L | 3 | 3 | 3 | 3 | |
| ISB1 | Full Standby Power Supply Current (CMOS Level), CS ≥ V _{Hc} , Vcc = Max., f = 0 | S | 20 | 20 | 20 | 20 | mA |
| | | L | 1.5 | 1.5 | 1.5 | 1.5 | |

2946 tbl 08

NOTES:

- All values are maximum guaranteed values.
- f_{MAX} = 1/TRC, all address inputs are cycling at f_{MAX}; f = 0 means no address pins are cycling.

AC Test Conditions

| | |
|-------------------------------|---------------------|
| Input Pulse Levels | GND to 3.0V |
| Input Rise/Fall Times | 5ns |
| Input Timing Reference Levels | 1.5V |
| Output Reference Levels | 1.5V |
| AC Test Load | See Figures 1 and 2 |

2946 tbl 09

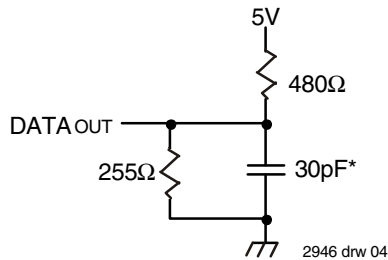


Figure 1. AC Test Load

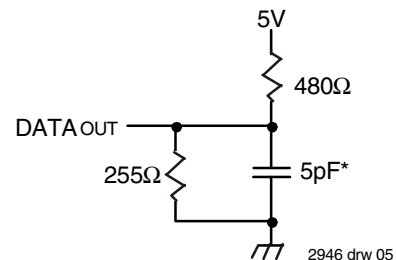


Figure 2. AC Test Load
(for tCLZ, tOLZ, tCHZ, tOHZ, tOW, and tWHZ)

*Includes scope and jig capacitances

DC Electrical Characteristics (V_{CC} = 5.0V ± 10%)

| Symbol | Parameter | Test Conditions | IDT71256S | | | IDT71256L | | | Unit | |
|-----------------|------------------------|---|----------------------|------|------|-----------|------|------|--------|----|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| I _{LI} | Input Leakage Current | V _{CC} = Max., V _{IN} = GND to V _{CC} | MIL. COM"L & IND. | — | — | 10 5 | — | — | 5 2 | μA |
| I _{LO} | Output Leakage Current | V _{CC} = Max., \overline{CS} = V _H , V _{OUT} = GND to V _{CC} | MIL. COM"L & IND. | — | — | 10 5 | — | — | 5 2 | μA |
| V _{OL} | Output Low Voltage | I _{OL} = 8mA, V _{CC} = Min. | — | — | 0.4 | — | — | 0.4 | V | |
| | | I _{OL} = 10mA, V _{CC} = Min. | — | — | 0.5 | — | — | 0.5 | | |
| V _{OH} | Output High Voltage | I _{OH} = -4mA, V _{CC} = Min. | 2.4 | — | — | 2.4 | — | — | V | |

2946 tbl 10

Data Retention Characteristics Over All Temperature Ranges (L Version Only) (V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

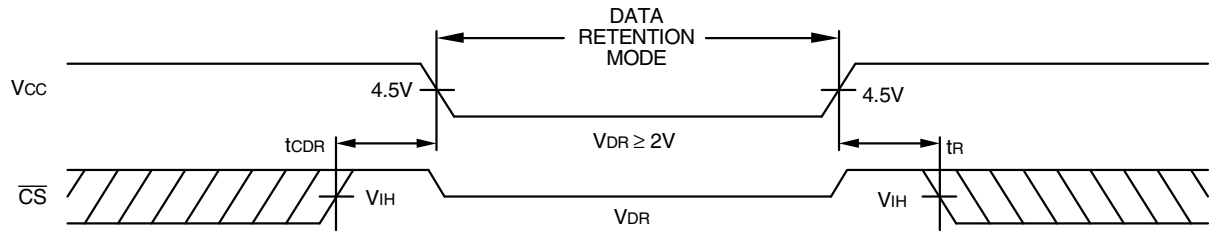
| Symbol | Parameter | Test Condition | Min. | Typ. ⁽¹⁾ V _{CC} @ | | Max. V _{CC} @ | | Unit |
|-------------------------------|--------------------------------------|-----------------------------|--------------------------------|--|------|---------------------------|------------|------|
| | | | | 2.0V | 3.0V | 2.0V | 3.0V | |
| V _{DR} | V _{CC} for Data Retention | — | 2.0 | — | — | — | — | V |
| I _{CDR} | Data Retention Current | MIL. COM"L & IND. | — | — | — | 500 120 | 800 200 | μA |
| t _{CDR} | Chip Deselect to Data Retention Time | $\overline{CS} \geq V_{HC}$ | 0 | — | — | — | — | ns |
| t _R ⁽²⁾ | Operation Recovery Time | | t _{RC} ⁽²⁾ | — | — | — | — | ns |

2946 tbl 11

NOTES:

1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by device characterization, but is not production tested.

Low Vcc Data Retention Waveform



2946 drw 06

AC Electrical Characteristics (Vcc = 5.0V ± 10%, All Temperature Ranges)

| Symbol | Parameter | 71256L20 ⁽¹⁾ | | 71256S25 71256L25 | | 71256S35 71256L35 | | 71256S45 ⁽³⁾ 71256L45 ⁽³⁾ | | Unit |
|---------------------------------|------------------------------------|-------------------------|------|----------------------|------|----------------------|------|--|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Read Cycle | | | | | | | | | | |
| t _{RC} | Read Cycle Time | 20 | — | 25 | — | 35 | — | 45 | — | ns |
| t _{AA} | Address Access Time | — | 20 | — | 25 | — | 35 | — | 45 | ns |
| t _{ACS} | Chip Select Access Time | — | 20 | — | 25 | — | 35 | — | 45 | ns |
| t _{OLZ} ⁽²⁾ | Chip Select to Output in Low-Z | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| t _{CHZ} ⁽²⁾ | Chip Deselect to Output in High-Z | — | 10 | — | 11 | — | 15 | — | 20 | ns |
| t _{OE} | Output Enable to Output Valid | — | 10 | — | 11 | — | 15 | — | 20 | ns |
| t _{OLZ} ⁽²⁾ | Output Enable to Output in Low-Z | 2 | — | 2 | — | 2 | — | 0 | — | ns |
| t _{OHZ} ⁽²⁾ | Output Disable to Output in High-Z | 2 | 8 | 2 | 10 | 2 | 15 | — | 20 | ns |
| t _{OH} | Output Hold from Address Change | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| Write Cycle | | | | | | | | | | |
| t _{WC} | Write Cycle Time | 20 | — | 25 | — | 35 | — | 45 | — | ns |
| t _{CW} | Chip Select to End-of-Write | 15 | — | 20 | — | 30 | — | 40 | — | ns |
| t _{AW} | Address Valid to End-of-Write | 15 | — | 20 | — | 30 | — | 40 | — | ns |
| t _{AS} | Address Set-up Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{WP} | Write Pulse Width | 15 | — | 20 | — | 30 | — | 35 | — | ns |
| t _{WR} | Write Recovery Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{DW} | Data to Write Time Overlap | 11 | — | 13 | — | 15 | — | 20 | — | ns |
| t _{WHZ} ⁽²⁾ | Write Enable to Output in High-Z | — | 10 | — | 11 | — | 15 | — | 20 | ns |
| t _{DH} | Data Hold from Write Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{OW} ⁽²⁾ | Output Active from End-of-Write | 5 | — | 5 | — | 5 | — | 5 | — | ns |

2946 tbl 12

NOTES:

- 0° to +70°C or -40° to +85°C temperature range only.
- This parameter is guaranteed by device characterization, but is not production tested.
- 55°C to +125°C temperature range only.

AC Electrical Characteristics (V_{CC} = 5.0V ± 10%, Military Temperature Ranges)

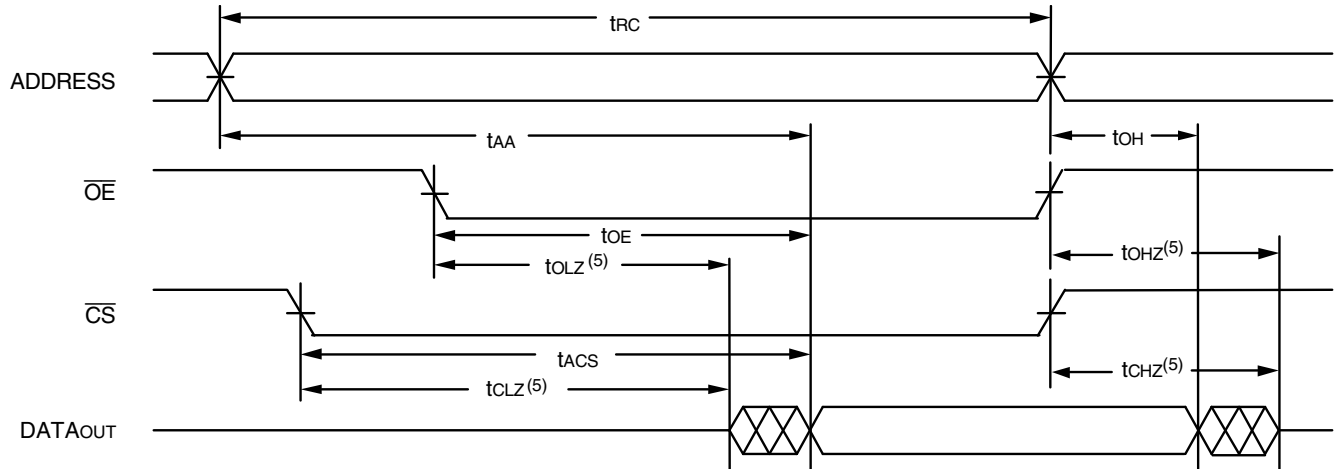
| Symbol | Parameter | 71256S55 ⁽¹⁾ 71256L55 ⁽¹⁾ | | 71256S70 ⁽¹⁾ 71256L70 ⁽¹⁾ | | 71256S85 ⁽¹⁾ 71256L85 ⁽¹⁾ | | 71256S100 ⁽¹⁾ 71256L100 ⁽¹⁾ | | Unit |
|---------------------------------|---|--|------|--|------|--|------|--|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Read Cycle | | | | | | | | | | |
| t _{RC} | Read Cycle Time | 55 | — | 70 | — | 85 | — | 100 | — | ns |
| t _{AA} | Address Access Time | — | 55 | — | 70 | — | 85 | — | 100 | ns |
| t _{ACS} | Chip Select Access Time | — | 55 | — | 70 | — | 85 | — | 100 | ns |
| t _{OLZ} ⁽²⁾ | Chip Select to Output in Low-Z | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| t _{CHZ} ⁽²⁾ | Chip Deselect to Output in High-Z | — | 25 | — | 30 | — | 35 | — | 40 | ns |
| t _{OE} | Output Enable to Output Valid | — | 25 | — | 30 | — | 35 | — | 40 | ns |
| t _{OLZ} ⁽²⁾ | Output Enable to Output in Low-Z | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{OHZ} ⁽²⁾ | Output Disable to Output in High-Z | 0 | 25 | 0 | 30 | — | 35 | — | 40 | ns |
| t _{OH} | Output Hold from Address Change | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| Write Cycle | | | | | | | | | | |
| t _{WC} | Write Cycle Time | 55 | — | 70 | — | 85 | — | 100 | — | ns |
| t _{CW} | Chip Select to End-of-Write | 50 | — | 60 | — | 70 | — | 80 | — | ns |
| t _{AW} | Address Valid to End-of-Write | 50 | — | 60 | — | 70 | — | 80 | — | ns |
| t _{AS} | Address Set-up Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{WP} | Write Pulse Width | 40 | — | 45 | — | 50 | — | 55 | — | ns |
| t _{WR} | Write Recovery Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{DW} | Data to Write Time Overlap | 25 | — | 30 | — | 35 | — | 40 | — | ns |
| t _{WHZ} ⁽²⁾ | Write Enable to Output in High-Z | — | 25 | — | 30 | — | 35 | — | 40 | ns |
| t _{DH} | Data Hold from Write Time (\overline{WE}) | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{OW} ⁽²⁾ | Output Active from End-of-Write | 5 | — | 5 | — | 5 | — | 5 | — | ns |

2946 tbl 13

NOTES:

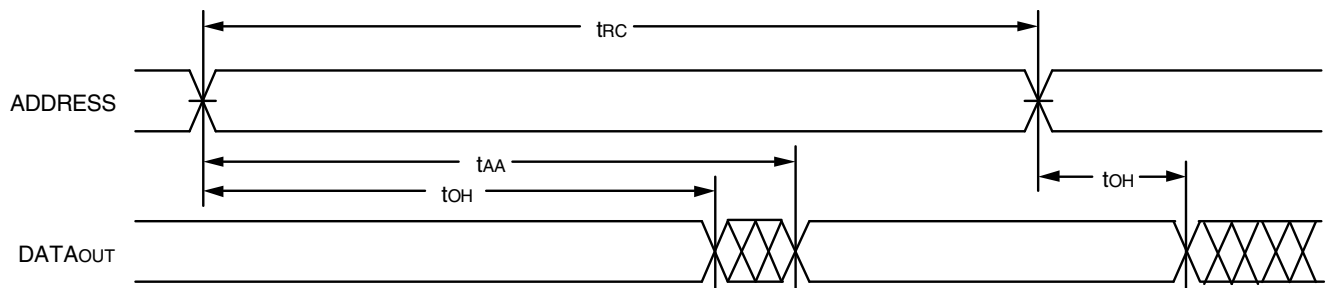
- 55° to +125°C temperature range only.
- This parameter is guaranteed by device characterization, but is not production tested.

Timing Waveform of Read Cycle No. 1⁽¹⁾



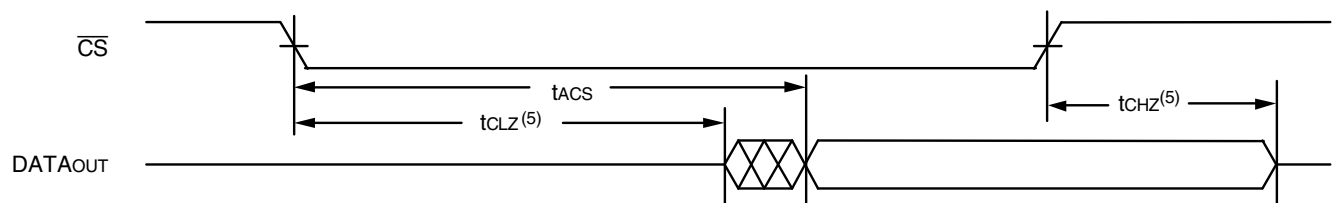
2946 drw 07

Timing Waveform of Read Cycle No. 2^(1,2,4)



2946 drw 08

Timing Waveform of Read Cycle No. 2^(1,3,4)

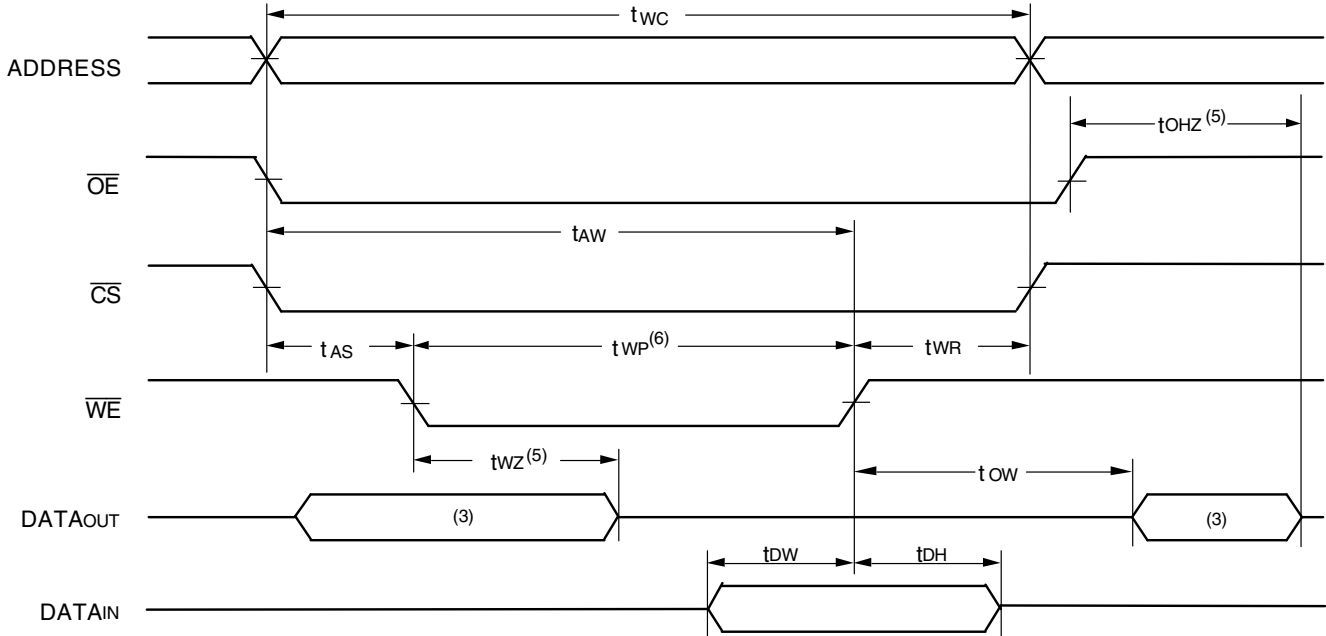


2946 drw 09

NOTES:

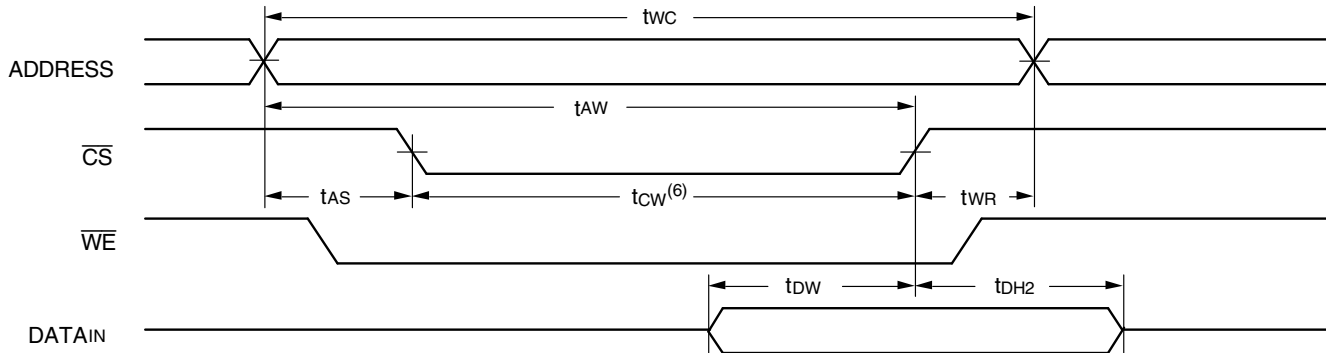
1. \overline{WE} is HIGH for Read Cycle.
2. Device is continuously selected, \overline{CS} is LOW.
3. Address valid prior to or coincident with \overline{CS} transition LOW.
4. \overline{OE} is LOW.
5. Transition is measured $\pm 200\text{mV}$ from steady state.

Timing Waveform of Write Cycle No. 1 (\overline{WE} Controlled Timing)^(1,2,4,6)



2946 drw 10

Timing Waveform of Write Cycle No. 2 (\overline{CS} Controlled Timing)^(1,2,4)

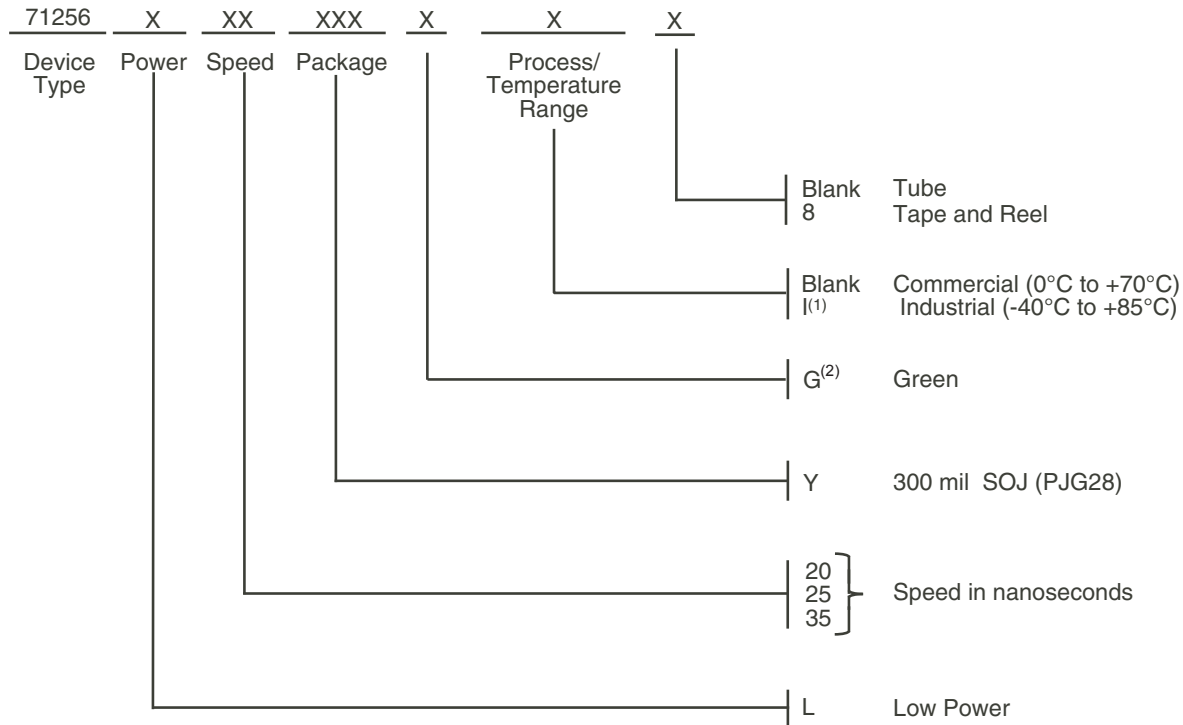


2946 drw 11

NOTES:

1. A write occurs during the overlap of a LOW \overline{CS} and a LOW \overline{WE} .
2. t_{WR} is measured from the earlier of \overline{CS} or \overline{WE} going HIGH to the end of the write cycle.
3. During this period, I/O pins are in the output state so that the input signals must not be applied.
4. If the \overline{CS} LOW transition occurs simultaneously with or after the \overline{WE} LOW transition, the outputs remain in a high-impedance state.
5. Transition is measured $\pm 200\text{mV}$ from steady state.
6. If \overline{OE} is LOW during a \overline{WE} controlled write cycle, the write pulse width must be the larger of t_{WP} or $(t_{WHZ} + t_{DW})$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW} . If \overline{OE} is HIGH during a \overline{WE} controlled write cycle, this requirement does not apply and the minimum write pulse width can be as short as the specified t_{WP} . For a \overline{CS} controlled write cycle, \overline{OE} may be LOW with no degradation to t_{CW} .

Ordering Information — Commercial & Industrial

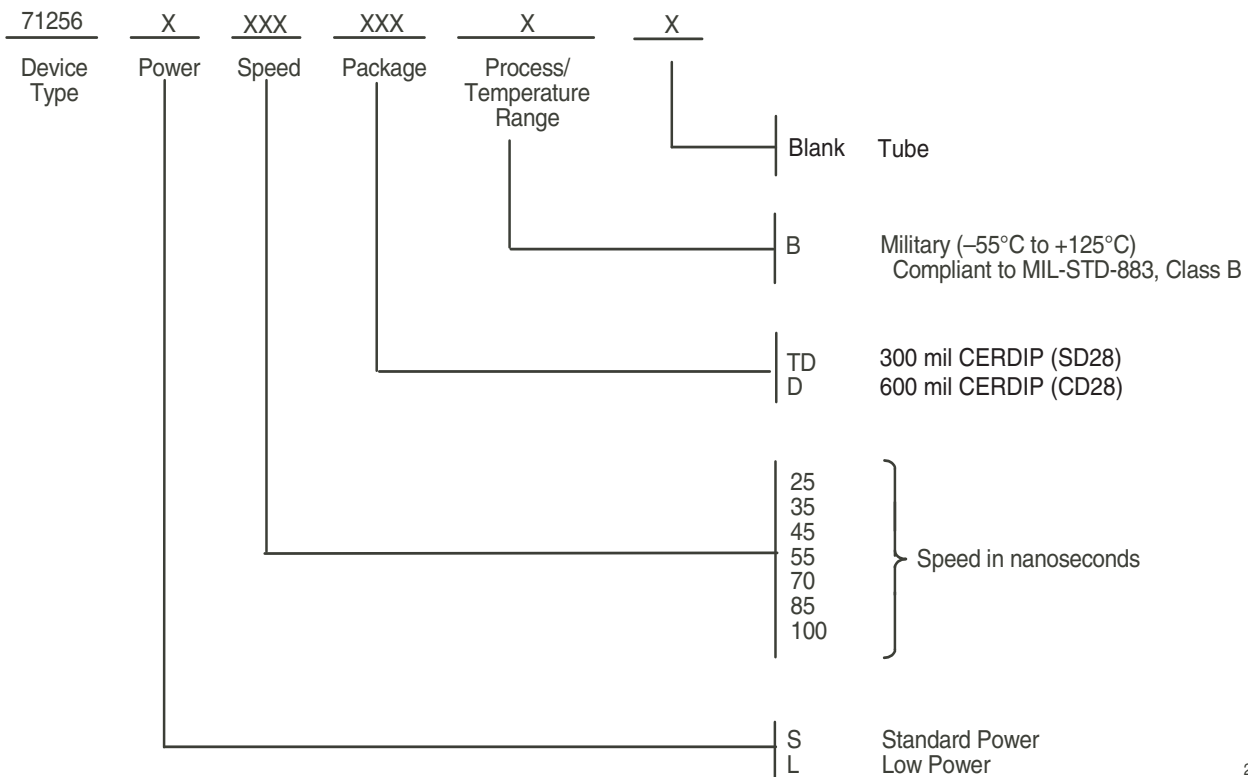


2946 drw 13

NOTES:

1. Contact your local sales office for Industrial temp range for other speeds, packages and powers.
2. Green parts available. For specific speeds, packages and powers contact your local sales office.

Ordering Information — Military



2946 drw 12

Orderable Part Information

| Speed (ns) | Orderable Part ID | Pkg. Code | Pkg. Type | Temp. Grade |
|------------|-------------------|-----------|-----------|-------------|
| 20 | 71256L20YG | PJG28 | SOJ | C |
| | 71256L20YG8 | PJG28 | SOJ | C |
| | 71256L20YGI | PJG28 | SOJ | I |
| | 71256L20YGI8 | PJG28 | SOJ | I |
| 25 | 71256L25DB | CD28 | CDIP | M |
| | 71256L25TDB | SD28 | CDIP | M |
| | 71256L25YG | PJG28 | SOJ | C |
| | 71256L25YG8 | PJG28 | SOJ | C |
| | 71256L25YGI | PJG28 | SOJ | I |
| | 71256L25YGI8 | PJG28 | SOJ | I |
| 35 | 71256L35DB | CD28 | CDIP | M |
| | 71256L35TDB | SD28 | CDIP | M |
| | 71256L35YG | PJG28 | SOJ | C |
| | 71256L35YG8 | PJG28 | SOJ | C |
| | 71256L35YGI | PJG28 | SOJ | I |
| | 71256L35YGI8 | PJG28 | SOJ | I |
| 45 | 71256L45DB | CD28 | CDIP | M |
| | 71256L45TDB | SD28 | CDIP | M |
| 55 | 71256L55DB | CD28 | CDIP | M |
| | 71256L55TDB | SD28 | CDIP | M |
| 70 | 71256L70DB | CD28 | CDIP | M |
| | 71256L70TDB | SD28 | CDIP | M |
| 85 | 71256L85DB | CD28 | CDIP | M |
| | 71256L85TDB | SD28 | CDIP | M |
| 100 | 71256L100DB | CD28 | CDIP | M |
| | 71256L100TDB | SD28 | CDIP | M |

| Speed (ns) | Orderable Part ID | Pkg. Code | Pkg. Type | Temp. Grade |
|------------|-------------------|-----------|-----------|-------------|
| 25 | 71256S25DB | CD28 | CDIP | M |
| | 71256S25TDB | SD28 | CDIP | M |
| 35 | 71256S35DB | CD28 | CDIP | M |
| | 71256S35TDB | SD28 | CDIP | M |
| 45 | 71256S45DB | CD28 | CDIP | M |
| | 71256S45TDB | SD28 | CDIP | M |
| 55 | 71256S55DB | CD28 | CDIP | M |
| | 71256S55TDB | SD28 | CDIP | M |
| 70 | 71256S70DB | CD28 | CDIP | M |
| | 71256S70TDB | SD28 | CDIP | M |
| 85 | 71256S85DB | CD28 | CDIP | M |
| | 71256S85TDB | SD28 | CDIP | M |
| 100 | 71256S100DB | CD28 | CDIP | M |
| | 71256S100TDB | SD28 | CDIP | M |

Datasheet Document History

| | | |
|-----------|----------------|--|
| 11/4/99: | | Updated to new format |
| | Pg. 1–5, 9 | Added Industrial Temperature Range offerings |
| | Pg. 1 | Removed 30, 120, and 150ns military and 45ns commercial speed grade offerings. |
| | Pg. 2 | Removed P28-2 package from DIP/SOJ Top View |
| | Pg. 3 | Removed 30ns and 45ns (Commercial only) speed grade offerings from DC Electrical table |
| | | Revised notes and footnotes |
| | Pg. 5 | Removed 30ns speed grade offering from AC Electrical table |
| | | Revised notes and footnotes |
| | Pg. 6 | Expressed Military Temperature range on AC Electrical table |
| | | Revised notes and footnotes |
| | Pg. 8 | Removed Note 1 and renumbered notes and footnotes |
| | Pg. 9 | Revised Ordering Information and presented by temperature range offering |
| | Pg. 10 | Added Datasheet Document History |
| 08/09/00: | | Not recommended for new designs |
| 02/01/01: | | Remove "Not recommended for new designs" |
| 11/15/06: | Pg. 3 | Changed power limits for commercial and industrial. Refer to PCNSR-0602-03. Added Restricted hazardous substance device to ordering information. |
| 11/01/08: | Pg. 2,9 | Corrected typo on pin 21 in 32-Pin LCC diagram. Updated the ordering information by removing the "IDT" notation. |
| 04/28/11: | Pg. 1, 2, 5, 9 | Added 20ns to Industrial offering. Obsoleted 28-pin 600 mil, 32-pin LCC and Added Tape and Reel to Ordering information and updated description of Restricted hazardous substance device to Green. |
| 09/26/13: | Pg. 1 | In the Description: removed IDT's reference to fabrication and removed the sentence "In the full standby mode, the low-power device consumes less than 15 μ W, typically". |
| 08/06/20: | Pg. 1 - 12 | Rebranded as Renesas datasheet |
| | Pg.1 & 9 | Updated Industrial temp and green availability |
| | Pg. 2 & 9 | Updated package codes |
| | Pg. 10 | Added Orderable Part Information tables |

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