3.3V CMOS 1-TO-5 CLOCK DRIVER

IDT74FCT38075

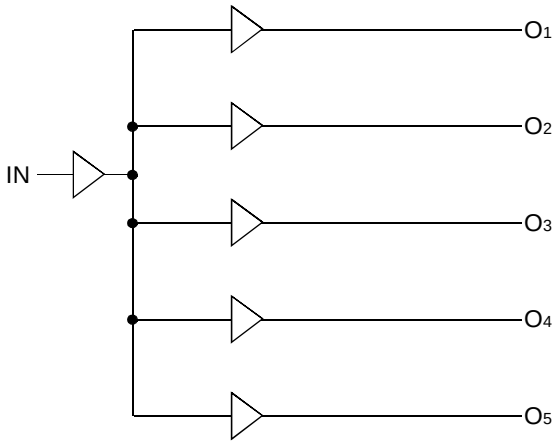
FEATURES:

- Advanced CMOS Technology
- Guaranteed low skew < 100ps (max.)
- Very low duty cycle distortion< 250ps (max.)
- High speed propagation delay< 3ns (max.)
- Very low CMOS power levels
- TTL compatible inputs and outputs
- 1:5 fanout
- Maximum output rise and fall time < 1.5ns (max.)
- Low input capacitance: 3pF typical
- V_{CC} = 3.3V ± 0.3V
- Inputs can be driven from 3.3V or 5V components
- Operating frequency up to 166MHz
- Available in SOIC package

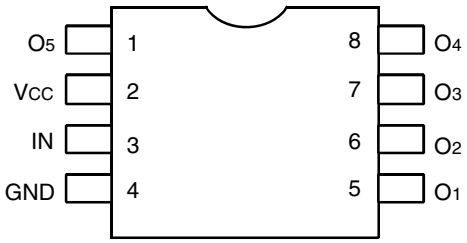
DESCRIPTION:

The FCT38075 is a 3.3V clock driver built using advanced CMOS technology. This low skew clock driver offers 1:5 fanout. The large fanout from a single input reduces loading on the preceding driver and provides an efficient clock distribution network. Multiple power and grounds reduce noise. Typical applications are clock and signal distribution.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SOIC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{CC}	Input Power Supply Voltage	–0.5 to +4.6	V
V_I	Input Voltage	–0.5 to +5.5	V
V_O	Output Voltage	–0.5 to V_{CC}+0.5	V
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	–65 to +165	°C

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3	4	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	—	6	pF

NOTE:
1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
IN	Input
Ox	Outputs

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = GND or V_{CC}	—	0.1	30	µA
ΔI_{CC}	Power Supply Current per Input HIGH	V_{CC} = Max.	V_{IN} = V_{CC} - 0.6V	—	45	300	µA
I_{CCD}	Dynamic Power Supply Current per Output(3)	V_{CC} = Max. C_L = 15pF All Outputs Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	80	120	µA/MHz
I_C	Total Power Supply Current(4)	V_{CC} = Max. C_L = 15pF All Outputs Toggling fi = 133MHz	V_{IN} = V_{CC} V_{IN} = GND		90	120	mA
			V_{IN} = V_{CC} –0.6V V_{IN} = GND		90	120	
		V_{CC} = Max. C_L = 15pF All Outputs Toggling fi = 166MHz	V_{IN} = V_{CC} V_{IN} = GND	—	120	150	
			V_{IN} = V_{CC} –0.6V V_{IN} = GND	—	120	150	

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = V_{CC} -0.6V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_i = Input Frequency

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified
Industrial: T_A = -40°C to +85°C, V_{CC} = 3.3V ± 0.3V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level			2	—	5.5	V
V_{IL}	Input LOW Level			–0.5	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = 5.5V	—	—	±1	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_I = GND	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3,4]		–45	–75	–180	mA
I_{ODL}	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3,4]		50	92	200	mA
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3,4]		–60	–135	–240	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –12mA	2.4[5]	3	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –100µA	V_{CC} - 0.2	—	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 12mA	—	0.3	0.5	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100µA	—	—	0.2	

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3, 25°C ambient.
3. This parameter is guaranteed but not tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
5. V_{OH} = V_{CC} - 0.6V at rated current.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE [3,4]

Symbol	Parameter	Conditions[1,8]	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay	C_L = 15pF f ≤166MHz	0.5	3	ns
t_R	Output Rise Time (0.8V to 2V)		—	1.5	ns
t_F	Output Fall Time (2V to 0.8V)		—	1.5	ns
$t_{SK(O)}$	Same device output pin-to-pin skew[5]		—	100	ps
$t_{SK(P)}$	Pulse skew[6]		—	250	ps
$t_{SK(PP)}$	Part to part skew[7]		—	550	ps
f_{MAX}	Input Frequency		—	166	MHz

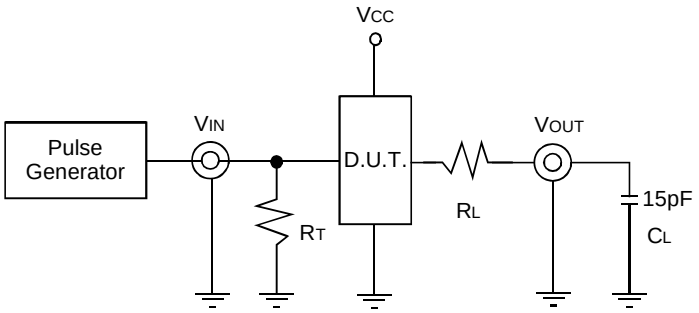
NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. t_{PLH}, t_{PHL}, $t_{SK(P)}$, and $t_{SK(O)}$ are production tested. All other parameters guaranteed but not production tested.
4. Propagation delay range indicated by Min. and Max. limit is due to V_{CC}, operating temperature and process parameters. These propagation delay limits do not imply skew.
5. Skew measured between all outputs under identical transitions and load conditions.
6. Skew measured is difference between propagation delay times t_{PHL} and t_{PLH} of same output under identical load conditions.
7. Part to part skew for all outputs given identical transitions and load conditions at identical V_{CC} levels and temperature.
8. Airflow of 1m/s is recommended for frequencies above 133MHz.

TEST CIRCUITS

TEST CONDITIONS

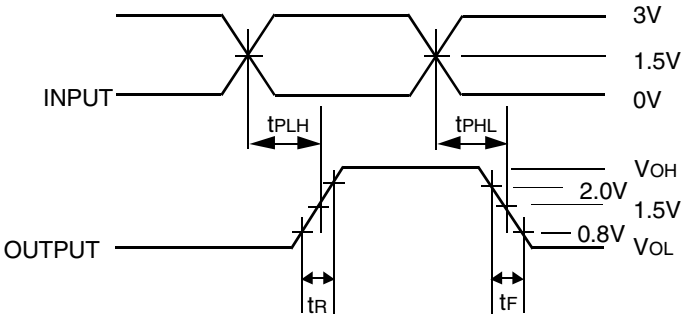
Symbol	V_{CC} = 3.3V ±0.3V	Unit
C_L	15	pF
R_L	33	Ω
R_T	Z_{OUT} of pulse generator	Ω
t_R / t_F	1 (0V to 3V or 3V to 0V)	ns

DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.
t_R / t_F = Rise/Fall time of the input stimulus from the Pulse Generator.

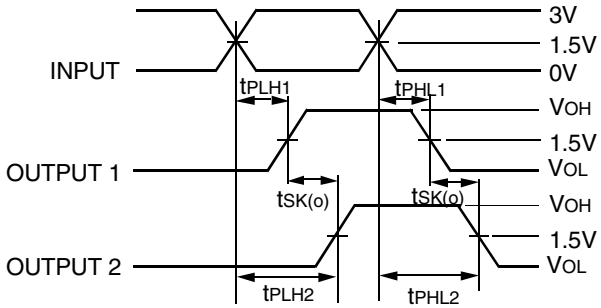


C_L = 15pF Circuit

TEST WAVEFORMS

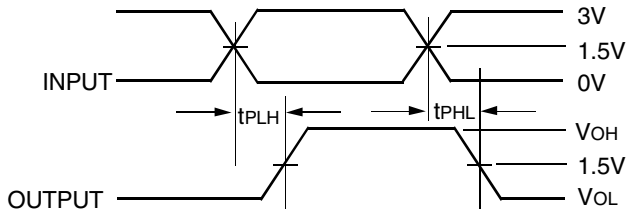


Propagation Delay



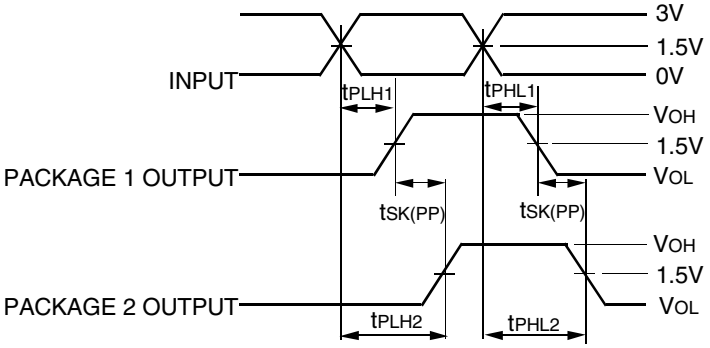
$t_{SK(o)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

Output Skew - $t_{SK(O)}$



$t_{SK(p)} = |t_{PHL} - t_{PLH}|$

Pulse Skew - $t_{SK(P)}$

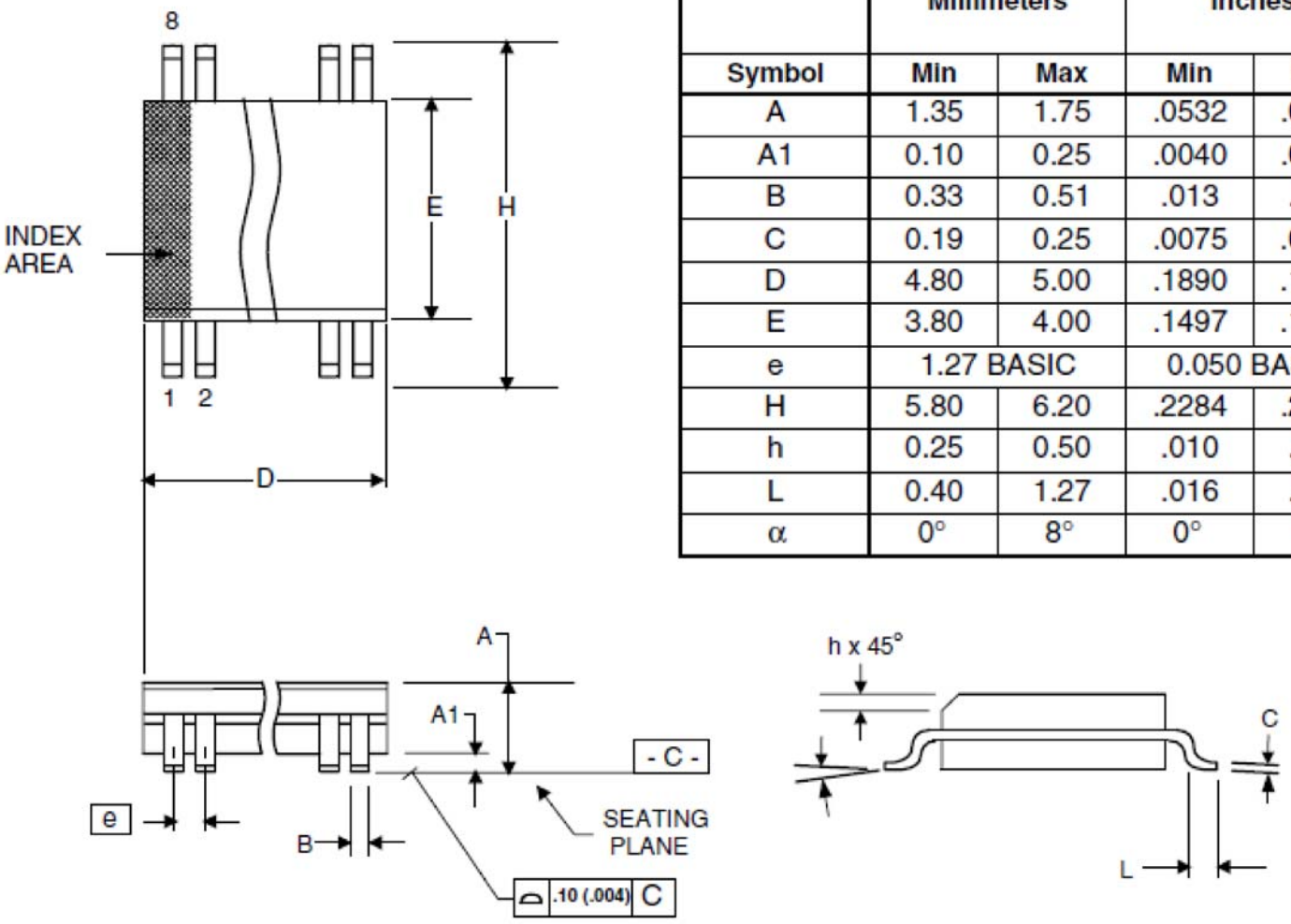


$t_{SK(PP)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

Part-to-Part Skew - $t_{SK(PP)}$

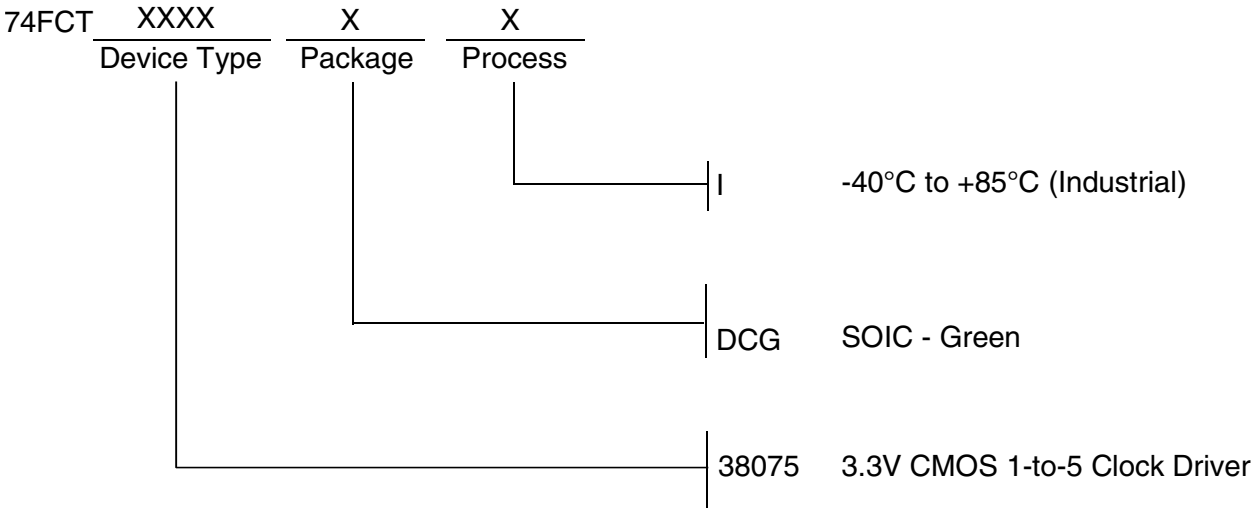
Part-to-Part Skew is for the same package and speed grade.

PACKAGE OUTLINE AND DIMENSIONS (8-PIN SOIC)



	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

ORDERING INFORMATION



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