13-BIT TO 26-BIT REGISTERED BUFFER WITH SSTL I/O

IDT74SSTVF16859

FEATURES:

- 1:2 register buffer
- Meets or exceeds JEDEC standard SSTVF16859
- 2.3V to 2.7V Operation for PC1600, PC2100, and PC2700
- 2.5V to 2.7V Operation for PC3200
- SSTL_2 Class I style data inputs/outputs
- Differential CLK input
- **RESET** control compatible with LVCMOS levels
- Latch-up performance exceeds 100mA
- ESD >2000V per MIL-STD-883, Method 3015; >200V using machine model (C = 200pF, R = 0)
- Available in 56 pin VFQFPN and 64 pin TSSOP packages

APPLICATIONS:

- Along with CSPT857C, Zero Delay PLL Clock buffer, provides complete solution for DDR1 DIMMs

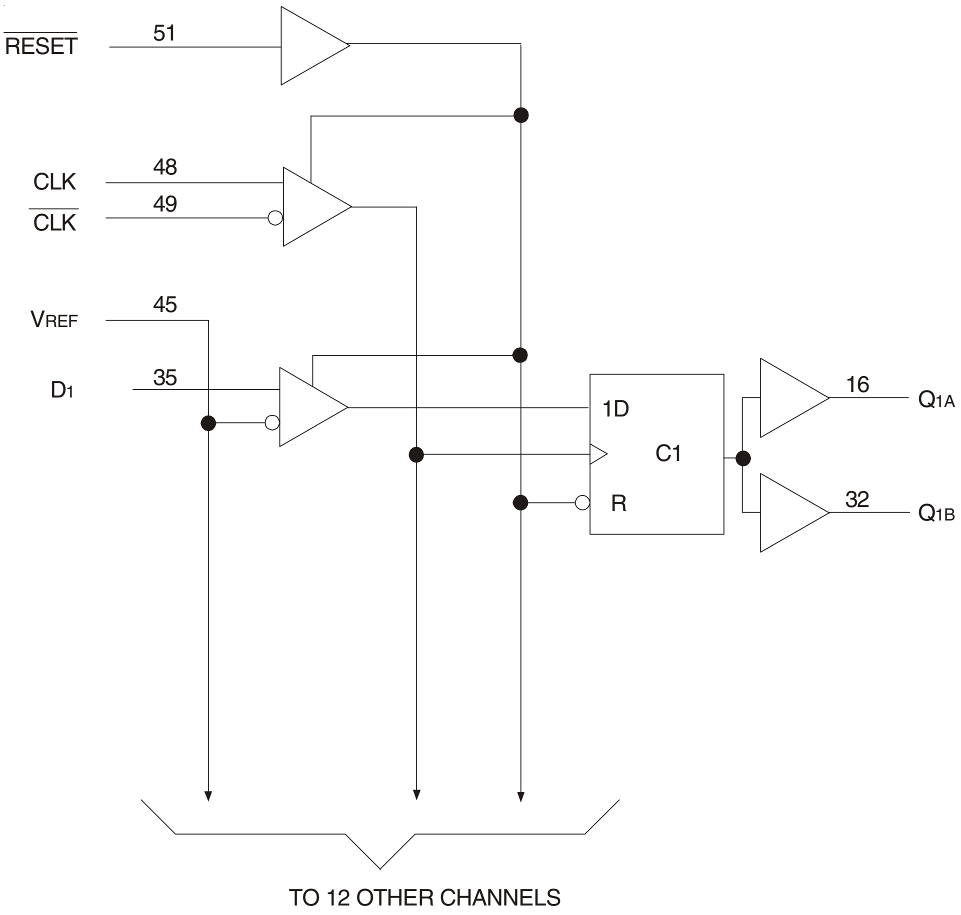
DESCRIPTION:

The SSTVF16859 is a 13-bit to 26-bit registered buffer designed for 2.3V-2.7V V_{DD} for PC1600 - PC2700 and 2.5V-2.7V V_{DD} for PC3200, and supports low standby operation. All data inputs and outputs are SSTL_2 level compatible with JEDEC standard for SSTL_2.

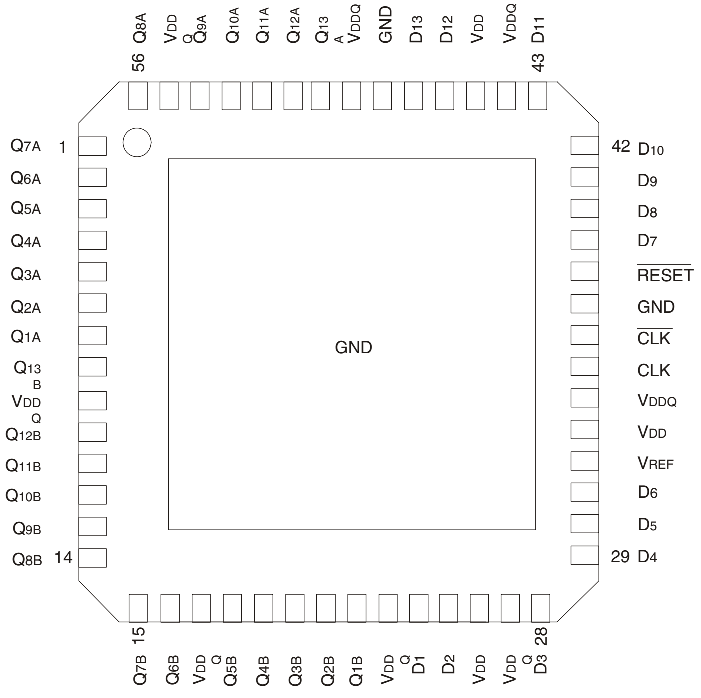
RESET is an LVCMOS input since it must operate predictably during the power-up phase. RESET, which can be operated independent of CLK and CLK, must be held in the low state during power-up in order to ensure predictable outputs (low state) before a stable clock has been applied.

RESET, when in the low state, will disable all input receivers, reset all registers, and force all outputs to a low state, before a stable clock has been applied. With inputs held low and a stable clock applied, outputs will remain low during the Low-to-High transition of RESET.

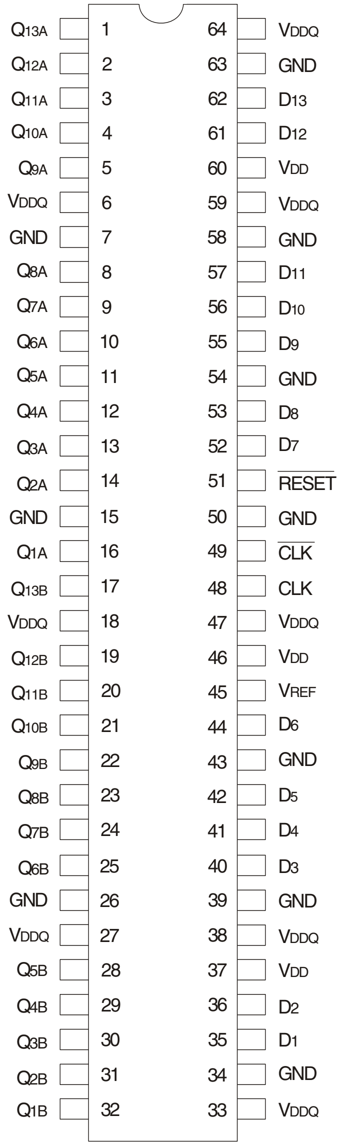
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



VFQFPN
TOP VIEW



TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
V_{DD} or V_{DDQ}	Supply Voltage Range	–0.5 to 3.6	V
V_I(2)	Input Voltage Range	–0.5 to V_{DD} +0.5	V
V_O(3)	Output Voltage Range	–0.5 to V_{DDQ} +0.5	V
I_{IK}	Input Clamp Current, $V_I < 0$	–50	mA
I_{OK}	Output Clamp Current, $V_O < 0$ or $V_O > V_{DDQ}$	±50	mA
I_O	Continuous Output Current, $V_O = 0$ to V_{DDQ}	±50	mA
V_{DD}	Continuous Current through each V_{DD}, V_{DDQ} or GND	±100	mA
T_{STG}	Storage Temperature Range	–65 to +150	°C

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. The input and output negative voltage ratings may be exceeded if the ratings of the I/P and O/P clamp current are observed.
3. The output current will flow if the following conditions are observed:
   a) Output in HIGH state
   b) $V_O = V_{DDQ}$

FUNCTION TABLE (1)

Input				Q Outputs
$\overline{\text{RESET}}$	CLK	$\overline{\text{CLK}}$	D	
H	↑	↓	L	L
H	↑	↓	H	H
H	L or H	L or H	X	Q_O(2)
L	X	X	X	L

NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW to HIGH
   ↓ = HIGH to LOW
2. Q_O = Output level before the indicated steady-state conditions were established.

PIN DESCRIPTION

Pin Names	Description
Q_1 - Q_{13}	Data Output
GND	Ground
V_{DDQ}	Output-stage drain power voltage
V_{DD}	Logic power voltage
$\overline{RESET}$	Asynchronous reset input - resets registers and disables data and clock differential input recievers
V_{REF}	Input reference voltage
CLK	Positive master clock input
$\overline{CLK}$	Negative master clock input
D_1 - D_{13}	Data Input - clocked in on the crossing of the rising edge of CLK and the falling edge of $\overline{CLK}$
Center PAD	Ground (MLF package only)

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE FOR PC1600 - PC2700

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, V_{DD} = 2.5V ±0.2V, V_{DDQ} = 2.5V ±0.2V

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IK}	Control Inputs	V_{DD} = 2.3V, I_I= –18mA	—	—	–1.2	V
V_{OH}		V_{DD} = 2.3V to 2.7V, I_{OH} = -100µA	V_{DD} – 0.2	—	—	V
		V_{DD} = 2.3V, I_{OH} = -8mA	1.95	—	—	
V_{OL}		V_{DD} = 2.3V to 2.7V, I_{OL} = 100µA	—	—	0.2	V
		V_{DD} = 2.3V, I_{OL} = 8mA	—	—	0.35	
I_I	All Inputs	V_{DD} = 2.7V,VI = V_{DD} or GND	—	—	±5	µA
I_{DD}	Static Standby	I_O = 0, V_{DD} = 2.7V, $\overline{RESET}$ = GND	—	—	0.01	mA
	Static Operating	I_O = 0, V_{DD} = 2.7V, $\overline{RESET}$ = V_{DD}, V_I = $V_{IH\ (AC)}$ or $V_{IL\ (AC)}$	—	—	20	
I_{DDD}	Dynamic Operating (Clock Only)	I_O = 0, V_{DD} = 2.7V, $\overline{RESET}$ = V_{DD}, V_I = $V_{IH\ (AC)}$ or $V_{IL\ (AC)}$, CLK and $\overline{CLK}$ Switching 50% Duty Cycle.	—	6	—	µA/Clock MHz
	Dynamic Operating (Per Each Data Input)(1)	I_O = 0, V_{DD} = 2.7V, $\overline{RESET}$ = V_{DD}, V_I = $V_{IH\ (AC)}$ or $V_{IL\ (AC)}$, CLK and $\overline{CLK}$ Switching 50% Duty Cycle. One Data Input Switching at Half Clock Frequency, 50% Duty Cycle.	—	43	—	µA/Clock MHz/Data Input
C_I	Data Inputs	V_{DD} = 2.5V, V_I = V_{REF} ± 310mV	2	—	3	pF
	CLK and $\overline{CLK}$	V_{ICR} = 1.25V, $V_{I\ (PP)}$ = 360mV	2	—	3	
	$\overline{RESET}$	V_I = V_{DD} or GND	2	—	3	

NOTE:
1. Power dissipation levels will allow operation at DDR333 speeds without excessive die temperature.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE FOR PC3200

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, V_{DD} = 2.6V ±0.1V, V_{DDQ} = 2.6V ±0.1V

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IK}	Control Inputs	V_{DD} = 2.5V, I_I = –18mA	—	—	–1.2	V
V_{OH}		V_{DD} = 2.5V to 2.7V, I_{OH} = -100µA	V_{DD} – 0.2	—	—	V
		V_{DD} = 2.5V, I_{OH} = -8mA	1.95	—	—	
V_{OL}		V_{DD} = 2.5V to 2.7V, I_{OL} = 100µA	—	—	0.2	V
		V_{DD} = 2.5V, I_{OL} = 8mA	—	—	0.35	
I_I	All Inputs	V_{DD} = 2.7V, VI = V_{DD} or GND	—	—	±5	µA
I_{DD}	Static Standby	I_O = 0, V_{DD} = 2.7V, $\overline{\text{RESET}}$ = GND	—	—	0.01	mA
	Static Operating	I_O = 0, V_{DD} = 2.7V, $\overline{\text{RESET}}$ = V_{DD}, V_I = $V_{IH (AC)}$ or $V_{IL (AC)}$	—	—	20	
I_{DDD}	Dynamic Operating (Clock Only)	I_O = 0, V_{DD} = 2.7V, $\overline{\text{RESET}}$ = V_{DD}, V_I = $V_{IH (AC)}$ or $V_{IL (AC)}$, CLK and $\overline{\text{CLK}}$ Switching 50% Duty Cycle.	—	6	—	µA/Clock MHz
	Dynamic Operating (Per Each Data Input)(1)	I_O = 0, V_{DD} = 2.7V, $\overline{\text{RESET}}$ = V_{DD}, V_I = $V_{IH (AC)}$ or $V_{IL (AC)}$, CLK and $\overline{\text{CLK}}$ Switching 50% Duty Cycle. One Data Input Switching at Half Clock Frequency, 50% Duty Cycle.	—	43	—	µA/Clock MHz/Data Input
C_I	Data Inputs	V_{DD} = 2.6V, V_I = V_{REF} ± 310mV	2	—	3	pF
	CLK and $\overline{\text{CLK}}$	V_{ICR} = 1.3V, $V_{I (PP)}$ = 360mV	2	—	3	
	$\overline{\text{RESET}}$	V_I = V_{DD} or GND	2	—	3	

NOTE:
1. Power dissipation levels will allow operation at DDR400 speeds without excessive die temperature.

OPERATING CHARACTERISTICS, T_A = 25°C (1)

Symbol	Parameter		Min.	Typ.(1)	Max.	Unit
V_{DD}	Supply Voltage		V_{DDQ}	—	2.7	V
V_{DDQ}	Output Supply Voltage	PC1600-PC2700	2.3	2.5	2.7	V
		PC3200	2.5	2.6	2.7	
V_{REF}	Reference Voltage (V_{REF}=V_{DDQ}/2)	PC1600-PC2700	1.15	1.25	1.35	V
		PC3200	1.25	1.3	1.35	
V_{TT}	Termination Voltage		V_{REF} – 40mV	V_{REF}	V_{REF} + 40mV	V
V_I	Input Voltage		0	—	V_{DD}	V
V_{IH}	AC High-Level Input Voltage	Data Inputs	V_{REF} + 310mV	—	—	V
V_{IL}	AC Low-Level Input Voltage	Data Inputs	—	—	V_{REF} – 310mV	V
V_{IH}	DC High-Level Input Voltage	Data Inputs	V_{REF} + 150mV	—	—	V
V_{IL}	DC Low-Level Input Voltage	Data Inputs	—	—	V_{REF} – 150mV	V
V_{IH}	High-Level Input Voltage	$\overline{\text{RESET}}$	1.7	—	—	V
V_{IL}	Low-Level Input Voltage	$\overline{\text{RESET}}$	—	—	0.7	V
V_{ICR}	Common-Mode Input Range	CLK, $\overline{\text{CLK}}$	0.97	—	1.53	V
$V_{I (PP)}$	Peak-to-Peak Input Voltage	CLK, $\overline{\text{CLK}}$	360	—	—	mV
I_{OH}	High-Level Output Current		—	—	–16	mA
I_{OL}	Low-Level Output Current		—	—	16	
T_A	Operating Free-Air Temperature		0	—	+70	°C

NOTE:
1. The $\overline{\text{RESET}}$ input of the device must be held at V_{DD} or GND to ensure proper device operation.

TIMING REQUIREMENTS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE

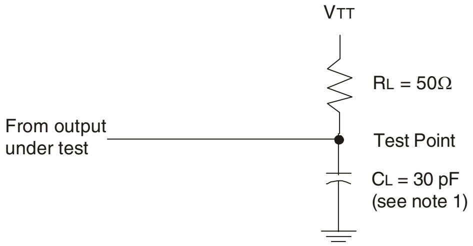
Symbol	Parameter		PC1600 - PC2700		PC3200		Unit
			Min.	Max.	Min.	Max.	
CLOCK	Clock Frequency		—	200	—	220	MHz
t_{W}	Pulse Duration, CLK, $\overline{CLK}$ HIGH or LOW		2.5	—	2.5	—	ns
t_{ACT}	Differential Inputs Active Time(1)		—	22	—	22	ns
t_{INACT}	Differential Inputs Inactive Time(2)		—	22	—	22	ns
t_{SU}	Setup Time, Fast Slew Rate(3, 5)	Data Before CLK↑, $\overline{CLK}$↓	0.65	—	0.65	—	ns
	Setup Time, Slow Slew Rate(4, 5)		0.75	—	0.75	—	ns
t_{H}	Hold Time, Fast Slew Rate(3,5)	Data Before CLK↑, $\overline{CLK}$ ↓	0.75	—	0.65	—	ns
	Hold Time, Slow Slew Rate(2,5)		0.9	—	0.8	—	ns

NOTES:
1. Data inputs must be low a minimum time of t_{ACT} max., after $\overline{RESET}$ is taken HIGH.
2. Data and clock inputs must be held at valid levels (not floating) a minimum time of t_{INACT} max., after $\overline{RESET}$ is taken LOW.
3. For data signal input slew rate is ≥1V/ns.
4. For data signal input slew rate is ≥0.5V/ns and <1V/ns.
5. CLK, $\overline{CLK}$ signal input slew rates are ≥1V/ns.

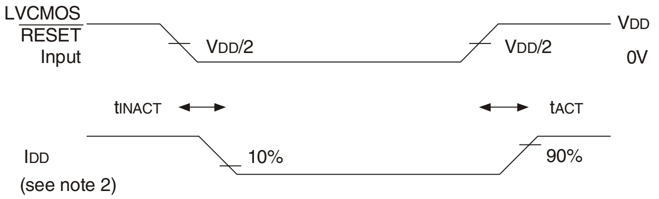
SWITCHING CHARACTERISTICS OVER RECOMMENDED FREE-AIR OPERATING RANGE (UNLESS OTHERWISE NOTED)

Symbol	Parameter	PC1600 - PC2700		PC3200		Unit
		Min.	Max.	Min.	Max.	
f_{MAX}		200	—	220	—	MHz
t_{PDM}	CLK and $\overline{CLK}$ to Q	1.1	2.6	1.1	2.4	ns
t_{PDMSS}	CLK and $\overline{CLK}$ to Q (simultaneous switching)	—	2.9	—	2.68	ns
t_{PHL}	$\overline{RESET}$ to Q	—	5	—	5	ns

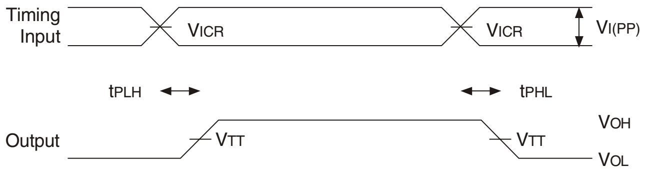
TEST CIRCUITS AND WAVEFORMS
FOR PC1600 - PC2700, V_{DD} = 2.5V ± 0.2V
FOR PC3200, V_{DD} = 2.6V ± 0.1V



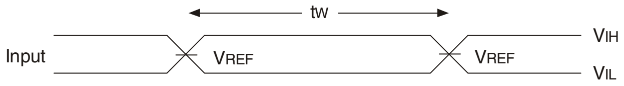
Load Circuit



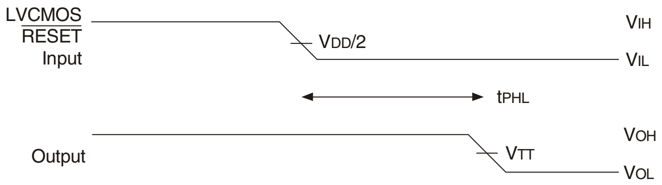
Voltage and Current Waveforms
Inputs Active and Inactive Times



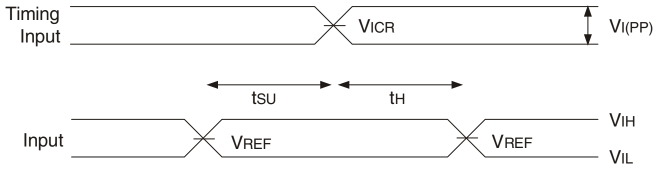
Voltage Waveforms - Propagation Delay Times



Voltage Waveforms - Pulse Duration



Voltage Waveforms - Propagation Delay Times



Voltage Waveforms - Setup and Hold Times

NOTES:
1. C_L includes probe and jig capacitance.
2. I_{DD} tested with clock and data inputs held at V_{DD} or GND, and I_O = 0mA.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, Z_O = 50Ω, input slew rate = 1 V/ns ±20% (unless otherwise specified).
4. The outputs are measured one at a time with one transition per measurement.
5. V_{TT} = V_{REF} = $V_{DDQ}/2$
6. V_{IH} = V_{REF} + 310mV (AC voltage levels) for differential inputs. V_{IH} = V_{DD} for LVCMOS input.
7. V_{IL} = V_{REF} - 310mV (AC voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.
8. t_{PDM} is t_{PD} with one output switching. t_{PDMSS} is t_{PD} with all outputs switching.

ORDERING INFORMATION

IDT74SSTVF	XX	XXX	XX	XX
	Family	Device Type	Package	Process

Blank	0°C to +70°C (Commercial)
PA	Thin Shrink Small Outline Package
PAG	TSSOP - Green
NL	Thermally Enhanced Plastic Very Fine Pitch Quad Flat No Lead Package
NLG	VFQFPN - Green
859	13-Bit to 26-Bit Registered Buffer with SSTL I/O
16	Double-Density

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