VCXO Jitter Attenuator and FemtoClock™ Multiplier

General Description

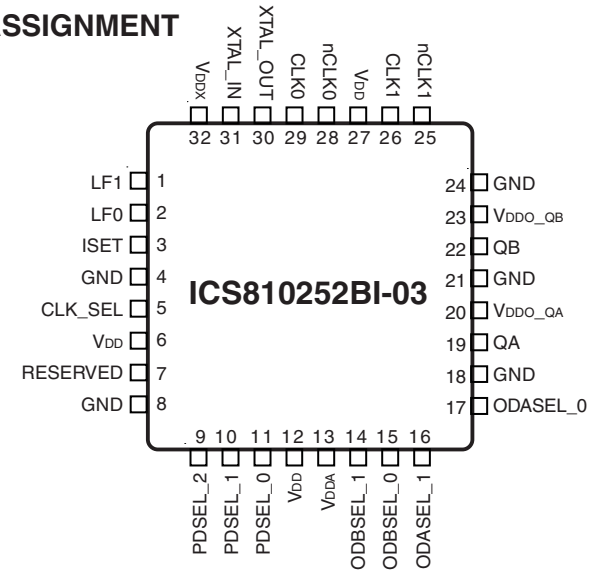
The ICS810252BI-03 is a member of the HiperClockS™ family of high performance clock solutions from IDT. The ICS810252BI-03 is a PLL based synchronous multiplier that is optimized for PDH or SONET to Ethernet clock jitter attenuation and frequency translation. The device contains two internal frequency multiplication stages that are cascaded in series. The first stage is a VCXO PLL that is optimized to provide reference clock jitter attenuation. The second stage is a FemtoClock™ frequency multiplier that provides the low jitter, high frequency Ethernet output clock that easily meets Gigabit and 10 Gigabit Ethernet jitter requirements. Pre-divider and output divider multiplication ratios are selected using device selection control pins. The multiplication ratios are optimized to support most common clock rates used in PDH, SONET and Ethernet applications. The VCXO requires the use of an external, inexpensive pullable crystal. The VCXO uses external passive loop filter components which allows configuration of the PLL loop bandwidth and damping characteristics. The device is packaged in a space-saving 32-TQFP, E-Pad and 32-VFQFN packages and supports industrial temperature range.

Features

- Two LVCMOS/LVTTL outputs, 17Ω impedance
  Each output supports independent frequency selection at 25MHz, 62.5MHz, 125MHz, and 156.25MHz
- Two differential inputs support the following input types: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Accepts input frequencies from 8kHz to 155.52MHz including 8kHz, 1.544MHz, 2.048MHz, 19.44MHz, 25MHz, 77.76MHz, 125MHz and 155.52MHz
- Attenuates the phase jitter of the input clock by using a low-cost pullable fundamental mode VCXO crystal
- VCXO PLL bandwidth can be optimized for jitter attenuation and reference tracking using external loop filter connection
- FemtoClock frequency multiplier provides low jitter, high frequency output
- Absolute pull range: ±50ppm
- FemtoClock VCO frequency: 625MHz
- RMS phase jitter @ 125MHz, using a 25MHz crystal (12kHz - 20MHz): 1.1ps (typical)
- 3.3V supply voltage
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

For functional replacement device use 810252DKI-02LF or 8T49N282B-dddNLGI

Pin Assignment



32-Lead TQFP, E-Pad
7mm x 7mm x 1.0mm package body
Y package
Top View

32-Lead VFQFN
5mm x 5mm x 0.925mm package body
K Package
Top View

BLOCK DIAGRAM

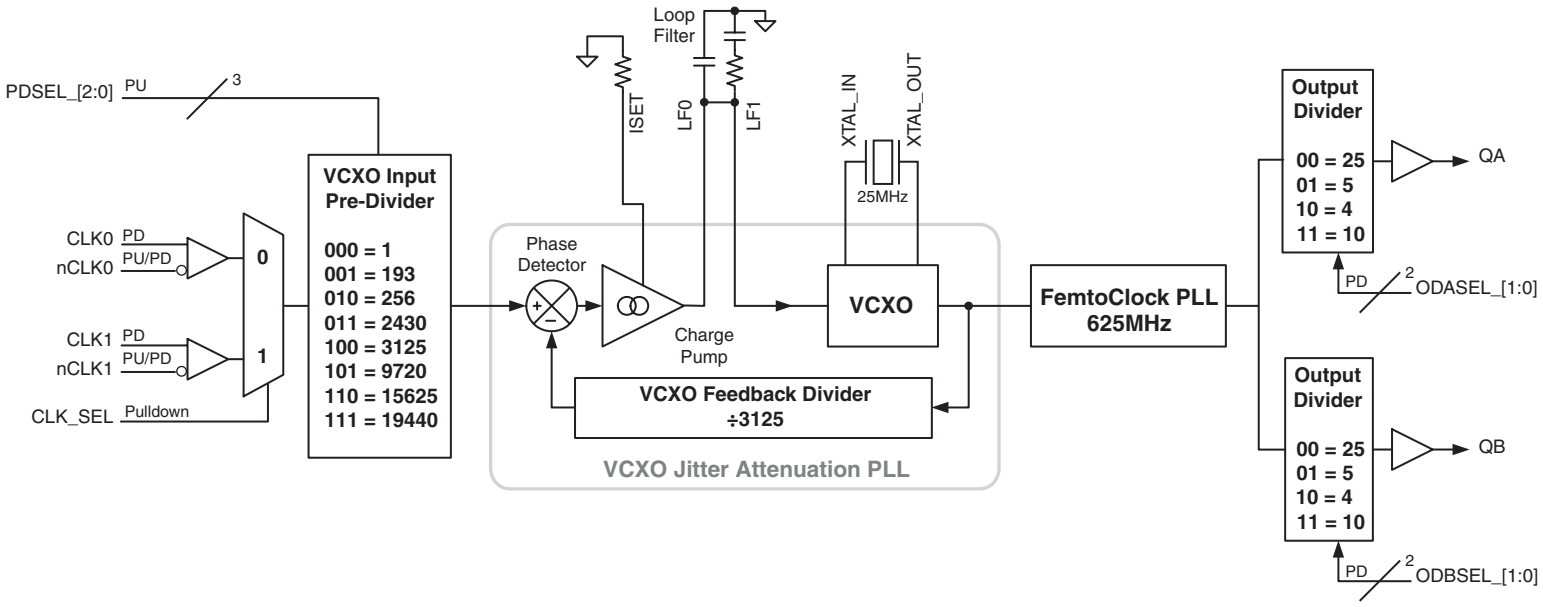


TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	LF1, LF0	Analog Input/Output		Loop filter connection node pins.
3	ISET	Analog Input/Output		Charge pump current setting pin.
4, 8, 18, 21, 24	GND	Power		Power supply ground.
5	CLK_SEL	Input	Pulldown	Input clock select. When HIGH selects CLK1/nCLK1. When LOW, selects CLK0/nCLK0. LVCMOS/LVTTL interface levels.
6, 12, 27	V_{DD}	Power		Core power supply pins.
7	RESERVED	Reserved		Reserved pin. Do not connect.
9, 10, 11	PDSEL_2, PDSEL_1, PDSEL_0	Input	Pullup	Pre-divider select pins. LVCMOS/LVTTL interface levels. See Table 3A.
13	V_{DDA}	Power		Analog supply pin.
14, 15	ODBSEL_1, ODBSEL_0	Input	Pulldown	Frequency select pins for Bank B output. See Table 3B. LVCMOS/LVTTL interface levels.
16, 17	ODASEL_1, ODASEL_0	Input	Pulldown	Frequency select pins for Bank A output. See Table 3B. LVCMOS/LVTTL interface levels.
19	QA	Output		Bank A single-ended clock output. LVCMOS/LVTTL interface levels. 17Ω output impedance.
20	V_{DDO_QA}	Power		Output power supply pin for QA clock output.
22	QB	Output		Bank B single-ended clock output. LVCMOS/LVTTL interface levels. 17Ω output impedance.
23	V_{DDO_QB}	Power		Output power supply pin for QB clock output.
25	nCLK1	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{DD}/2$ bias voltage when left floating.
26	CLK1	Input	Pulldown	Non-inverting differential clock input.
28	nCLK0	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{DD}/2$ bias voltage when left floating.
29	CLK0	Input	Pulldown	Non-inverting differential clock input.
30, 31	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
32	V_{DDX}	Power		Power supply pin for VCXO charge pump.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD}, V_{DDX}, $V_{DDO\_QA,}$ V_{DDO_QB} = 3.465V		10		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{OUT}	Output Impedance			17		Ω

TABLE 3A. PRE-DIVIDER FUNCTION TABLE

Inputs			Pre-Divider Value
PDSEL_2	PDSEL_1	PDSEL_0	
0	0	0	1
0	0	1	193
0	1	0	256
0	1	1	2430
1	0	0	3125
1	0	1	9720
1	1	0	15625
1	1	1	19440 (default)

TABLE 3B. OUTPUT DIVIDER FUNCTION TABLE

Inputs		Output Divider Value
ODxSEL_1	ODxSEL_0	
0	0	25 (default)
0	1	5
1	0	4
1	1	10

TABLE 3C. FREQUENCY FUNCTION TABLE

Input Frequency (MHz)	Pre-Divider Value	VCXO Frequency (MHz)	Femtoclock VCO Frequency (MHz)	Output Divider Value	Output Frequency (MHz)
0.008	1	25	625	25	25
0.008	1	25	625	5	125
0.008	1	25	625	4	156.25
0.008	1	25	625	10	62.5
1.544	193	25	625	25	25
1.544	193	25	625	5	125
1.544	193	25	625	4	156.25
1.544	193	25	625	10	62.5
2.048	256	25	625	25	25
2.048	256	25	625	5	125
2.048	256	25	625	4	156.25
2.048	256	25	625	10	62.5
19.44	2430	25	625	25	25
19.44	2430	25	625	5	125
19.44	2430	25	625	4	156.25
19.44	2430	25	625	10	62.5
25	3125	25	625	25	25
25	3125	25	625	5	125
25	3125	25	625	4	156.25
25	3125	25	625	10	62.5
77.76	9720	25	625	25	25
77.76	9720	25	625	5	125
77.76	9720	25	625	4	156.25
77.76	9720	25	625	10	62.5
125	15625	25	625	25	25
125	15625	25	625	5	125
125	15625	25	625	4	156.25
125	15625	25	625	10	62.5
155.52	19440	25	625	25	25
155.52	19440	25	625	5	125
155.52	19440	25	625	4	156.25
155.52	19440	25	625	10	62.5

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA} 32 Lead VFQFN 32 Lead TQFP	 37°C/W (0 mps) 32.2°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO\_QA} = V_{DDO\_QB} = V_{DDX}$ = 3.3V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.13	3.3	V_{DD}	V
V_{DDO_QA}, V_{DDO_QB}	Output Supply Voltage		3.135	3.3	3.465	V
V_{DDX}	Charge Pump Supply Voltage		3.135	3.3	3.465	V
$I_{DD} + I_{DDX}$	Power and Charge Pump Supply Current				190	mA
I_{DDA}	Analog Supply Current				13	mA
$I_{DDO\_QA} + I_{DDO\_QB}$	Output Supply Current	No Load			2	mA

Table 4B. LVCMOS / LVTTL DC Characteristics, $V_{DD} = V_{DDO\_QA} = V_{DDO\_QB}$ = 3.3V±5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	CLK_SEL, ODASEL_[0:1], ODBSEL_[0:1]	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		PDSEL[0:2]	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	CLK_SEL, ODASEL_[0:1], ODBSEL_[0:1]	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		PDSEL[0:2]	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage; NOTE 1			2.6			V
V_{OL}	Output Low Voltage; NOTE 1					0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDO\_QA,\_QB}$/2.

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, $V_{DD} = V_{DDO\_QA} = V_{DDO\_QB} = V_{DDX}$ = 3.3V±5%, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK0/nCLK0, CLK1/nCLK1	$V_{IN} = V_{DD}$ = 3.465V			150	µA
I_{IL}	Input Low Current	CLK0, CLK1	V_{IN} = 0V, V_{DD} = 3.465V	-5			µA
		nCLK0, nCLK1	V_{IN} = 0V, V_{DD} = 3.465V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

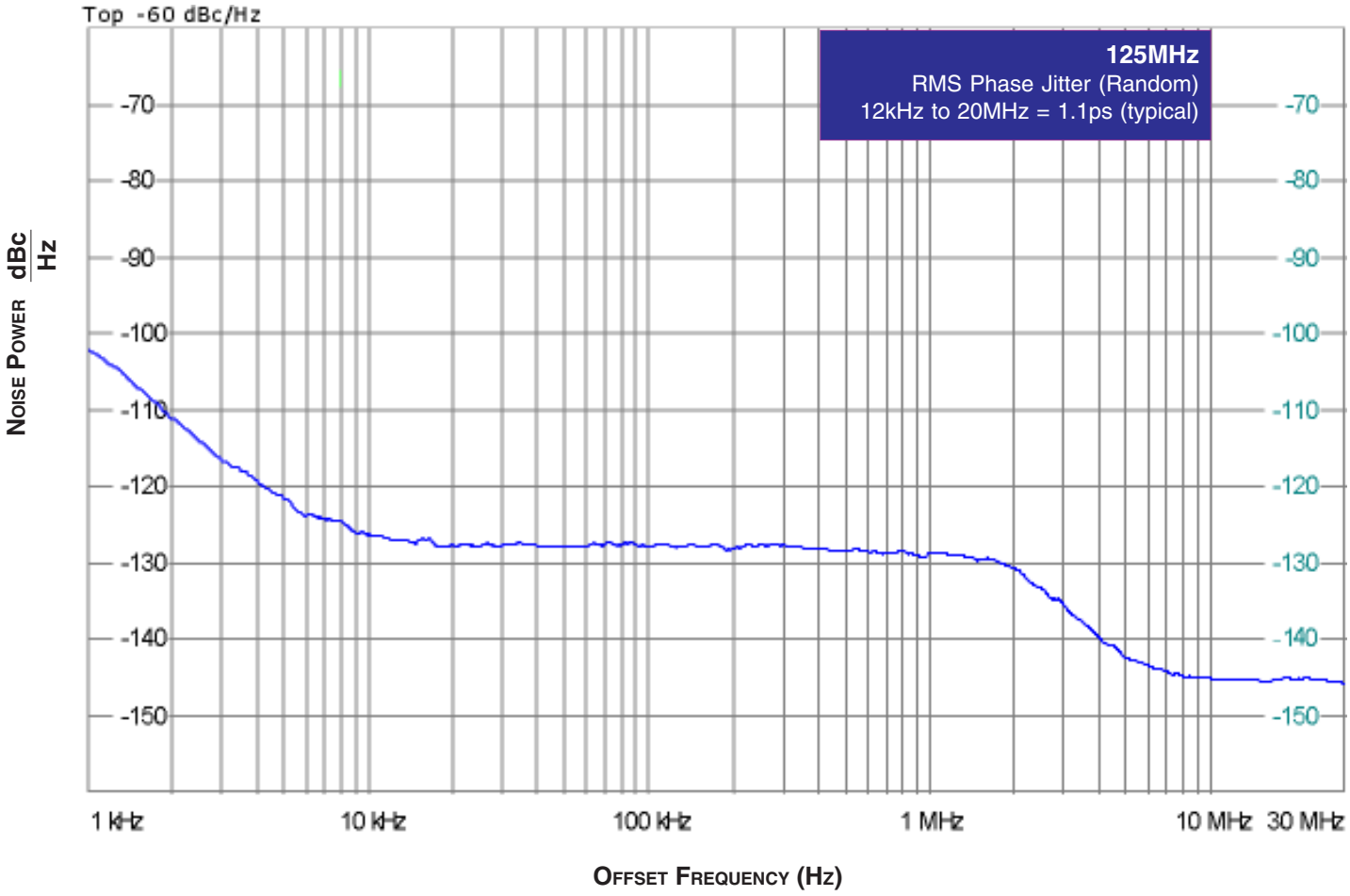
NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 5. AC CHARACTERISTICS, $V_{DD} = V_{DDO\_QA} = V_{DDO\_QB} = V_{DDX}$ = 3.3V±5%, T_A = -40°C TO 85°C

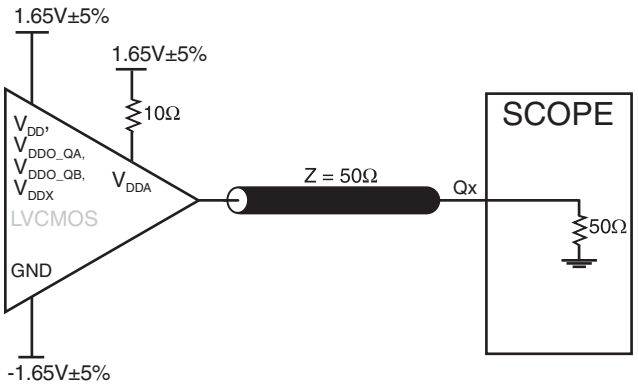
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency		0.008		155.52	MHz
f_{OUT}	Output Frequency		25		156.25	MHz
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 1	125MHz, 25MHz crystal Integration Range: 12kHz - 20MHz		1.1		ps
*t*sk(o)	Output Skew; NOTE 2, 3				130	ps
odc	Output Duty Cycle		47		53	%
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		500	ps
t_{LOCK}	VCXO & FemtoClock PLL Lock Time; NOTE 4	Reference Clock Input is ±50ppm from Nominal Frequency			3	s

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Characterized with outputs at the same frequency using the loop filter components for the high loop bandwidth. Refer to *VCXO-PLL Loop Bandwidth Selection Table.*
NOTE 1: Please refer to the Phase Noise Plot.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs at the same supply voltage, same frequency and with equal load conditions. Measured at V_{DDO}/2.
NOTE 4: Lock time measured from power-up to stable output frequency.

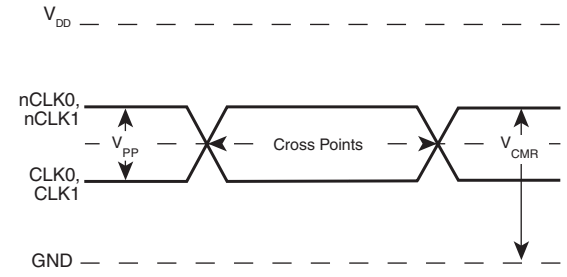
TYPICAL PHASE NOISE AT 125MHZ



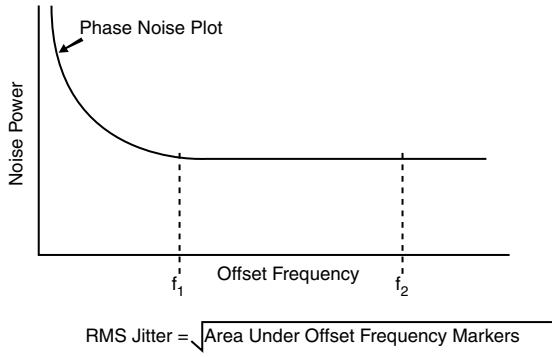
PARAMETER MEASUREMENT INFORMATION



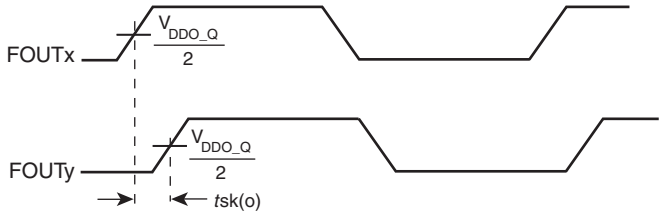
3.3V OUTPUT LOAD AC TEST CIRCUIT



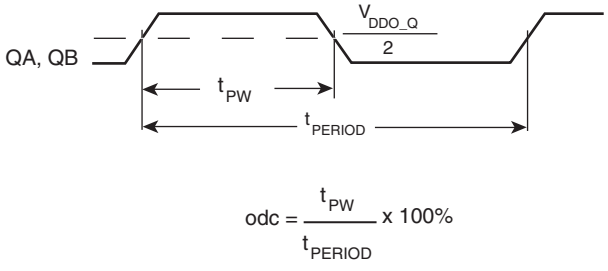
DIFFERENTIAL INPUT LEVEL



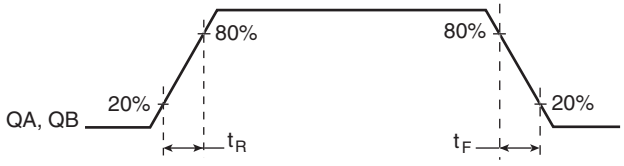
PHASE JITTER



OUTPUT SKEW

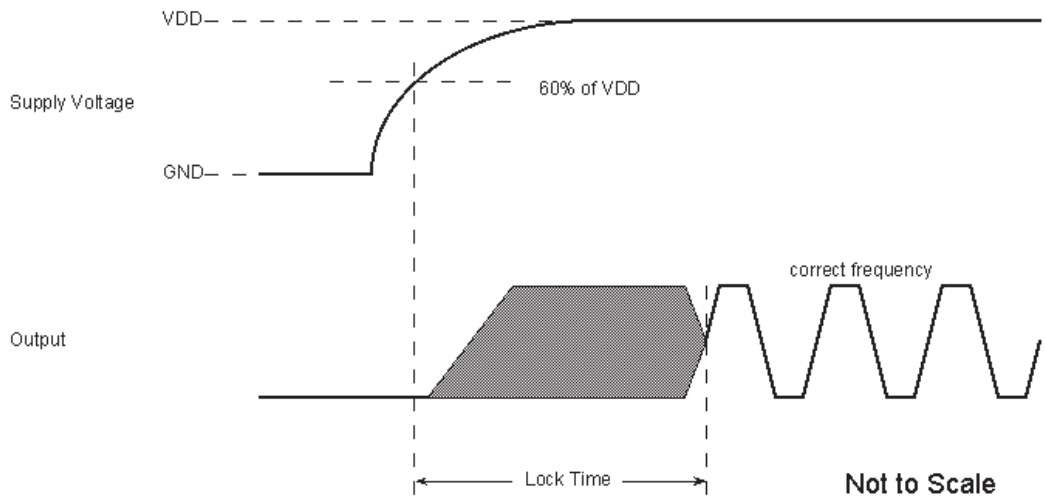


OUTPUT DUTY CYCLE/PULSE WIDTH/tPERIOD



OUTPUT RISE/FALL TIME

PARAMETER MEASUREMENT INFORMATION, CONTINUED



VCXO & FEMTOCLOCK PLL LOCK TIME

APPLICATION INFORMATION

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CLK/nCLK INPUTS
For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

LVCMOS CONTROL PINS
All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVCMOS OUTPUTS
All unused LVCMOS output can be left floating. There should be no trace attached.

Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS810252BI-03 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDX}, V_{DDA}, V_{DDO_QA} and V_{DDO_QB} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

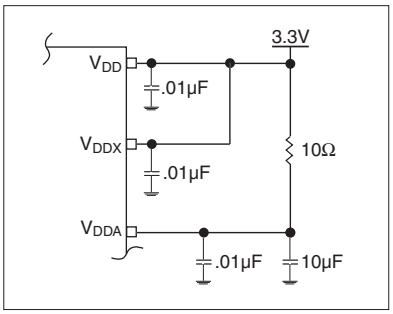


Figure 1. Power Supply Filtering

Wiring the Differential Input to Accept Single Ended Levels

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF ≅ V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

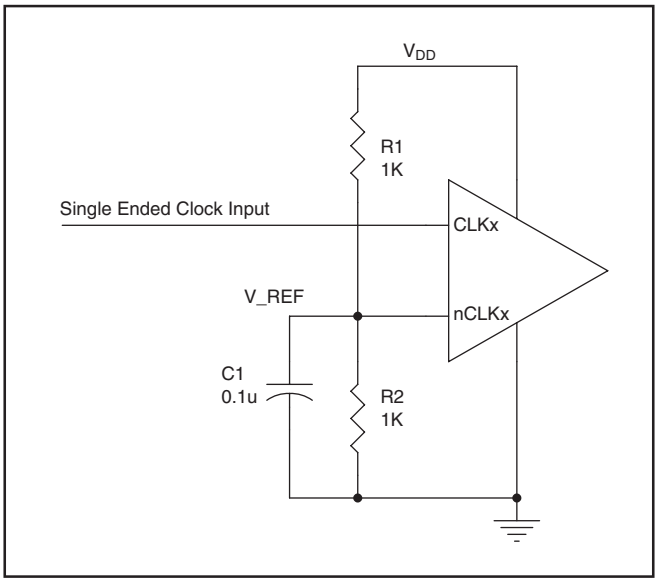


Figure 2. Single Ended Signal Driving Differential Input

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3F* show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in Figure 3A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

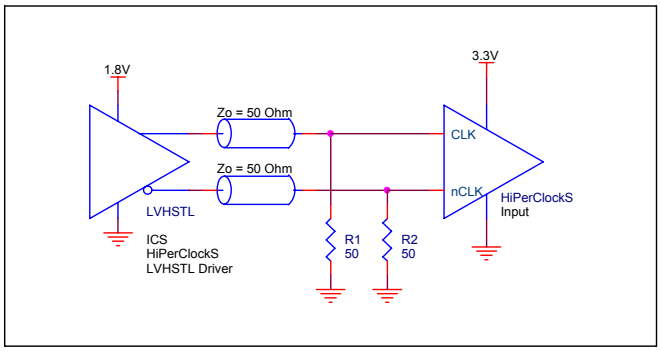


Figure 3A. HiPerClockS CLK/nCLK Input Driven by an IDT Open Emitter HiPerClockS LVHSTL Driver

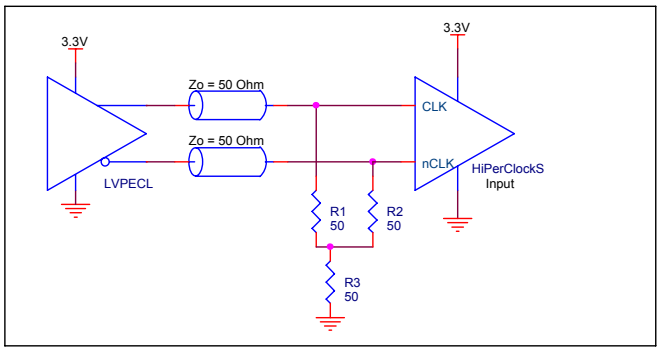


Figure 3B. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

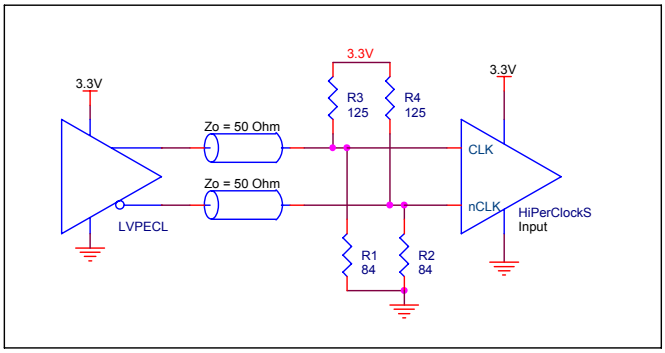


Figure 3C. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

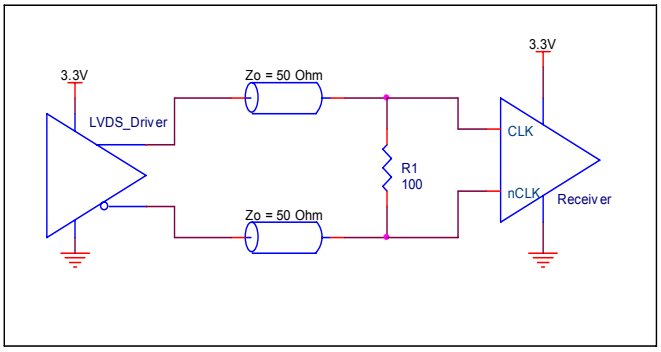


Figure 3D. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVDS Driver

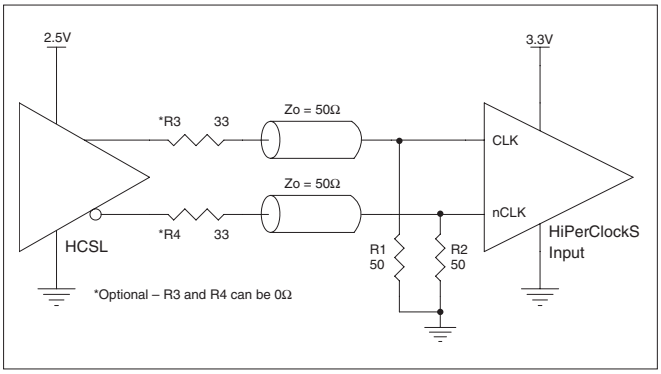


Figure 3E. HiPerClockS CLK/nCLK Input Driven by a 3.3V HCSL Driver

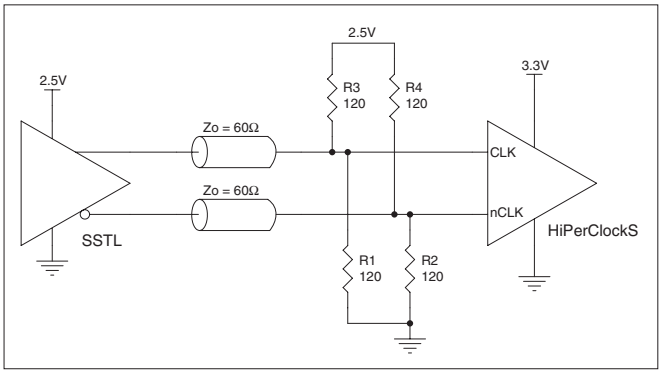


Figure 3F. HiPerClockS CLK/nCLK Input Driven by a 2.5V SSTL Driver

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

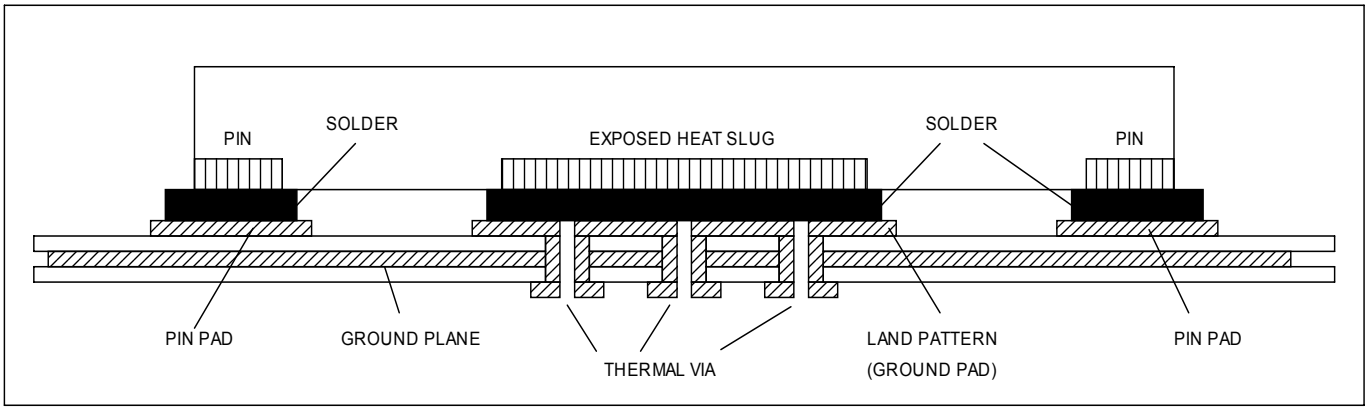


Figure 4. P.C.Assembly for Exposed Pad Thermal Release Path –Side View (Drawing not to Scale)

TQFP EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 5.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

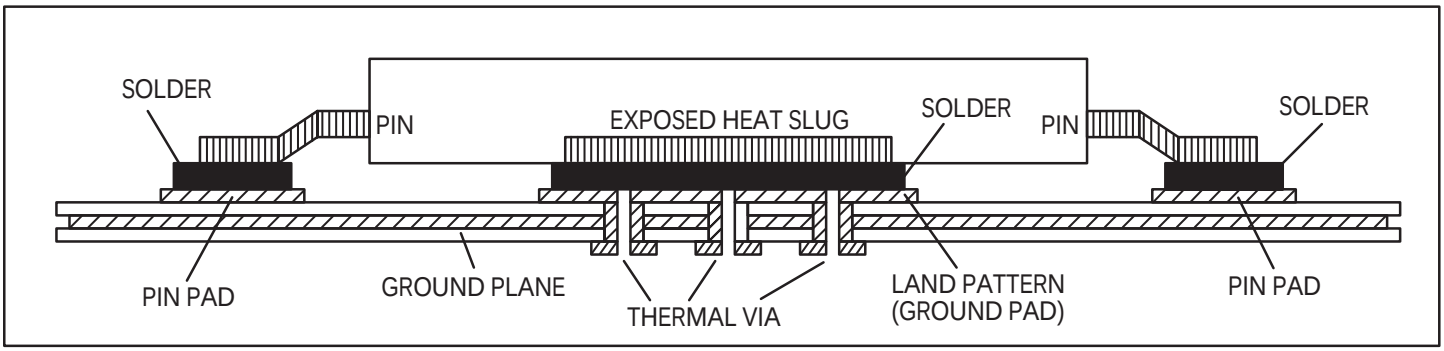


Figure 5. Assembly for Exposed Pad Thermal Release Path –Side View (Drawing not to Scale)

Layout Guideline

Figure 6 shows an example of the 810252IB-03 application schematic. In this example, the device is operated at V_{DD} = 3.3V. The decoupling capacitors should be located as close as possible to the power pin. The input is driven by a 3.3V LVPECL driver. An optional 3-pole filter can also be used for additional spur reduction. It is recommended that the loop filter components be laid out for the 3-pole option. This will also allow the 2-pole filter to be used.

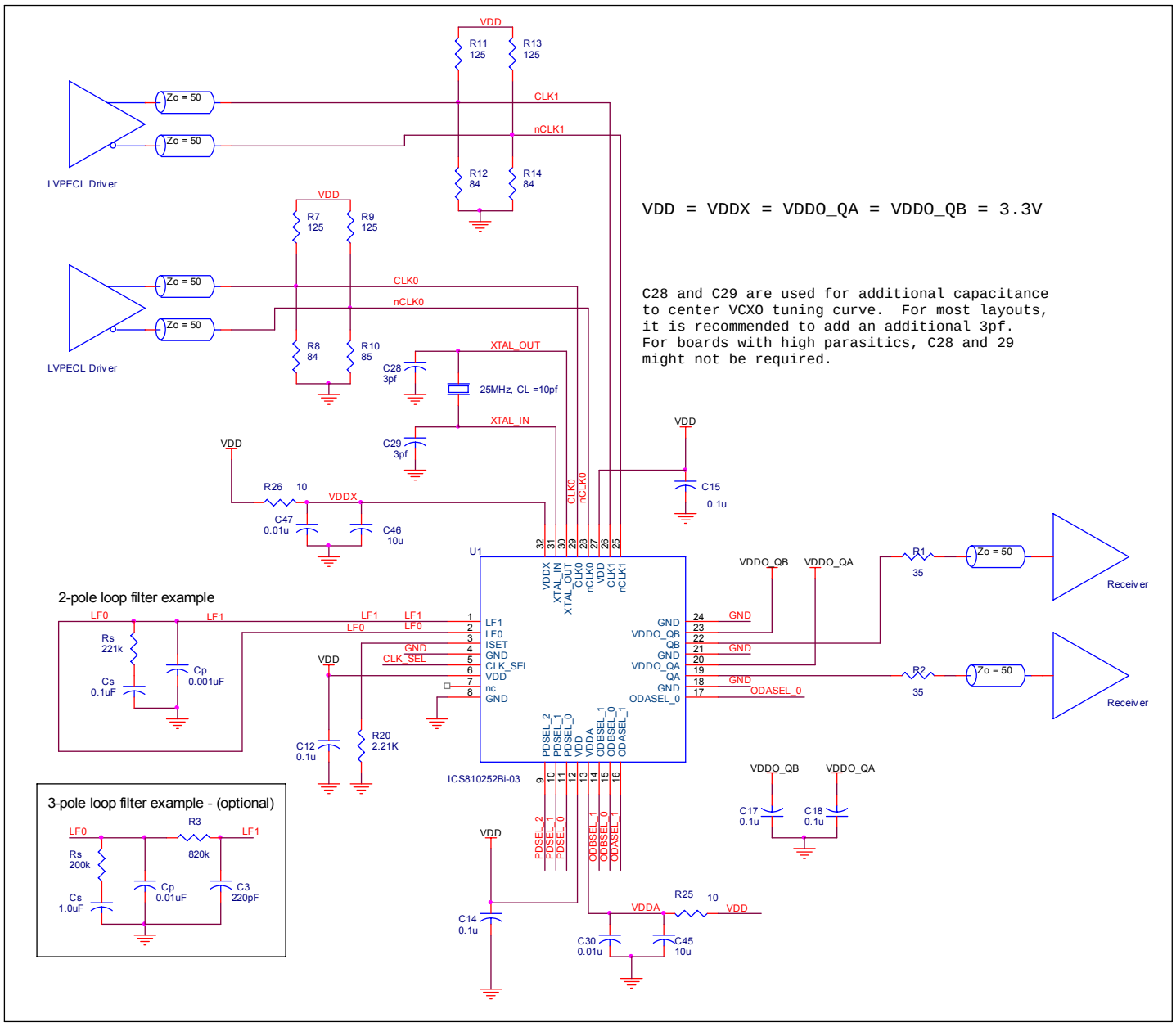


Figure 6. Schematic of Recommended Layout

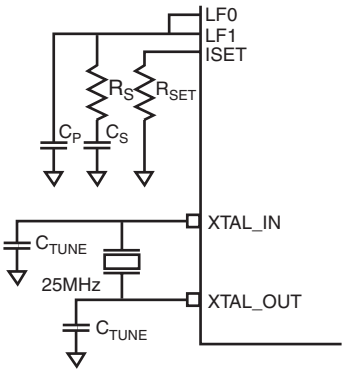
VCXO-PLL External Components

Choosing the correct external components and having a proper printed circuit board (PCB) layout is a key task for quality operation of the VCXO-PLL. In choosing a crystal, special precaution must be taken with the package and load capacitance (C_L). In addition, frequency, accuracy and temperature range must also be considered. Since the pulling range of a crystal also varies with the package, it is recommended that a metal-canned package like HC49 be used. Generally, a metal-canned package has a larger pulling range than a surface mounted device (SMD). For crystal selection information, refer to the *VCXO Crystal Selection Application Note.*

The crystal's load capacitance C_L characteristic determines its resonating frequency and is closely related to the VCXO tuning range. The total external capacitance seen by the crystal when installed on a board is the sum of the stray board capacitance, IC package lead capacitance, internal varactor capacitance and any installed tuning capacitors (C_{TUNE}).

If the crystal C_L is greater than the total external capacitance, the VCXO will oscillate at a higher frequency than the crystal specification. If the crystal C_L is lower than the total external capacitance, the VCXO will oscillate at a lower frequency than the crystal specification. In either case, the absolute tuning range is reduced. The correct value of C_L is dependant on the characteristics of the VCXO. The recommended C_L in the *Crystal Parameter Table* balances the tuning range by centering the tuning curve.

The frequency of oscillation in the third overtone mode is not necessarily at exactly three times the fundamental frequency. The mechanical properties of the quartz element dictate the position of the overtones relative to the fundamental. The oscillator circuit may excite both the fundamental and overtone modes simultaneously. This will cause a nonlinearity in the tuning curve. This potential problem is the reason VCXO crystals are required to be tested for absence of any activity inside a ±200ppm window at three times the fundamental frequency. Refer to F_{L_30VT} and $F_{L\_30VT\_SPURS}$ in the Crystal Characterization Table.



The crystal and external loop filter components should be kept as close as possible to the device. Loop filter and crystal traces should be kept short and separated from each other. Other signal traces should be kept separate and not run underneath the device, loop filter or crystal components.

VCXO Characteristics Table

Symbol	Parameter	Typical	Unit
k_{VCXO}	VCXO Gain	8000	Hz/V
C_{V_LOW}	Low Varactor Capacitance	8	pF
C_{V_HIGH}	High Varactor Capacitance	17	pF

VCXO-PLL Loop Bandwidth Selection Table

Bandwidth	Crystal Frequency (MHz)	R_S (kΩ)	C_S (µF)	C_P (µF)	R_{SET} (kΩ)
10Hz (Low)	25MHz	120	1.0	0.01	8.8
50Hz (Mid)	25MHz	221	0.1	0.001	2.21
125Hz (High)	25MHz	620	0.022	0.0004	2.21

Crystal Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
	Mode of Operation		Fundamental		
f_N	Frequency		25		MHz
f_T	Frequency Tolerance			±20	ppm
f_S	Frequency Stability			±20	ppm
	Operating Temperature Range	-40		85	°C
C_L	Load Capacitance		10		pF
C_O	Shunt Capacitance		4		pF
C_O/C_1	Pullability Ratio		220	240	
F_{L_30VT}	3rd Overtone F_L		200		
$F_{L\_30VT\_SPURS}$	3rd Overtone F_L Spurs		200		
ESR	Equivalent Series Resistance			40	Ω
	Drive Level			1	mW
	Aging @ 25°C			±3 per year	ppm

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS810252BI-03. Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS810252BI-03 is the sum of the core power plus the analog plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

Core Power Dissipation

- Power $(core)_{MAX} = V_{DD\_MAX} * ((I_{DD} + I_{DDX}) + I_{DDA})$ = 3.465V * (190mA + 13mA) = **703.4mW**

Output Power Dissipation

- Output Impedance R_{OUT} Power Dissipation due to Loading 50Ω to $V_{DDO}/2$
  Output Current $I_{OUT} = V_{DDO\_MAX} / [2 * (50Ω + R_{OUT})]$ = 3.465V / [2 * (50Ω + 17Ω)] = **25.9mA**
- Power Dissipation on the R_{OUT} per LVCMOS output
  Power $(R_{OUT}) = R_{OUT} * (I_{OUT})^2$ = 17Ω * (25.9mA)² = **11.4mW per output**
- Total Power Dissipation on the R_{OUT}
  Total Power (R_{OUT}) = 11.4mW * 2 = **22.8mW**

Dynamic Power Dissipation at 125MHz

Power (125MHz) = C_{PD} * Frequency * $(V_{DDO})^2$ = 10pF * 125MHz * (3.465V)² = **15mW per output**
Total Dynamic Power (125MHz) = **15mW * 2 = 30mW**

Total Power Dissipation

- **Total Power**
  = Power $(core)_{MAX}$ + Total Power (R_{OUT}) + Total Dynamic Power (125MHz)
  = 703.4mW + 22.8mW + 30mW
  = 756.2mW

2. Junction Temperature.
Junction temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$
Tj = Junction Temperature
θ_{JA} = Junction-to-Ambient Thermal Resistance
Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)
T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 37°C/W per Table 6A below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.756W * 37°C/W = 113°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of terminated outputs, supply voltage, air flow, and the number of board layers.

TABLE 6A. THERMAL RESISTANCE θ_{JA} FOR 32 LEAD VFQFN, FORCED CONVECTION

θ_{JA} vs. 0 Air Flow (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

TABLE 6B. θ_{JA} VS. AIR FLOW TABLE FOR 32 LEAD TQFP, E-PAD

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	32.2°C/W	26.3°C/W	24.7°C/W

3. Case Temperature calculated from Junction Temperature θ_{JC} Calculations

In applications where there is a heatsink present, and the majority of the power is dissipated through the top of the device, the junction temperature can be calculated from the case temperature, T_C, using the junction-to-case thermal resistance value θ_{JC}. In practical application is it the average of the case temperature of the surface of the device on which the heatsink is attached.

The equation for calculating the junction temperature is as follows:

$$Tj = \theta_{JC} * Pd\_case + T_C$$

Tj = Junction Temperature
θ_{JC}= Junction-to-Case Thermal Resistance
Pd_case = Total Device Power Dissipation *through the case*
T_C = Average Case Temperature

It is important to emphasize that case temperature calculations using θ_{JC} do not use Pd_total, rather they use Pd_case, which is the portion of power dissipated through the case. In real applications it is difficult to quantify the power dissipated through the case, so the value of θ_{JC} is best used for a package-to-package comparison, rather than a junction temperature calculation. As such, the JEDEC standard (JESD51-2) uses another parameter, ψ_{JT} (PsiJT), which can be used to calculate junction temperature from a measured case temperature.

ψ_{JT} Calculations

ψ_{JT} is the thermal characterization parameter which reports the differences between junction temperature and the temperature at the top dead center of the outside surface of the component package, divided by the power applied to the component. This requires knowing the total power dissipation and a measured case temperature in order to calculate the junction temperature. It can also be calculated using an estimated case temperature for a given junction temperature. In the following equation, T_T, is used to indicate the single-point temperature measurement at the top-center of the case. The change in the naming convention from T_C to T_T is to differentiate the use between the θ_{JC} and ψ_{JT} calculations.

The equation for T_J is as follows: $T_J = T_T + \psi_{JT} * Pd\_total$

Solving for T_T yields: $T_T = T_J - \psi_{JT} * Pd\_total$

T_J = Junction Temperature
ψ_{JT} = (PsiJT) Junction-to-Top of Package Parameter
Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)
T_T = Temperature at the top-center of the package

The advantage of this method is that it allows for the calculation of the junction temperature or case temperature using total power dissipation and eliminates the need to quantify power dissipation through the top of the device. In order to calculate T_T, the appropriate ψ_{JT} factor must be used. Assuming no air flow, a multi-layer board, and E-Pad soldered to the board, the appropriate value is 0.3°C/W per Table 7 below. Therefore, T_T for a T_J value of 113°C (from the example in section 2) with all outputs switching is:

T_T = 113.0°C – 0.756W * 0.3°C/W = 112.8°C.

This calculation is only an example. T_J will vary depending on the number of terminated outputs, supply voltage, air flow and the number of board layers.

Table 7. ψ_{JT} for 32 Lead VFQFN, Forced Convection

ψ_{JT} by Velocity (Meters per Second)	
	0
Multi-Layer PCB, JEDEC Standard Test Boards	0.3°C/W

Reliability Information

Table 8A. θ_{JA} vs. Air Flow Table for 32 Lead VFQFN

θ_{JA} vs. 0 Air Flow (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

Table 8B. θ_{JA} vs. Air Flow Table for 32 Lead TQFP, E-Pad

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	32.2°C/W	26.3°C/W	24.7°C/W

Transistor Count

The transistor count for ICS810252BI-03 is: 6597

Package Outline - Y Suffix for 32 Lead TQFP, E-Pad

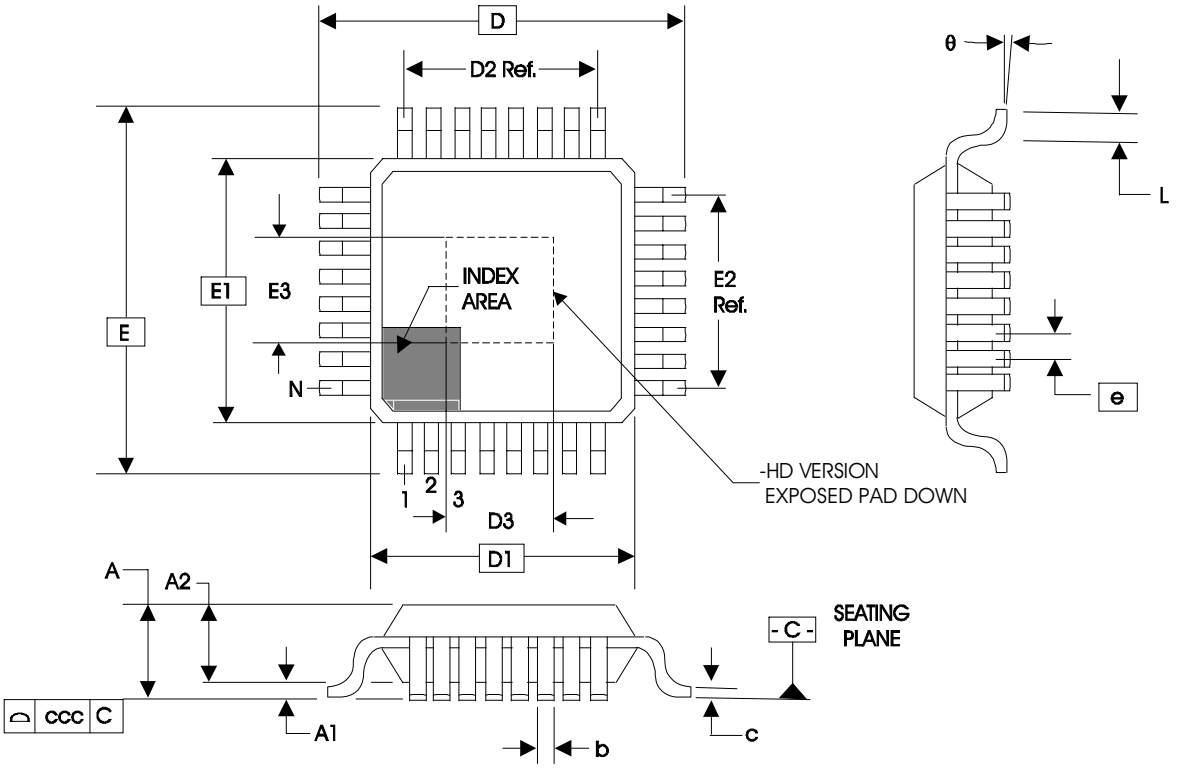
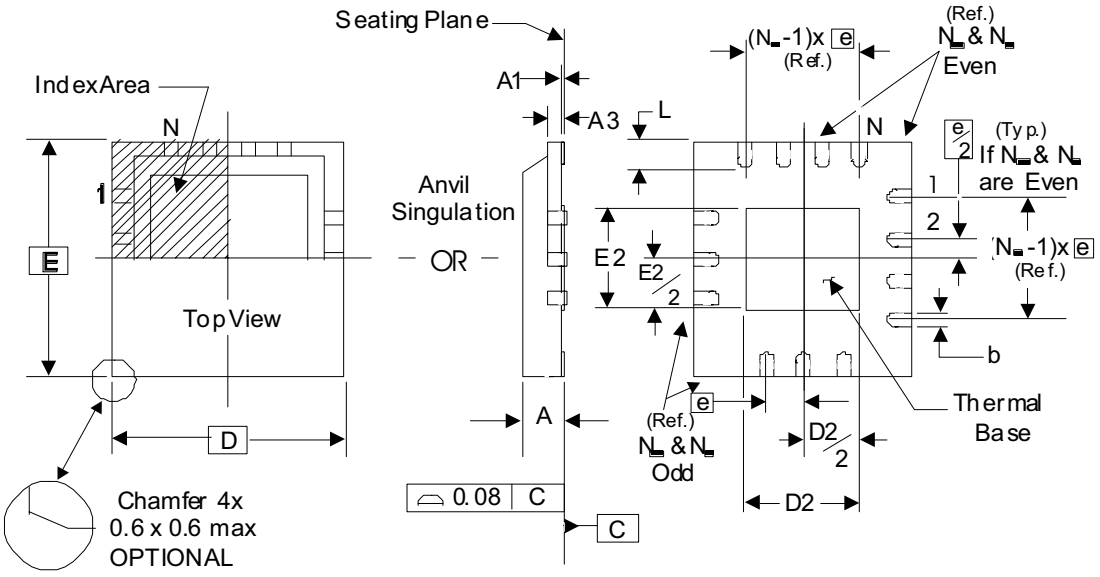


Table 9A. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	ABA-HD		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	--	--	1.20
A1	0.05	0.10	0.15
A2	0.95	1.0	1.05
b	0.30	0.35	0.40
c	0.09	--	0.20
D, E		9.00 BASIC	
D1, E1		7.00 BASIC	
D2, E2		5.60 Ref.	
e		0.80 BASIC	
L	0.45		0.75
θ	0°	--	7°
ccc	--	--	0.10
D3 & D3	3.0	3.5	4.0

Reference Document: JEDEC Publication 95, MS-026

Package Outline and Dimensions - K Suffix for 32 Lead VFQFN



NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 9B below.

Table 9B. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	VHHD-2		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	0.80	--	1.00
A1	0	--	0.05
A3		0.25 Ref.	
b	0.18	0.25	0.30
N_D			8
N_E			8
D		5.00 BASIC	
D2	3.0	3.15	3.3
E		5.00 BASIC	
E2	3.0	3.15	3.3
e		0.50 BASIC	
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
810252BKI-03LF	ICS252BI03L	32 Lead "Lead-Free" VFQFN	tray	-40°C to 85°C
810252BKI-03LFT	ICS252BI03L	32 Lead "Lead-Free" VFQFN	2500 tape & reel	-40°C to 85°C
810252BYI-03LF	ICS0252BI03L	32 lead "Lead-Free" TQFP, E-Pad	tray	-40°C to 85°C
810252BYI-03LFT	ICS0252BI03L	32 lead "Lead-Free" TQFP, E-Pad	1000 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	 T9B	16 21	VCXO-PLL External Components - replace 2nd to last paragraph. Crystal Characteristics Table - add 3rd Overtone specs. VFQFN Package Dimensions - corrected D2/E2 dimensions.	8/20/09
A		1	Product Discontinuation Notice - PDN CQ-14-05	8/21/14

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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