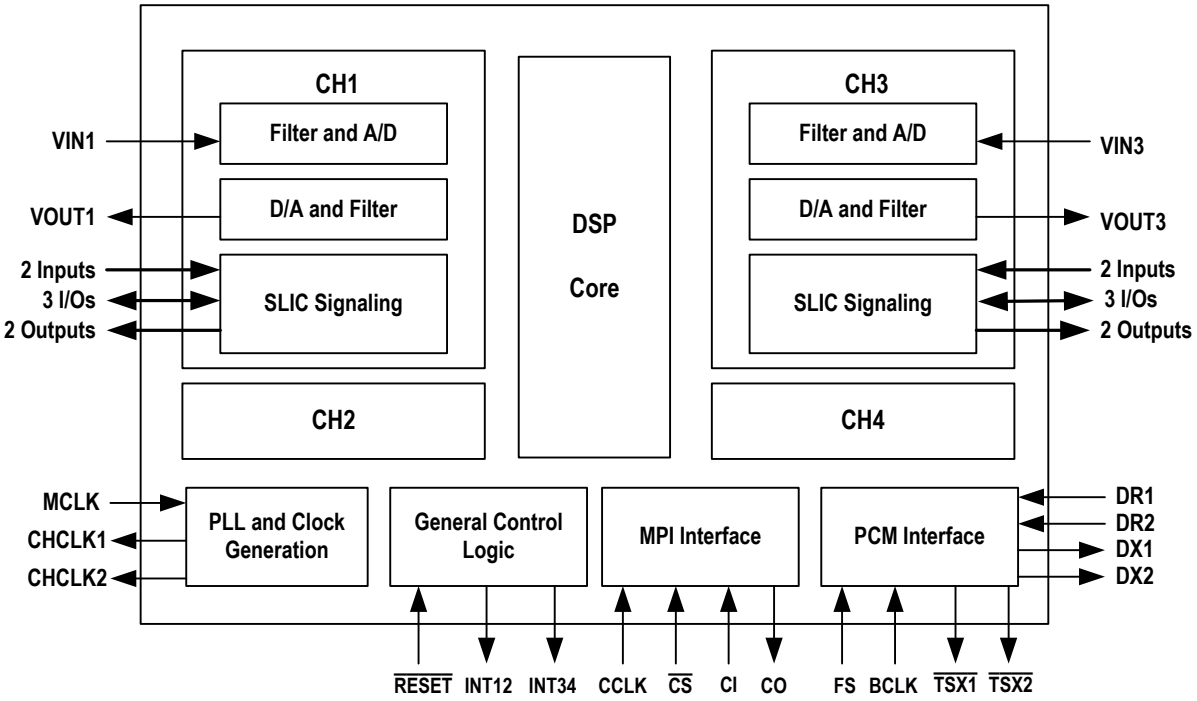
QUAD PROGRAMMABLE PCM CODEC WITH MPI INTERFACE

IDT821054

FEATURES

- 4-channel CODEC with on-chip digital filters
- Software selectable A/μ-law, linear code conversion
- Meets ITU-T G.711 - G.714 requirements
- Programmable digital filters adapting to system demands:
  - AC impedance matching
  - Transhybrid balance
  - Frequency response correction
  - Gain setting
- Supports two programmable PCM buses
- Flexible PCM interface with up to 128 programmable time slots, data rate from 512 kbits/s to 8.192 Mbits/s
- MPI control interface
- Broadcast mode for coefficient setting
- 7 SLIC signaling pins (including 2 debounced pins) per channel
- Fast hardware ring trip mechanism
- 2 programmable tone generators per channel for testing, ringing and DTMF generation
- 1 programmable FSK generator for sending Caller-ID messages
- Two programmable chopper clocks
- Master clock frequency selectable: 1.536 MHz, 1.544 MHz, 2.048 MHz, 3.072 MHz, 3.088 MHz, 4.096 MHz, 6.144 MHz, 6.176 MHz or 8.192 MHz
- Advanced test capabilities:
  - 3 analog loopback tests
  - 5 digital loopback tests
  - Level metering function
- High analog driving capability (300 Ω AC)
- TTL/CMOS compatible digital I/O
- CODEC identification
- +5 V single power supply
- Low power consumption
- Operating temperature range: -40°C to +85°C
- Package available: 64 Pin PQFP

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION

The IDT821054 is a feature rich, single-chip, programmable 4-channel PCM CODEC with on-chip filters. Besides the μ-Law/A-Law companding and linear coding/decoding (14 effective bits + 2 extra sign bits), the IDT821054 also provides 1 FSK generator for sending Caller-ID messages, 2 programmable tone generators per channel (which can generate ring signals) and 2 programmable chopper clocks for SLICs.

The digital filters in the IDT821054 provide necessary transmit and receive filtering for voice telephone circuits to interface with time-division multiplexed systems. An integrated programmable DSP realizes AC impedance matching, transhybrid balance, frequency response correction and gain adjustment functions. The IDT821054 supports 2 PCM buses with programmable sampling edge, which allows an extra delay of up to 7 clocks. Once the delay is determined, it is effective to all four channels of the IDT821054. The device also provides 7 signaling pins per channel for SLICs.

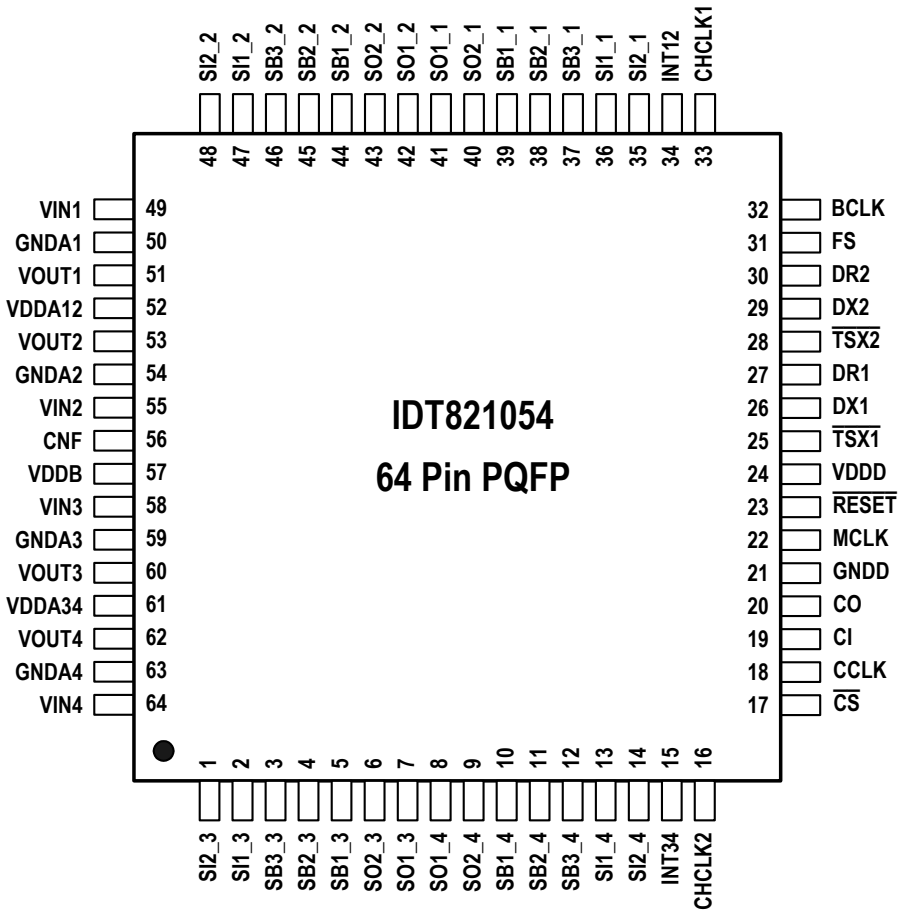
The IDT821054 is programmed via a Microprocessor Interface (MPI). Two PCM buses are provided to transfer the compressed or linear PCM data.

The device offers strong test capability with several analog/digital loopbacks and level metering function. It brings convenience to system maintenance and diagnosis.

A unique feature of “Hardware Ring Trip” is implemented in the IDT821054. When an off-hook signal is detected, the IDT821054 will reverse an output pin to stop the ringing signal immediately.

The IDT821054 can be used in digital telecommunication applications such as Central Office Switch, PBX, DLC and Integrated Access Devices (IADs), i.e. VoIP and VoDSL.

PIN CONFIGURATION



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1 PIN DESCRIPTION

Name	Type	Pin Number	Description
GNDA1 **GNDA2** **GNDA3** **GNDA4**	Ground	50 54 59 63	**Analog Ground.** All ground pins should be connected together.
GNDD	Ground	21	**Digital Ground.** All digital signals are referred to this pin.
VDDA12 **VDDA34**	Power	52 61	**+5 V Analog Power Supply.** These pins should be connected to ground via a 0.1 µF capacitor. All power supply pins should be connected together.
VDDD	Power	24	**+5 V Digital Power Supply.**
VDDB	Power	57	**+5 V Analog Power Supply.** This pin should be connected to ground via a 0.1 µF capacitor. All power supply pins should be connected together.
CNF	–	56	**Capacitor Noise Filter.** This pin should be connected to ground via a 0.22 µF capacitor.
VIN1-4	I	49, 55, 58, 64	**Analog Voice Inputs of Channel 1-4.** These pins should be connected to the corresponding SLIC via a 0.22 µF capacitor.
VOUT1-4	O	51, 53, 60, 62	**Voice Frequency Receiver Outputs of Channel 1-4.** These pins can drive 300 Ω AC load. It can drive transformers directly.
SI1_(1-4) **SI2_(1-4)**	I	36, 47, 2, 13 35, 48, 1, 14	**SLIC Signalling Inputs with debounce function for Channel 1-4.**
SB1_(1-4) **SB2_(1-4)** **SB3_(1-4)**	I/O	39, 44, 5, 10 38, 45, 4, 11 37, 46, 3, 12	**Bi-directional SLIC Signalling I/Os for Channel 1-4.** These pins can be individually programmed as input or output.
SO1_(1-4) **SO2_(1-4)**	O	41, 42, 7, 8 40, 43, 6, 9	**SLIC Signalling Outputs for Channel 1-4.**
DX1	O	26	**Transmit PCM Data Output, PCM Highway One.** Transmit PCM Data to PCM highway one. This pin is a tri-state output pin.
DX2	O	29	**Transmit PCM Data Output, PCM Highway Two.** Transmit PCM Data to PCM highway two. This pin is a tri-state output pin.
DR1	I	27	**Receive PCM Data Input, PCM Highway One.** The PCM data is received from PCM highway one (DR1) or two (DR2). The receive PCM highway is selected by local register LREG6.
DR2	I	30	**Receive PCM Data Input, PCM Highway Two.** The PCM data is received from PCM highway one (DR1) or two (DR2). The receive PCM highway is selected by local register LREG6.
FS	I	31	**Frame Synchronization.** FS is an 8 kHz synchronization clock that identifies the beginning of the PCM frame.
BCLK	I	32	**Bit Clock.** This pin clocks out the PCM data to DX1 or DX2 pin and clocks in PCM data from DR1 or DR2 pin. It may vary from 512 kHz to 8.192 MHz and should be synchronous to FS.
$\overline{\text{TSX1}}$ **$\overline{\text{TSX2}}$**	0	25 28	**Transmit Output Indicator.** The $\overline{\text{TSX1}}$ pin becomes low when PCM data is transmitted via DX1. Open-drain. The $\overline{\text{TSX2}}$ pin becomes low when PCM data is transmitted via DX2. Open-drain.

Name	Type	Pin Number	Description
$\overline{\text{CS}}$	I	17	**Chip Selection.** A logic low level on this pin enables the Serial Control Interface.
CI	I	19	**Serial Control Interface Data Input.** Control data input pin. CCLK determines the data rate.
CO	O	20	**Serial Control Interface Data Output (Tri-State)**. Control data output pin. CCLK determines the data rate.
CCLK	I	18	**Serial Control Interface Clock.** This is the clock for the Serial Control Interface. It can be up to 8.192 MHz.
MCLK	I	22	**Master Clock Input.** This pin provides the clock for the DSP of the IDT821054. The frequency of the MCLK can be 1.536 MHz, 1.544 MHz, 2.048 MHz, 3.072 MHz, 3.088 MHz, 4.096 MHz, 6.144 MHz, 6.176 MHz or 8.192 MHz.
$\overline{\text{RESET}}$	I	23	**Reset Input.** Forces the device to default mode. Active low.
INT12	O	34	**Interrupt Output Pin for Channel 1-2.** Active high interrupt signal for Channel 1 and 2, open-drain. It reflects the changes on the corresponding SLIC input pins.
INT34	O	15	**Interrupt Output Pin for Channel 3-4.** Active high interrupt signal for Channel 3 and 4, open-drain. It reflects the changes on the corresponding SLIC input pins.
CHCLK1	O	33	**Chopper Clock Output One.** Provides a programmable output signal (2 -28 ms) synchronous to MCLK.
CHCLK2	O	16	**Chopper Clock Output Two.** Provides a programmable output signal (256 kHz, 512 kHz or 16.384 MHz) synchronous to MCLK.

2 FUNCTIONAL DESCRIPTION

The IDT821054 is a four-channel PCM CODEC with on-chip digital filters. It provides a four-wire solution for the subscriber line circuitry in digital switches. The IDT821054 converts analog voice signals to digital PCM samples and digital PCM samples back to analog voice signals. The digital filters are used to bandlimit the voice signals during conversion. High performance oversampling Analog-to-Digital Converters (ADC) and Digital-to-Analog Converters (DAC) in the IDT821054 provide the required conversion accuracy. The associated decimation and interpolation filtering is performed by both dedicated hardware and Digital Signal Processor (DSP). The DSP also handles all other necessary procession such as PCM bandpass filtering, sample rate conversion and PCM companding.

2.1 MPI/PCM INTERFACE

A serial Microprocessor Interface (MPI) is provided for the master device to control the IDT821054. Two PCM buses are provided to transfer the digital voice data.

2.1.1 MICROPROCESSOR INTERFACE (MPI)

The internal configuration registers (local/global), the SLIC signaling interface and the Coefficient-RAM of the IDT821054 are programmed by the master device via MPI, which consists of four lines (pins): CCLK, $\overline{CS}$, CI and CO. All commands and data are aligned in byte (8 bits) and transferred via the MPI interface. CCLK is the clock of the MPI interface. The frequency of CCLK can be up to 8.192 MHz. $\overline{CS}$ is the chip selection pin. A low level on $\overline{CS}$ enables the MPI interface. CI and CO are data input and data output pins, carrying control commands and data bytes to/from the IDT821054.

The data transfer is synchronized to the CCLK signal. The contents of CI is latched on the rising edges of CCLK, while CO changes on the falling edges of CCLK. The CCLK signal is the only reference of CI and CO pins. Its duty and frequency may not necessarily be standard.

When the $\overline{CS}$ pin becomes low, the IDT821054 treats the first byte on the CI pin as command and the rest as data. To write another command, the $\overline{CS}$ pin must be changed from low to high to finish the previous command and then changed from high to low to indicate the start of a new command. When a read/write operation is completed, the $\overline{CS}$ pin must be set to high in 8-bit time.

During the execution of commands that are followed by output data byte(s), the IDT821054 will not accept any new commands from the CI pin. But the data transfer sequence can be interrupted by setting the $\overline{CS}$ pin to high at any time. See Figure - 1 and Figure - 2 for examples of MPI write and read operation timing diagrams.

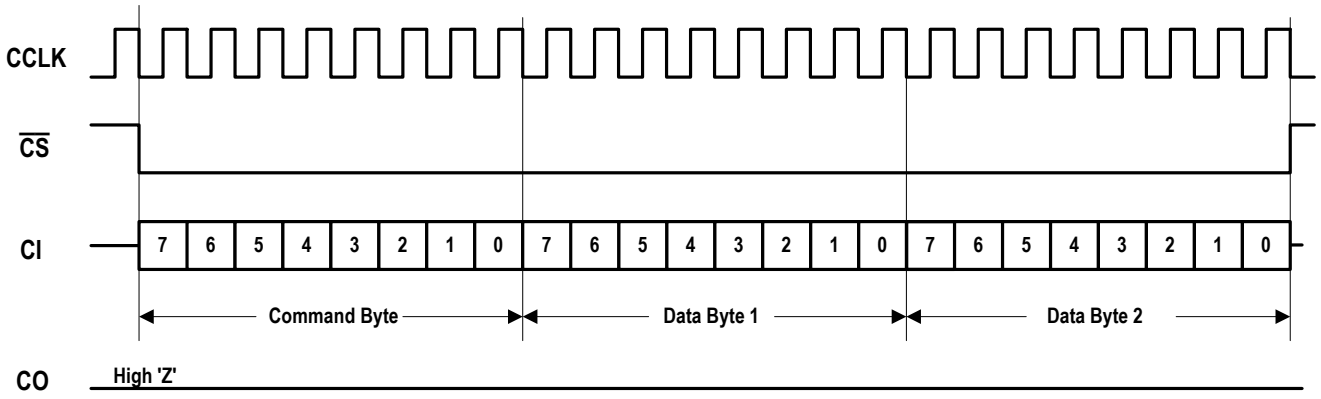


Figure - 1 An Example of the MPI Interface Write Operation

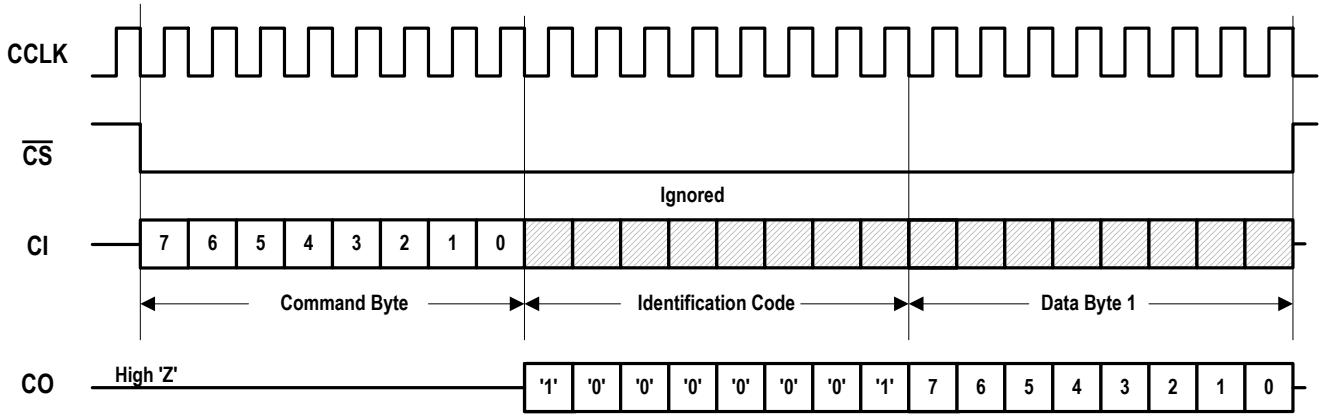


Figure - 2 An Example of the MPI Interface Read Operation (ID = 81H)

2.1.2 PCM BUS

The IDT821054 provides two flexible PCM buses for all 4 channels. The digital PCM data can be compressed (A/μ-law) or linear code. As shown in Figure - 3, the data rate can be configured as same as the Bit Clock (BCLK) or half of it. The PCM data is transmitted or received either on the rising edges or on the falling edges of the BCLK signal. The transmit and receive time slots can offset from the FS signal by 0 to 7 periods of BCLK. All these configurations are made by global register GREG7, which is effective for all four channels.

The PCM data of each channel can be assigned to any time slot of the PCM bus. The number of available time slots is determined by the frequency of the BCLK signal. For example, if the frequency is 512 kHz, 8 time slots (TS0 to TS7) are available. If the frequency is 1.024 MHz, 16 time slots (TS0 to TS15) are available. The IDT821054 accepts BCLK frequency of 512 kHz to 8.192 MHz at increments of 64 kHz.

When compressed PCM code (8-bit wide) is selected, the voice data of one channel occupies one time slot. The TT[6:0] bits in local register LREG5 select the transmit time slot for each channel, while the RT[6:0] bits in LREG6 select the receive time slot for each channel.

When linear PCM code is selected, the voice data is a 16-bit 2's complement number (b13 to b0 are effective bits, b15 and b14 are as same as the sign bit b13). So, the voice data of one channel occupies one time slot group, which consists of 2 adjacent time slots. The TT[6:0] bits in LREG5 select a transmit time slot group for the specified channel. If TT[6:0] = n(d), it means that time slots TS(2n+1) and TS(2n+2) are selected. For example, if TT[6:0] = 00H, it means that TS0 and TS1 are selected. The RT[6:0] bits in LREG6 select a receive time slot group for the specified channel in the same way.

The PCM data of each individual channel can be clocked out to transmit PCM highway one (DX1) or two (DX2) on the programmed edges of BCLK according to time slot assignment. The transmit PCM highway is selected by the THS bit in LREG5. The frame sync (FS) pulse identifies the beginning of a transmit frame (TS0). The PCM data is serially transmitted on DX1 or DX2 with MSB first.

The PCM data of each individual channel is received from receive PCM highway one (DR1) or two (DR2) on the programmed edges of BCLK according to time slot assignment. The receive PCM highway is selected by the RHS bit in LREG6. The frame sync (FS) pulse identifies the beginning of a receive frame (TS0). The PCM data is serially received from DR1 or DR2 with MSB first.

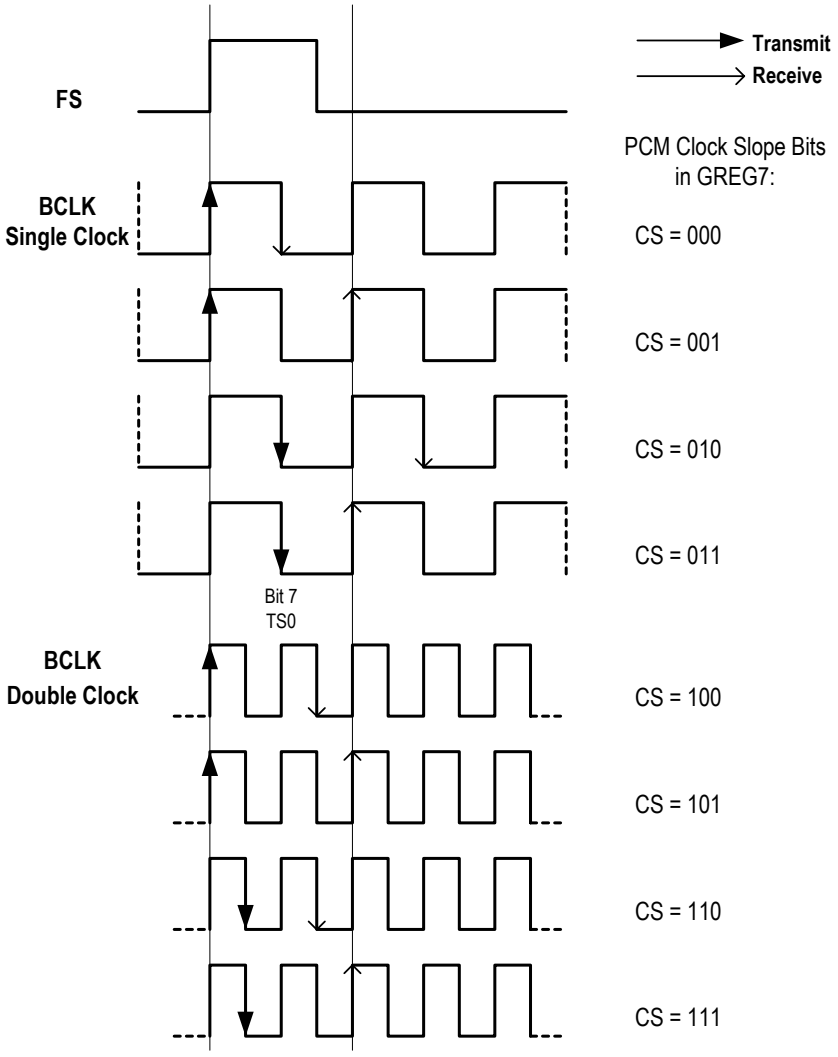


Figure - 3 Sampling Edge Selection Waveform

2.2 DSP PROGRAMMING

2.2.1 SIGNAL PROCESSING

Several blocks are programmable for signal processing. This allows users to optimize the performance of the IDT821054 for the system. Figure - 4 shows the signal flow for each channel and indicates the programmable blocks.

The programmable digital filters are used to adjust gain and impedance, balance transhybrid and correct frequency response. All the coefficients of the digital filters can be calculated automatically by a software provided by IDT. When users provide accurate SLIC model, impedance and gain requirements, this software will calculate all the coefficients automatically. After loading these coefficients to the coefficient RAM of the IDT821054, the final AC characteristics of the line card (consists of SLIC and CODEC) will meet the ITU-T specifications.

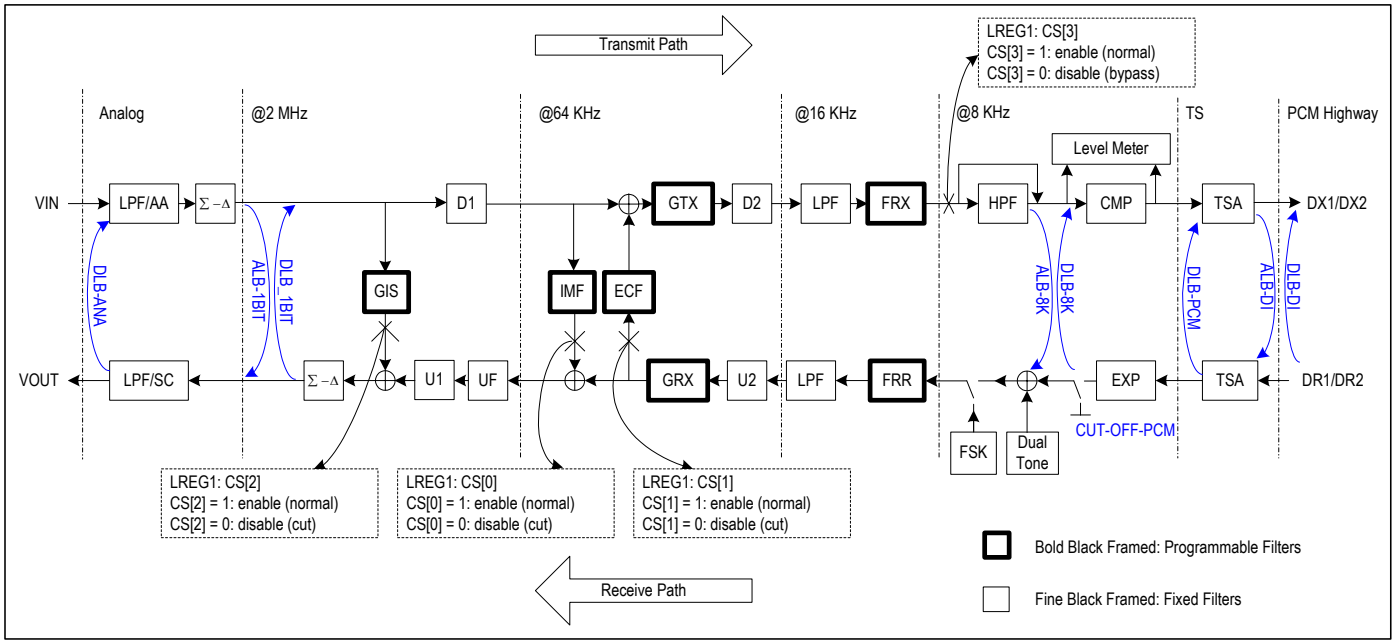


Figure - 4 Signal Flow for Each Channel

Abbreviation List:

LPF/AA: Anti-Alias Low-pass Filter
LPF/SC: Smoothing Low-pass Filter
LPF: Low-pass Filter
HPF: High-pass Filter
GIS: Gain for Impedance Scaling
D1: 1st Down Sample Stage
D2: 2nd Down Sample Stage
U1: 1st Up Sample Stage
U2: 2nd Up Sample Stage
UF: Up Sampling Filter (64 k - 128 k)
IMF: Impedance Matching Filter
ECF: Echo Cancellation Filter
GTX: Gain for Transmit Path
GRX: Gain for Receive Path
FRX: Frequency Response Correction for Transmit
FRR: Frequency Response Correction for Receive
CMP: Compression
EXP: Expansion
TSA: Time Slot Assignment

2.2.2 GAIN ADJUSTMENT

The analog gain and digital gain of each channel can be adjusted separately in the IDT821054.

For each individual channel, the analog A/D gain in the transmit path can be selected as 0 dB or 6 dB. The selection is done by the GAD bit in LREG9. It is 0 dB by default.

For each individual channel, the analog D/A gain in the receive path can be selected as 0 dB or -6 dB. The selection is done by the GDA bit in LREG9. It is 0 dB by default.

For each individual channel, the digital gain in the transmit path (GTX) is programmable from -3 dB to +12 dB with minimum 0.1 dB step. If the CS[5] bit in local register LREG1 is '0', the GTX filter is disabled. If the CS[5] bit is '1', the GTX is programmed by the coefficient RAM.

For each individual channel, the digital gain in the receive path (GRX) is programmable from -12 dB to +3 dB with minimum 0.1 dB step. If the CS[7] bit in LREG1 is '0', the GRX filter is disabled. If the CS[7] bit is '1', the GRX is programmed by the coefficient RAM.

2.2.3 IMPEDANCE MATCHING

The IDT821054 provides a programmable feedback path from VIN to VOUT for each channel. This feedback synthesizes the two-wire impedance of the SLIC. The programmable Impedance Matching Filter (IMF) and Gain of Impedance Scaling filter (GIS) work together to realize impedance matching. If the CS[0] bit in LREG1 is '0', the IMF is disabled. If the CS[0] bit is '1', the IMF coefficient is programmed by the coefficient RAM. If the CS[2] bit in LREG1 is '0', the GIS filter is disabled. If the CS[2] bit is '1', the GIS coefficient is programmed by the coefficient RAM.

2.2.4 TRANSHYBRID BALANCE

The ECF filter is used to adjust transhybrid balance and ensure that the echo cancellation meets the ITU-T specifications. If the CS[1] bit in LREG1 is '0', the ECF filter is disabled. If the CS[1] bit is '1', the ECF coefficient is programmed by the coefficient RAM.

2.2.5 FREQUENCY RESPONSE CORRECTION

The IDT821054 provides two filters that can be programmed to correct any frequency distortion caused by the impedance matching filter. They are the Frequency Response Correction in the Transmit path filter (FRX) and the Frequency Response Correction in the Receive path filter (FRR). If the CS[4] bit in LREG1 is '0', the FRX filter is disabled. If the CS[4] bit is '1', the FRX coefficient is programmed by the coefficient RAM. If the CS[6] bit in LREG1 is '0', the FRR filter is disabled. If the CS[6] bit is '1', the FRR coefficient is programmed by the coefficient RAM.

Refer to "9 Appendix: IDT821054 Coe-RAM Mapping" for the address of the GTX, GRX, FRX, FRR, GIS, ECF and IMF coefficients.

2.3 SLIC CONTROL

The SLIC control interface of the IDT821054 consists of 7 pins per channel: 2 inputs SI1 and SI2, 3 I/Os SB1 to SB3, and 2 outputs SO1 and SO2.

2.3.1 SI1 AND SI2

The SLIC inputs SI1 and SI2 can be read in 2 ways - globally for all 4 channels or locally for each individual channel.

The SI1 and SI2 status of all 4 channels can be read via global register GREG9. The SIA[3:0] bits in this register represent the debounced SI1 data of Channel 4 to Channel 1. The SIB[3:0] bits in this register represent the debounced SI2 data of Channel 4 to Channel 1.

Both the SI1 and SI2 pins can be connected to off-hook, ring trip, ground key signals or other signals. The global register GREG9 provides a more efficient way to obtain time-critical data such as on/off-hook and ring trip information from the SLIC input pins SI1 and SI2.

The SI1 and SI2 status of each channel can also be read via the corresponding local register LREG4.

2.3.2 SB1, SB2 AND SB3

The SLIC I/O pin SB1 of each channel can be configured as input or output via global register GREG10. The SB1C[3:0] bits in GREG10 determine the SB1 directions of Channel 4 to Channel 1: '0' means input and '1' means output. The SB2C[3:0] bits in GREG11 and the SB3C[3:0] bits in GREG12 respectively determine the SB2 and SB3 directions of Channel 4 to Channel 1 in the same way.

If the SB1, SB2 or SB3 pin is selected as input, its information can be read from both global and local registers. The SB1[3:0], SB2[3:0] and SB3[3:0] bits in global registers GREG10, GREG11 and GREG12 respectively contain the information of SB1, SB2 and SB3 for all four channels. Users can also read the information of SB1, SB2 and SB3 of the specified channel from local register LREG4.

If the SB1, SB2 and SB3 pins are configured as outputs, data can only be written to them via GREG10, GREG11 and GREG12 respectively.

2.3.3 SO1 AND SO2

The control data can only be written to the two output pins SO1 and SO2 by local register LREG4 on a per-channel basis. When being read, the SO1 and SO2 bits in LREG4 will be read out with the data written to them in the previous write operation.

2.4 HARDWARE RING TRIP

In order to avoid the damage caused by high voltage ring signal, the IDT821054 provides a hardware ring trip function to respond to the off-hook signal as fast as possible. This function is enabled by setting the RTE bit in GREG8 to '1'.

The off-hook signal can be input via either SI1 or SI2 pin, while the ring control signal can be output via any of the SO1, SO2, SB1, SB2 and SB3 pins (assume that SB1-SB3 are configured as outputs). The IS bit in GREG8 is used to select an input pin and the OS[2:0] bits are used to select an output pin.

When a valid off-hook signal arrives at the selected input pin (SI1 or SI2), the IDT821054 will turn off the ring signal by inverting the logic level of the selected output pin (SO1, SO2, SB1, SB2 or SB3), regardless of the value of the corresponding SLIC output control register (the value should be changed later). This function provides a much faster response to off-hook signals than the software ring trip which turns off the ring signal by changing the value of the corresponding register.

The IPI bit in GREG8 is used to indicate the valid polarity of the input pin. If the off-hook signal is active low, the IPI bit should be set to '0'. If the off-hook signal is active high, the IPI bit should be set to '1'. The OPI bit in GREG8 is used to indicate the valid polarity of the output pin. If the ring control signal is required to be low in normal status and high to activate a ring, the OPI bit should be set to '1'. If it is required to be high in normal status and low to activate a ring, the OPI bit should be set to '0'.

Here is an example: In a system where the off-hook signal is active low and ring control signal is active high, the IPI bit should be set to '0' and the OPI bit should be set to '1'. In normal status, the selected input (off-hook signal) is high and the selected output (ring control signal) is low. When the ring is activated by setting the output (ring control signal) to high, a low pulse appearing on the input (off-hook signal) will inform the device to invert the output to low and cut off the ring signal.

2.5 INTERRUPT AND INTERRUPT ENABLE

An interrupt mechanism is provided in the IDT821054 for reading the SLIC input state. Each change of the SLIC input state will generate an interrupt.

Any of the SLIC inputs including SI1, SI2, SB1, SB2 and SB3 (if SB1-SB3 are configured as inputs) can be an interrupt source. As SI1 and SI2 signals are debounced while the SB1 to SB3 signals are not, users should pay more attention to the interrupt sources of SB1 to SB3.

Local register LREG2 is used to enable/disable the interrupts. Each bit of IE[4:0] in LREG2 corresponds to one interrupt source of the specified channel. When one bit of IE[4:0] is '0', the corresponding interrupt is ignored (disabled), otherwise, the corresponding interrupt is recognized (enabled).

Multiple interrupt sources can be enabled at the same time. All interrupts can be cleared simultaneously by executing a write operation to global register GREG2. Additionally, the interrupts caused by all four

channels' SI1 and SI2 status changes can be cleared by applying a read operation to GREG9. If SB1, SB2 and SB3 pins are configured as inputs, a read operation to GREG10, GREG11 and GREG12 clears the interrupt generated by the corresponding SB port of all four channels. A read operation to LREG4 clears all 7 interrupt sources of the specified channel.

2.6 DEBOUNCE FILTERS

For each channel, the IDT821054 provides two debounce filter circuits: Debounced Switch Hook (DSH) Filter for the SI1 signal and Ground Key (GK) Filter for the SI2 signal. See Figure - 5 for details. The two debounce filters are used to buffer the input signals on SI1 and SI2 pins before changing the state of the SLIC Debounced Input SI1/SI2 Register (GREG9). The Frame Sync (FS) signal is necessary for both DSH and GK filters.

The DSH[3:0] bits in LREG3 are used to program the debounce period of the SI1 input of the corresponding channel. The DSH filter is initially clocked at half of the frame sync rate (250 µs). Any data changing at this sample rate resets a counter that clocks at the rate of 2 ms. The value of the counter is programmable from 0 to 30 via LREG3. The debounced SI1 signals of Channel 4 to 1 are written to the SIA[3:0] bits in GREG9. The corresponding SIA bit will not be updated until the value of the counter is reached. The SI1 pin usually contains the SLIC switch hook status.

The GK[3:0] bits in LREG3 are used to program the debounce interval of the SI2 input of the corresponding channel. The debounced SI2 signals of Channel 4 to 1 are written to the SIB[3:0] bits in GREG9. The GK debounce filter consists of a six-state up/down counter that ranges between 0 and 6. This counter is clocked by the GK timer at the sampling period of 0-30 ms, which is programmed via LREG3. If the sampled value is low, the value of the counter will be decremented by each clock pulse. If the sampled value is high, the value of the counter is incremented by each clock pulse. When the value increases to 6, it sets a latch whose output is routed to the corresponding SIB bit. If the value decreases to 0, the latch will be cleared and the output bit will be set to 0. In other cases, the latch and the SIB status remain in their previous state without being changed. In this way, at least six consecutive GK clocks with the debounce input remaining at the same state can effect an output change.

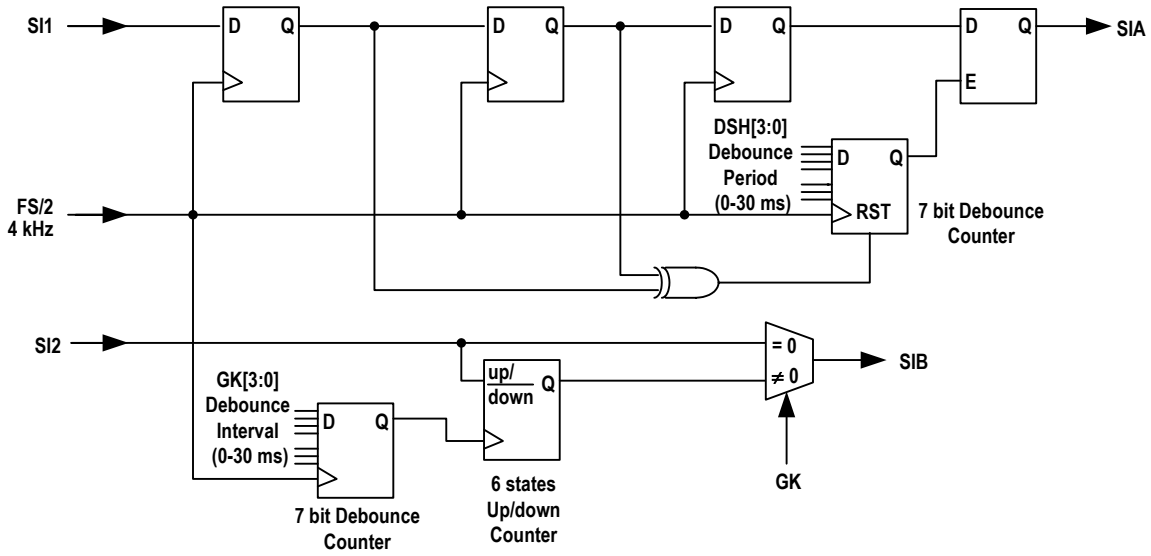


Figure - 5 Debounce Filter

2.7 CHOPPER CLOCK

The IDT821054 provides two programmable chopper clock outputs CHCLK1 and CHCLK2. They can be used to drive the power supply switching regulators on SLICs. The two chopper clocks are synchronous to MCLK. The CHCLK1 outputs a signal which clock cycle is programmable from 2 to 28 ms. The CHCLK2 outputs a signal which frequency can be 256 kHz, 512 kHz or 16.384 MHz. The frequencies of the two chopper clocks are programmed by global register GREG5.

2.8 DUAL TONE AND RING GENERATION

The IDT821054 provides two tone generators (tone generator 0 and tone generator 1) for each channel. They can produce signals such as test tone, DTMF, dial tone, busy tone, congestion tone and Caller-ID Alerting Tone, and output it to the VOUT pin.

The dual tone generators of each channel can be enabled by setting the TEN0 and TEN1 bits in LREG10 to '1'respectively.

The frequency and amplitude of the tone signal are programmed by the Coe-RAM. The frequency and amplitude coefficients are calculated by the following formulas:

Frequency coefficient = $32767 * \cos(f / 8000 * 2 * \pi)$

Amplitude coefficient = $A * 32767 * \sin(f / 8000 * 2 * \pi)$

Herein, 'f' is the desired frequency of the tone signal, 'A' is the scaling parameter of the amplitude. The range of 'A' is from 0 to 1.

A = 1, corresponds to the maximum amplitude of 1.57 V.

A = 0, corresponds to the minimum amplitude of 0 V.

It is a linear relationship between 'A' and the amplitude. That is, if $A=\beta\ (0<\beta<1)$, the amplitude will be $1.57 * \beta$ (V).

The frequency range is from 25 Hz to 3400 Hz. The frequency tolerances are as the following:

25 Hz < f < 40 Hz, tolerance < ±12%

40 Hz < f < 60 Hz, tolerance < ±5%
60 Hz < f < 100 Hz, tolerance < ±2.5%
100 Hz < f < 3400 Hz, tolerance < ±1%

The frequency and amplitude coefficients should be converted to corresponding hexadecimal values before being written to the Coe-RAM. Refer to "9 Appendix: IDT821054 Coe-RAM Mapping" for the address of the tone coefficients.

The ring signal is a special signal generated by the dual tone generators. When only one tone generator is enabled, or dual tone generators produce the same tone signal and frequency of the tone meets the ring signal requirement (10 Hz to 100 Hz), a ring signal will be generated and output to the VOUT pin.

2.9 FSK SIGNAL GENERATION

The IDT821054 has a built-in FSK generator for all four channels to send Caller-ID signals. The general procedure of sending a Caller-ID signal is as shown in Figure - 6.

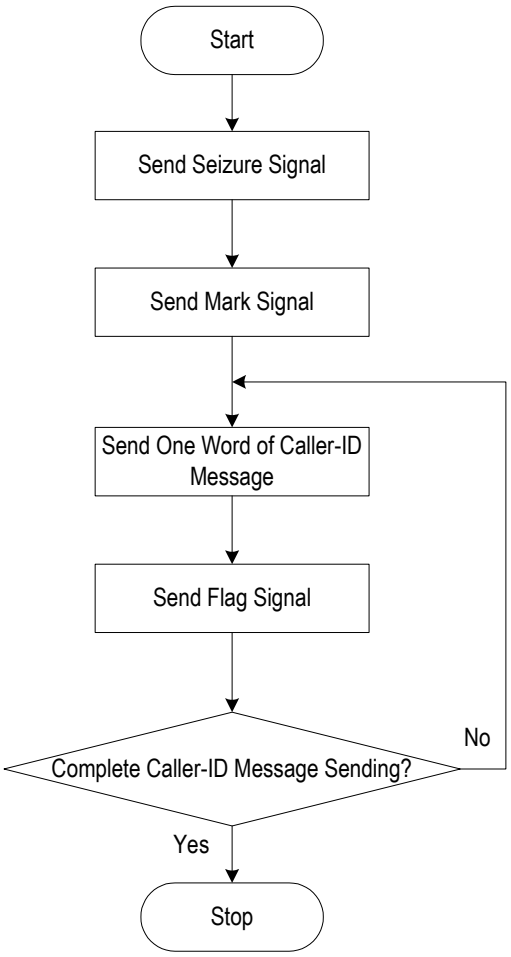


Figure - 6 General Procedure of Sending Caller-ID Signal

The Seizure Signal is a series of '01' pairs. Seizure Length, i.e. the number of the '01' pairs of the Seizure Signal, is programmable. It is two times of the value of the SL[7:0] bits in GREG15. For example, if SL[7:0] = 5 (d), the Seizure Length will be 10 (d).

The Mark Signal is a series of '1'. The length of the Mark Signal (Mark Length) is determined by the ML[7:0] bits in GREG16.

The Caller-ID message should be written to the FSK-RAM before it is sent out. The FSK-RAM consists of 32 words, and each word consists of two bytes, so it can contain up to 64 bytes of message at one time. If the total message is longer than 64 bytes, it should be written to the FSK-RAM at two or more times. Data Length, i.e. the number of the data bytes that are written to the FSK-RAM for transmission, is set by the DL[7:0] bits in GREG14.

One 'Word' of the Caller-ID message consists of 10 bits: one Start Bit at the beginning, one Stop Bit at the end and eight bits of Caller-ID message in the middle. For the IDT821054, the eight bits of Caller-ID message are from the FSK-RAM, and the Start Bit/Stop Bit will be added automatically when sending the Caller-ID message.

The Flag Signal is a series of '1'. The length of the Flag Signal (Flag Length) is determined by the FL[7:0] bits in GREG13.

The BS (BT/Bellcore Selection) bit in GREG17 determines which specification the FSK generator will follow. The IDT821054 supports both Bellcore 202 and BT standards. Table - 1 is the comparison of these two standards.

Table - 1 BT/Bellcore Standard of FSK Signal

Item	BT	Bellcore
Mark (1) frequency	1300 Hz ± 1.5%	1200 Hz ± 1.1%
Space (0) frequency	2100 Hz ± 1.1%	2200 Hz ± 1.1%
Transmission rate	1200 baud ± 1%	1200 Hz ± 1%
Word format	1 start bit which is '0', 8 word bits (with least significant bit LSB first), 1 stop bit which is '1'.	1 start bit which is '0', 8 word bits (with least significant bit LSB first), 1 stop bit which is '1'.

The MAS (Mark After Send) bit in GREG17 determines whether to keep on sending a series of '1's after the completion of sending the content in the FSK-RAM. If the total Caller-ID message is longer than 64 bytes, the MAS bit should be set to '1' to hold the link after the first 64 bytes of Caller-ID message have been sent. Then, users can update the FSK-RAM with new data and send the new data without re-sending the Seizure Signal and Mark Signal. This is important to keep the integrity of Caller-ID information.

The FCS[2:0] (FSK Channel Selection) bits in GREG17 are used to select one of the four channels to send the FSK signal. The FO bit GREG17 is used to enable/disable the FSK generator. When all configurations and FSK-RAM updating have been completed, the FS (FSK Start) bit in GREG17 should be set to '1' to trigger the sending of FSK signal. The FS bit will be reset to '0' after all data bytes in the FSK-RAM have been sent out.

A recommended procedure of programming the FSK generator is shown in Figure - 7.

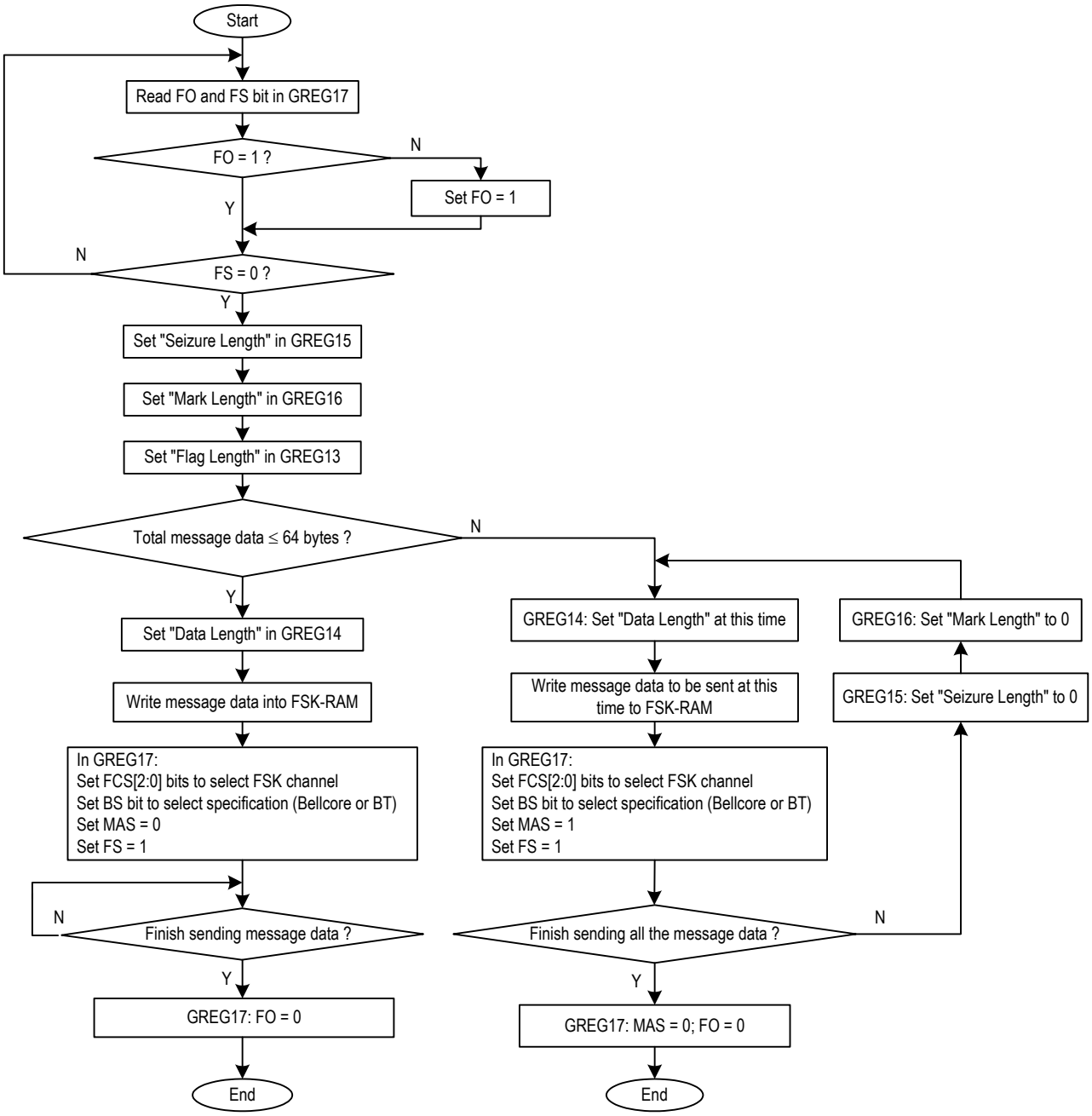


Figure - 7 A Recommended Procedure of Programming the FSK Generator

2.10 LEVEL METERING

The IDT821054 integrates a level meter which is shared by all 4 channels. The level meter is designed to emulate the off-chip PCM test equipment so as to facilitate the line-card, subscriber line and users telephone set monitoring. The level meter tests the return signal and reports the measurement result via the MPI interface. When combined with tone generation and loopbacks, it allows the microprocessor to test the channel integrity. The signal on the channel selected by the CS[1:0] bits in GREG21 will be metered.

The level meter is enabled by setting the LMO bit in GREG21 to '1'. A level meter counter register (GREG20) is used to set the value of time cycles for sampling the PCM data (8 kHz sampling rate). The output of level meter is sent to the level meter result registers GREG18 and GREG19. The LVLL[7:0] bits in GREG18 contain the lower 7 bits of the result and a data-ready bit (LVLL[0]), while the LVLH[7:0] bits in GREG19 contain the higher 8 bits of the result. An internal accumulator sums the rectified samples until the value set in GREG20 is reached. By then, the LVLL[0] bit is set to '1' and accumulation result is latched into GREG18 and GREG19 simultaneously.

Once the higher byte of result (GREG19) is read, the LVLL[0] bit in GREG18 will be reset. It will be set to '1' again by a new data available. The contents of GREG18 and GREG19 will be overwritten by the following metering result if they have not been read out yet. To read the level meter result registers, it is recommended to read GREG18 (lower byte of result) first.

The L/C bit in GREG21 determines the level meter operation mode. If the L/C bit is '1', it means that metering mode is selected. In this mode,

the linear PCM data will be sent to the level meter and the metering result will be output to GREG18 and GREG19. With this result, the signal level can be calculated.

For A-law compressed PCM code or linear PCM code, the signal level can be calculated by the following formula:

$$A(dbm0) = 20 \times \log\left(\frac{LM_{Result} \times 2^5 \times \pi}{LM_{Countnumber} \times 2 \times 8192}\right) + 3.14$$

For μ-law compressed PCM code, the signal level can be calculated by the following formula:

$$A(dbm0) = 20 \times \log\left(\frac{LM_{Result} \times 2^5 \times \pi}{LM_{Countnumber} \times 2 \times 8192}\right) + 3.17$$

LM_{Result}: the value in the level meter result registers (GREG18 & GREG19);

$LM_{Countnumber}$: the count number of the level meter (set in GREG20).

If the L/C bit is '0', it means that message mode is selected. In this mode, the compressed PCM data will be output to GREG19 transparently without metering.

Refer to the Application Note for further details on the level meter.

2.11 CHANNEL POWER DOWN/STANDBY MODE

Each individual channel of the IDT821054 can be powered down independently by setting the PD bit in LREG9 to '1'. If one channel is powered down and enters the standby mode, the PCM data transfer and the D/A, A/D converters of this channel will be disabled. In this way, the power consumption of the device can be reduced.

When the IDT821054 is powered up or reset, all four channels will be powered down. All circuits that contain programmed information retain their data after power down. The microprocessor interface is always active so that new commands can be received and executed.

2.12 POWER DOWN/SUSPEND MODE

A suspend mode is provided for the whole chip to save power. The suspend mode saves much more power consumption than the standby mode. In this mode, the PLL block is turned off and the DSP operation is disabled. Only global and local commands can be executed, the RAM operation is disabled as the internal clock has been turned off. The PLL block is powered down by setting the PPD bit in GREG22 to '1'. Once the PLL and all four channels are powered down, the IDT821054 will enter the suspend mode.

3 OPERATING THE IDT821054

3.1 PROGRAMMING DESCRIPTION

The IDT821054 is programmed by writing commands to registers and coefficient RAM. A Channel Program Enable register (GREG6) is provided for addressing individual or multiple channels. The CE[3:0] bits in this register are assigned to Channel 4 to Channel 1 respectively. The channels are enabled to be programmed by setting their respective CE bits to '1'. If two or more channels are enabled, the successive write commands will be effective to all enabled channels. A broadcast mode can be implemented by simply enabling all four channels before performing other write-operation. The broadcast mode is very useful for configuring the coefficient RAM of the IDT821054 in a large system. But for read operations, multiple addressing is not allowed.

The IDT821054 uses an Identification Code to distinguish itself from other devices in the system. When being read, the IDT821054 will output an Identification Code of 81H first to indicate that the following data bytes are from the IDT821054.

3.1.1 COMMAND TYPE AND FORMAT

The IDT821054 provides three types of commands as follows:

Local Command (LC), which is used to address the local registers of the specified channel(s).

Global Command (GC), which is used to address the global registers of all four channels.

RAM Command (RC), which is used to address the coefficient RAM (Coe-RAM) and FSK-RAM.

The format of the command is as the following:

b7	b6	b5	b4	b3	b2	b1	b0
$\overline{R}$/W	CT		Address				

$\overline{R}$/W: Read/Write Command bit
- b7 = 0: Read Command
- b7 = 1: Write Command

CT: Command Type
- b6 b5 = 00: LC - Local Command
- b6 b5 = 01: GC - Global Command
- b6 b5 = 10: Not Allowed
- b6 b5 = 11: RC - RAM Command

Address: b[4:0], specify one or more local/global registers or a block of Coe-RAM or FSK-RAM to be addressed.

For Local Command and Global Command, the b[4:0] bits are used to specify the address of the local registers and global registers respectively.

For the RAM Command, b4 is used to distinguish the Coe-RAM and the FSK-RAM:

b4 = 0: Command for addressing the Coe-RAM. The b[3:0] bits are used to address the blocks in the Coe-RAM.

b4 = 1: Command for addressing the FSK-RAM. The b3 bit is always '0' and the b[2:0] bits are used to address the blocks in the FSK-RAM.

3.1.2 ADDRESSING THE LOCAL REGISTERS

When addressing the local registers, users must specify which channel(s) will be addressed first. If two or more channels are specified via GREG6, the corresponding local registers of the specified channels will be addressed by a Local Command at the same time.

The IDT821054 provides a consecutive adjacent addressing method for accessing the local registers. According to the address specified in a Local Command, there will be 1 to 4 adjacent local registers to be addressed automatically, with the highest order first. For example, if the address specified in a Local Command ends with '11' (b1b0 = 11), 4 adjacent registers will be addressed by this command; if b1b0 = 10, 3 adjacent registers will be addressed. See Table - 2 for details.

Table - 2 Consecutive Adjacent Addressing

Address Specified in a Local Command	In/Out Data Bytes	Address of the Local Registers to be accessed
b[4:0] = XXX11 (b1b0 = 11, four bytes of data)	byte 1	XXX11
	byte 2	XXX10
	byte 3	XXX01
	byte 4	XXX00
b[4:0] = XXX10 (b1b0 = 10, three bytes of data)	byte 1	XXX10
	byte 2	XXX01
	byte 3	XXX00
b[4:0] = XXX01 (b1b0 = 01, two bytes of data)	byte 1	XXX01
	byte 2	XXX00
b[4:0] = XXX00 (b1b0 = 00, one byte of data)	byte 1	XXX00

When addressing local registers, the procedure of consecutive adjacent addressing can be stopped by the $\overline{CS}$ signal at any time. If $\overline{CS}$ is changed from low to high, the operation to the current register and the next adjacent registers will be aborted. However, the previous operation results will not be affected.

3.1.3 ADDRESSING THE GLOBAL REGISTERS

For global registers are shared by all four channels, it is no need to specify the channel(s) before addressing a global register. Except for this, the global registers are addressed in a similar way as local registers. The procedure of consecutive adjacent addressing can be stopped by the $\overline{CS}$ signal at any time.

3.1.4 ADDRESSING THE COE-RAM

There are totally 40 words of Coe-RAM per channel. They are divided to 5 blocks. Each block consists of 8 words. Each word is 14-bit wide.

The 5 blocks of the Coe-RAM are assigned for different filter coefficients as shown below (refer to "9 Appendix: IDT821054 Coe-RAM Mapping" for the address of the Coe-RAM):

Block 1: IMF RAM (Word 0 - Word 7), containing the Impedance Matching Filter coefficient.

Block 2: ECF RAM (Word 8 - Word 15), containing the Echo Cancellation Filter coefficient.

Block 3: GIS RAM (Word 16 - Word 19) and Tone Generator RAM (Word 20 - Word 23), containing the Gain of Impedance Scaling and dual tone coefficients.

Block 4: FRX RAM (Word 24 - Word 30) and GTX RAM (Word 31), containing the coefficient of the Frequency Response Correction in Transmit Path and the Gain in Transmit Path;

Block 5: FRR RAM (Word 32 - Word 38) and GRX RAM (Word 39), containing the coefficient of the Frequency Response Correction in Receive Path and the Gain in Receive Path.

For the Coe-RAM is addressed on a per-channel basis, users should specify a channel (by setting the corresponding CE bit in GREG6 to '1') before writing/reading coefficients to/from the Coe-RAM.

To write a Coe-RAM word, 16 bits (b[15:0]) or two 8-bit bytes are needed to fulfill with MSB first**,** but the lowest two bits (b[1:0]) will be ignored. When read, each word will output 16 bits with MSB first, but the lowest two bits (b[1:0]) are meaningless.

The address in a Coe-RAM command (b[4:0]) specifies a block of Coe-RAM to be accessed. When a Coe-RAM command is executed, the CODEC automatically counts down from the highest address to the lowest address of the specified block. So all 8 words of the block will be addressed by one Coe-RAM command.

When addressing the Coe-RAM, the procedure of consecutive adjacent addressing can be stopped by the $\overline{CS}$ signal at any time. If the $\overline{CS}$ signal is changed from low to high, the operation to the current word and the next adjacent words will be aborted. However, the previous operation results will not be affected.

3.1.5 ADDRESSING FSK-RAM

The FSK-RAM consists of 4 blocks, and each block has 8 16-bit words. The total 32 words (i.e. 64 bytes) of FSK-RAM are shared by all four channels and only one channel can use it at one time.

To write a FSK-RAM word, 16 bits (or, two 8-bit bytes) are needed to fulfill with MSB first**.** When being read, each FSK-RAM word in FSK-RAM will output 16 bits with MSB first.

When addressing the FSK-RAM, the b3 bit in a FSK-RAM Command should be '0' and the b4 bit should be '1', the b[2:0] bits specify one of the 4 blocks of FSK-RAM. Then, all 8 words of the specified block will be addressed automatically, with the highest order word first.

3.1.6 PROGRAMMING EXAMPLES

3.1.6.1 Example of Programming Local Registers

- **Writing to LREG2 and LREG1 of Channel 1:**

1010, 0101 Channel Enable command
0001, 0010 Data for GREG6 (Channel 1 is enabled for programming)
1000, 0001 Local register write command (The address is '00001', which means that data will be written to LREG2 and LREG1.)
xxxx, xxxx Data for LREG2
xxxx, xxxx Data for LREG1

- **Reading from LREG2 and LREG1 of Channel 1:**

1010, 0101 Channel Enable command
0001, 0010 Data for GREG6 (Channel 1 is enabled for programming)
0000, 0001 Local register read command (The address is '00001', which means that LREG2 and LREG1 will be read.)
After the preceding commands are executed, data will be sent out as follows:
1000, 0001 Identification code
xxxx, xxxx Data read out from LREG2
xxxx, xxxx Data read out from LREG1

3.1.6.2 Example of Programming Global Registers

- **Writing to GREG1:**

1010, 0000 Global register write command (The address is '00000', which means that data will be written to GREG1.)
1111, 1111 Data for GREG1

- **Reading from GREG1:**

0010, 0000 Global register read command (The address is '00000', which means that GREG1 will be read.)
After the preceding command is executed, data will be sent out as follows:
1000, 0001 Identification code
0000, 0001 Data read out from GREG1

3.1.6.3 Example of Programming the Coefficient-RAM

- **Writing to the Coe-RAM**

1010,0101 Channel Enable command
0001,0010 Data for GREG6 (Channel 1 is enabled for programming)
1110,0010 Coe-RAM write command (The address of '00010' is located in block 3, which means that data will be written to block 3.)
data byte 1 high byte of word 8 of block 3
data byte 2 low byte of word 8 of block 3
data byte 3 high byte of word 7 of block 3
data byte 4 low byte of word 7 of block 3
data byte 5 high byte of word 6 of block 3
data byte 6 low byte of word 6 of block 3
data byte 7 high byte of word 5 of block 3
data byte 8 low byte of word 5 of block 3

data byte 9 high byte of word 4 of block 3 (see Note 1)
data byte 10 low byte of word 4 of block 3
data byte 11 high byte of word 3 of block 3
data byte 12 low byte of word 3 of block 3
data byte 13 high byte of word 2 of block 3
data byte 14 low byte of word 2 of block 3
data byte 15 high byte of word 1 of block 3
data byte 16 low byte of word 1 of block 3

Note 1: In block 3 of the Coe-RAM, word 5 to word 8 are used for tone coefficients while word 1 to word 4 are used for GIS coefficients. If users do not want to change the GIS coefficient while writing tone coefficients to the Coe-RAM, they can stop the procedure of consecutive adjacent addressing (after writing data to word 5) by pulling the $\overline{CS}$ signal to high, or they can rewrite word 1 to word 4 with the original GIS coefficients.

- **Reading from the Coe-RAM**

1010,0011 Channel Enable command
0001,0010 Data for GREG6 (Channel 1 is enabled for programming)
0110,0010 Coe-RAM read command (The address of '00010' is located in block 3, which means that block 3 will be read.)
After the preceding commands are executed, data will be sent out as follows:
1000,0001 Identification code
data byte 1 data read out from high byte of word 8 of block 3
data byte 2 data read out from low byte of word 8 of block 3
data byte 3 data read out from high byte of word 7 of block 3
data byte 4 data read out from low byte of word 7 of block 3
data byte 5 data read out from high byte of word 6 of block 3
data byte 6 data read out from low byte of word 6 of block 3
data byte 7 data read out from high byte of word 5 of block 3
data byte 8 data read out from low byte of word 5 of block 3
data byte 9 data read out from high byte of word 4 of block 3
data byte 10 data read out from low byte of word 4 of block 3
data byte 11 data read out from high byte of word 3 of block 3
data byte 12 data read out from low byte of word 3 of block 3
data byte 13 data read out from high byte of word 2 of block 3
data byte 14 data read out from low byte of word 2 of block 3
data byte 15 data read out from high byte of word 1 of block 3
data byte 16 data read out from low byte of word 1 of block 3

3.1.6.4 Example of Programming the FSK-RAM

- **Writing to the FSK-RAM:**

1111,0010 FSK-RAM write command (The address of '010' is located in block 3, which means that data will be written to block 3.)
data byte 1 high byte of word 8 of block 3
data byte 2 low byte of word 8 of block 3
data byte 3 high byte of word 7 of block 3
data byte 4 low byte of word 7 of block 3
data byte 5 high byte of word 6 of block 3
data byte 6 low byte of word 6 of block 3
data byte 7 high byte of word 5 of block 3
data byte 8 low byte of word 5 of block 3
data byte 9 high byte of word 4 of block 3
data byte 10 low byte of word 4 of block 3
data byte 11 high byte of word 3 of block 3
data byte 12 low byte of word 3 of block 3
data byte 13 high byte of word 2 of block 3
data byte 14 low byte of word 2 of block 3
data byte 15 high byte of word 1 of block 3
data byte 16 low byte of word 1 of block 3

- **Reading from the FSK-RAM:**

0111,0010 FSK-RAM read command (The address of '010' is located in block 3, which means that block 3 will be read.)
After the preceding commands are executed, data will be sent out as follows:
1000,0001 Identification code

data byte 1	data read out from high byte of word 8 of block 3
data byte 2	data read out from low byte of word 8 of block 3
data byte 3	data read out from high byte of word 7 of block 3
data byte 4	data read out from low byte of word 7 of block 3
data byte 5	data read out from high byte of word 6 of block 3
data byte 6	data read out from low byte of word 6 of block 3
data byte 7	data read out from high byte of word 5 of block 3
data byte 8	data read out from low byte of word 5 of block 3
data byte 9	data read out from high byte of word 4 of block 3
data byte 10	data read out from low byte of word 4 of block 3
data byte 11	data read out from high byte of word 3 of block 3
data byte 12	data read out from low byte of word 3 of block 3
data byte 13	data read out from high byte of word 2 of block 3
data byte 14	data read out from low byte of word 2 of block 3
data byte 15	data read out from high byte of word 1 of block 3
data byte 16	data read out from low byte of word 1 of block 3

3.2 POWER-ON SEQUENCE

To power on the IDT821054, users should follow the sequence below:

1. Apply ground first;
2. Apply VCC, finish signal connections and set the $\overline{\text{RESET}}$ pin to logic low. The device then goes into the default state;
3. Set the $\overline{\text{RESET}}$ pin to logic high;
4. Select master clock frequency;
5. Program filter coefficients and other parameters as required;

3.3 DEFAULT STATE AFTER RESET

When the IDT821054 is powered on, or reset either by command or by setting the $\overline{\text{RESET}}$ pin to logic low for at least 50 µs, the device will enter the default state as follows:

1. All four channels are powered down and in standby mode.
2. All loopbacks and cutoff are disabled.
3. The DX1 pin is selected for all channels to transmit data and the DR1 pin is selected for all channels to receive data.
4. The master clock frequency is 2.048 MHz.
5. Transmit and receive time slots are set to be 0-3 respectively for Channel 1-4. The PCM data rate is as same as the BCLK frequency. The PCM data is transmitted on rising edges of the BCLK signal and received on falling edges of it.
6. A-Law is selected.
7. The digital filters including GRX, FRR, GTX, FRX, GIS, ECF and IMF are disabled. The high-pass filters (HPF) are enabled. Refer to Figure - 4 and descriptions on LREG1 for details.
8. The SB1, SB2 and SB3 pins are configured as inputs.
9. The SI1 and SI2 pins are configured as no debounce.
10. All interrupts are disabled and all pending interrupts are cleared.
11. All feature function blocks including FSK generator, dual tone generators, hardware ring trip and level meter are disabled.
12. The outputs of CHCLK1 and CHCLK2 are set to high.

The data stored in the RAM will not be changed by any kind of reset operations. So the RAM data will not be lost unless the device is powered down physically.

3.4 REGISTERS DESCRIPTION

3.4.1 REGISTERS OVERVIEW

Table - 3 Global Registers (GREG) Mapping

Name	Function	Register Byte								Read Command	Write Command	Default Value
		b7	b6	b5	b4	b3	b2	b1	b0			
GREG1	Version number (read)/ no operation (write)									20H	A0H	01H
GREG2	Interrupt clear									–	A1H	–
GREG3	Software reset									–	A2H	–
GREG4	Hardware reset									–	A3H	–
GREG5	Chopper clock selection	Reserved		CHclk2[1]	CHclk2[0]	CHclk1[3]	CHclk1[2]	CHclk1[1]	CHclk1[0]	24H	A4H	00H
GREG6	MCLK selection and channel program enable	CE[3]	CE[2]	CE[1]	CE[0]	Sel[3]	Sel[2]	Sel[1]	Sel[0]	25H	A5H	02H
GREG7	Data format, companding law, clock slope and PCM delay time selection	A-μ	VDS	CS[2]	CS[1]	CS[0]	OC[2]	OC[1]	OC[0]	26H	A6H	00H
GREG8	SLIC ring trip setting and control	OPI	Reserved	IPI	IS	RTE	OS[2]	OS[1]	OS[0]	27H	A7H	00H
GREG9	Debounced data on SI1 and SI2 pins	SIB[3]	SIB[2]	SIB[1]	SIB[0]	SIA[3]	SIA[2]	SIA[1]	SIA[0]	28H	–	00H
GREG10	SB1 direction control and SB1 data	SB1C[3]	SB1C[2]	SB1C[1]	SB1C[0]	SB1[3]	SB1[2]	SB1[1]	SB1[0]	29H	A9H	00H
GREG11	SB2 direction control and SB2 data	SB2C[3]	SB2C[2]	SB2C[1]	SB2C[0]	SB2[3]	SB2[2]	SB2[1]	SB2[0]	2AH	AAH	00H
GREG12	SB3 direction control and SB3 data	SB3C[3]	SB3C[2]	SB3C[1]	SB3C[0]	SB3[3]	SB3[2]	SB3[1]	SB3[0]	2BH	ABH	00H
GREG13	FSK Flag Length	FL[7]	FL[6]	FL[5]	FL[4]	FL[3]	FL[2]	FL[1]	FL[0]	2CH	ACH	00H
GREG14	FSK Data Length	DL[7]	DL[6]	DL[5]	DL[4]	DL[3]	DL[2]	DL[1]	DL[0]	2DH	ADH	00H
GREG15	FSK Seizure Length	SL[7]	SL[6]	SL[5]	SL[4]	SL[3]	SL[2]	SL[1]	SL[0]	2EH	AEH	00H
GREG16	FSK Mark Length	ML[7]	ML[6]	ML[5]	ML[4]	ML[3]	ML[2]	ML[1]	ML[0]	2FH	AFH	00H
GREG17	FSK configuration	Reserved		FCS[1]	FCS[0]	FO	BS	MAS	FS	30H	B0H	00H
GREG18	Level meter result low byte	LVLL[7]	LVLL[6]	LVLL[5]	LVLL[4]	LVLL[3]	LVLL[2]	LVLL[1]	LVLL[0]	31H	–	00H
GREG19	Level meter result high byte	LVLH[7]	LVLH[6]	LVLH[5]	LVLH[4]	LVLH[3]	LVLH[2]	LVLH[1]	LVLH[0]	32H	–	00H
GREG20	Level meter count number	CN[7]	CN[6]	CN[5]	CN[4]	CN[3]	CN[2]	CN[1]	CN[0]	33H	B3H	00H
GREG21	level meter mode and channel selection, level meter enable	Reserved				LMO	L/C	CS[1]	CS[0]	34H	B4H	00H
GREG22	Loopback control and PLL power down	Reserved		PPD	DLB_ANA	ALB_8k	DLB_8k	DLB_DI	ALB_DI	35H	B5H	00H
GREG23	Over-sampling timing tuning									37H	B7H	00H

Table - 4 Local Registers (LREG) Mapping

Name	Function	Register Byte								Read Command	Write Command	Default Value
		b7	b6	b5	b4	b3	b2	b1	b0			
LREG1	Coefficient selection	CS[7]	CS[6]	CS[5]	CS[4]	CS[3]	CS[2]	CS[1]	CS[0]	00H	80H	08H
LREG2	Local loopbacks control and SLIC input interrupt enable	IE[4]	IE[3]	IE[2]	IE[1]	IE[0]	DLB_PCM	ALB_1BIT	DLB_1BIT	01H	81H	00H
LREG3	DSH and GK debounce filters configuration	GK[3]	GK[2]	GK[1]	GK[0]	DSH[3]	DSH[2]	DSH[1]	DSH[0]	02H	82H	00H
LREG4	SLIC IO status/control data	Reserved	SO2	SO1	SB3	SB2	SB1	SI2	SI1	03H	83H	–
LREG5	Transmit highway and time slot selection	THS	TT[6]	TT[5]	TT[4]	TT[3]	TT[2]	TT[1]	TT[0]	04H	84H	00H for CH1 01H for CH2 02H for CH3 03H for CH4
LREG6	Receive highway and time slot selection	RHS	RT[6]	RT[5]	RT[4]	RT[3]	RT[2]	RT[1]	RT[0]	05H	85H	00H for CH1 01H for CH2 02H for CH3 03H for CH4
LREG7	PCM data low byte	PCM[7]	PCM[6]	PCM[5]	PCM[4]	PCM[3]	PCM[2]	PCM[1]	PCM[0]	06H	–	00H
LREG8	PCM data high byte	PCM[15]	PCM[14]	PCM[13]	PCM[12]	PCM[11]	PCM[10]	PCM[9]	PCM[8]	07H	–	00H
LREG9	Channel power down, A/D and D/A gains, PCM cutoff	PD	PCMCT	GAD	GDA	0	0	0	0	08H	88H	80H
LREG10	Tone generator enable and tone program enable	Reserved				1	1	TEN1	TEN0	09H	89H	00H

For the global and local registers described below, it should be noted that:
1. R/W = 0, Read command. R/W = 1, Write command.
2. The reserved bit(s) in the registers must be filled in '0' in write operation and be ignored in read operation.

3.4.2 GLOBAL REGISTERS LIST

GREG1: No Operation, Write (A0H); Version Number, Read (20H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	R/W	0	1	0	0	0	0	0

By applying a read operation (20H) to this register, users can read out the version number of the IDT821054. The default value is 01H. To write to this register (no operation), a data byte of FFH must follow the write command (A0H) to ensure proper operation.

GREG2: Interrupt Clear, Write Only (A1H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	1	0	1	0	0	0	0	1

All interrupts on SLIC I/O will be cleared by applying a write operation to this register. Note that a data byte of FFH must follow the write command (A1H) to ensure proper operation.

GREG3: Software Reset, Write Only (A2H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	1	0	1	0	0	0	1	0

A write operation to this register resets all local registers, but does not reset global registers and RAM. Note that when writing to this register, a data byte of FFH must follow the write command (A2H) to ensure proper operation.

GREG4: Hardware Reset, Write Only (A3)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	1	0	1	0	0	0	1	1

A write operation to this register is equivalent to setting the RESET pin to logic low (Refer to "3.3 Default State After Reset" on page 21 for details). Note that when applying this write command, a data byte of FFH must follow to ensure proper operation.

GREG5: Chopper Clock Selection, Read/Write (24H/A4H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	R/W	0	1	0	0	1	0	0
I/O data	Reserved		Chclk2[1]	Chclk2[0]	Chclk1[3]	Chclk1[2]	Chclk1[1]	Chclk1[0]

This register is used to select the frequency of the CHclk2 and CHclk1 output signals.
CHclk2[1:0] = 00: the output of chclk2 is set to high permanently (default);
CHclk2[1:0] = 01: chclk2 outputs a digital signal with the frequency of 512 kHz;
CHclk2[1:0] = 10: chclk2 outputs a digital signal with the frequency of 256 kHz;
CHclk2[1:0] = 11: chclk2 outputs a digital signal with the frequency of 16384 kHz;

CHclk1[3:0] = 0000: the output of chclk1 is set to high permanently (default);
CHclk1[3:0] = 0001: chclk1 outputs a digital signal with the frequency of 1000/2 Hz;
CHclk1[3:0] = 0010: chclk1 outputs a digital signal with the frequency of 1000/4 Hz;
CHclk1[3:0] = 0011: chclk1 outputs a digital signal with the frequency of 1000/6 Hz;
CHclk1[3:0] = 0100: chclk1 outputs a digital signal with the frequency of 1000/8 Hz;
CHclk1[3:0] = 0101: chclk1 outputs a digital signal with the frequency of 1000/10 Hz;
CHclk1[3:0] = 0110: chclk1 outputs a digital signal with the frequency of 1000/12 Hz;
CHclk1[3:0] = 0111: chclk1 outputs a digital signal with the frequency of 1000/14 Hz;

CHclk1[3:0] = 1000: chclk1 outputs a digital signal with the frequency of 1000/16 Hz;
CHclk1[3:0] = 1001: chclk1 outputs a digital signal with the frequency of 1000/18 Hz;
CHclk1[3:0] = 1010: chclk1 outputs a digital signal with the frequency of 1000/20 Hz;
CHclk1[3:0] = 1011: chclk1 outputs a digital signal with the frequency of 1000/22 Hz;
CHclk1[3:0] = 1100: chclk1 outputs a digital signal with the frequency of 1000/24 Hz;
CHclk1[3:0] = 1101: chclk1 outputs a digital signal with the frequency of 1000/26 Hz;
CHclk1[3:0] = 1110: chclk1 outputs a digital signal with the frequency of 1000/28 Hz;
CHclk1[3:0] = 1111: the output of chclk1 is set to low permanently.

GREG6: MCLK Selection and Channel Program Enable, Read/Write (25H/A5H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	0	0	1	0	1
I/O data	CE[3]	CE[2]	CE[1]	CE[0]	Sel[3]	Sel[2]	Sel[1]	Sel[0]

The higher 4 bits (CE[3:0]) in this register are used to specify the desired channel(s) before addressing local registers or Coe-RAM. The CE[0] to CE[3] bits indicate the program enable state for Channel 1 to Channel 4 respectively.
CE[0] = 0: Disabled, Channel 1 can not receive programming commands (default);
CE[0] = 1: Enabled, Channel 1 can receive programming commands;
CE[1] = 0: Disabled, Channel 2 can not receive programming commands (default);
CE[1] = 1: Enabled, Channel 2 can receive programming commands;
CE[2] = 0: Disabled, Channel 3 can not receive programming commands (default);
CE[2] = 1: Enabled, Channel 3 can receive programming commands;
CE[3] = 0: Disabled, Channel 4 can not receive programming commands (default);
CE[3] = 1: Enabled, Channel 4 can receive programming commands.

The lower 4 bits (Sel[3:0]) in this register are used to select the Master Clock frequency.
Sel[3:0] = 0000: 8.192 MHz
Sel[3:0] = 0001: 4.096 MHz
Sel[3:0] = 0010: 2.048 MHz (default)
Sel[3:0] = 0110: 1.536 MHz
Sel[3:0] = 1110: 1.544 MHz
Sel[3:0] = 0101: 3.072 MHz
Sel[3:0] = 1101: 3.088 MHz
Sel[3:0] = 0100: 6.144 MHz
Sel[3:0] = 1100: 6.176 MHz

GREG7: A/μ-law, Linear/Compressed Code, Clock Slope and Delay Time Selection, Read/Write (26H/A6H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	0	0	1	1	0
I/O data	A-μ	VDS	CS[2]	CS[1]	CS[0]	OC[2]	OC[1]	OC[0]

The A/μ-law select bit (A-μ) selects the companding law:
A-μ = 0: A-law is selected (default)
A-μ = 1: μ-law is selected.

The Voice Data Select bit (VDS) defines the format of the voice data:
VDS = 0: Compressed code (default)
VDS = 1: Linear code

The Clock Slope bits (CS[2:0]) select single or double clock and clock edges of transmitting and receiving data.
CS[2] = 0: Single clock (default)
CS[2] = 1: Double clock

CS[1:0] = 00: transmits data on rising edges of BCLK, receives data on falling edges of BCLK (default).
CS[1:0] = 01: transmits data on rising edges of BCLK, receives data on rising edges of BCLK.

CS[1:0] = 10: transmits data on falling edges of BCLK, receives data on falling edges of BCLK.
CS[1:0] = 11: transmits data on falling edges of BCLK, receives data on rising edges of BCLK.

The PCM data Offset Configuration bits (OC[2:0]) determine that the transmit and receive time slots of PCM data offset from the FS signal by how many periods of BCLK:
OC[2:0] = 000: 0 period of BCLK (default);
OC[2:0] = 001: 1 period of BCLK;
OC[2:0] = 010: 2 periods of BCLK;
OC[2:0] = 011: 3 periods of BCLK;
OC[2:0] = 100: 4 periods of BCLK;
OC[2:0] = 101: 5 periods of BCLK;
OC[2:0] = 110: 6 periods of BCLK;
OC[2:0] = 111: 7 periods of BCLK.

GREG8: SLIC Ring Trip Setting and Control, Read/Write (27H/A7H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	0	0	1	1	1
I/O data	OPI	Reserved	IPI	IS	RTE	OS[2]	OS[1]	OS[0]

The Output Polarity Indicator bit (OPI) indicates the valid polarity of output:
OPI = 0: the selected output pin changes from low to high to activate the ring (default);
OPI = 1: the selected output pin changes from high to low to activate the ring.

The Input Polarity Indicator bit (IPI) indicates the valid polarity of input:
IPI = 0: active low (default);
IPI = 1: active high.

The Input Selection bit (IS) determines which input will be selected as the off-hook indication signal source.
IS = 0: SI1 is selected (default);
IS = 1: SI2 is selected.

The Ring Trip Enable bit (RTE) enables or disables the ring trip function block:
RTE = 0: the ring trip function block is disabled (default);
RTE = 1: the ring trip function block is enabled.

The Output Selection bits (OS[2:0]) determine which output will be selected as the ring control signal source.
OS[2:0] = 000 - 010: not defined;
OS[2:0] = 011: SB1 is selected (when SB1 is configured as an output);
OS[2:0] = 100: SB2 is selected (when SB2 is configured as an output);
OS[2:0] = 101: SB3 is selected (when SB3 is configured as an output);
OS[2:0] = 110: SO1 is selected;
OS[2:0] = 111: SO2 is selected.

GREG9: SI Data, Read Only (28H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	0	0	1	0	1	0	0	0
I/O data	SIB[3]	SIB[2]	SIB[1]	SIB[0]	SIA[3]	SIA[2]	SIA[1]	SIA[0]

The SIA[3:0] bits contain the debounced data (off-hook status) on the SI1 pins of Channel 4 to Channel 1 respectively.
The SIB[3:0] bits contain the debounced data (ground key status) on the SI2 pins of Channel 4 to Channel 1 respectively.

GREG10: SB1 Direction Control and SB1 Status/Control Data, Read/Write (29H/A9H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	0	1	0	0	1
I/O data	SB1C[3]	SB1C[2]	SB1C[1]	SB1C[0]	SB1[3]	SB1[2]	SB1[1]	SB1[0]

The SB1 direction control bits SB1C[3:0] in this register determine the directions of the SB1 pins of Channel 4 to Channel 1 respectively.
SB1C[0] = 0: the SB1 pin of Channel 1 is configured as input (default);
SB1C[0] = 1: the SB1 pin of Channel 1 is configured as output;
SB1C[1] = 0: the SB1 pin of Channel 2 is configured as input (default);
SB1C[1] = 1: the SB1 pin of Channel 2 is configured as output;
SB1C[2] = 0: the SB1 pin of Channel 3 is configured as input (default);
SB1C[2] = 1: the SB1 pin of Channel 3 is configured as output;
SB1C[3] = 0: the SB1 pin of Channel 4 is configured as input (default);
SB1C[3] = 1: the SB1 pin of Channel 4 is configured as output.

When the SB1 pins of Channel 1 to Channel 4 are configured as inputs, the SB1[0] to SB1[3] bits contain the status of these four SB1 pins respectively. When the SB1 pins of Channel 1 to Channel 4 are configured as outputs, the control data is written to these four SB1 pins via the SB1[0] to SB1[3] bits respectively.

GREG11: SB2 Direction Control and SB2 Status/Control Data, Read/Write (2AH/AAH)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	0	1	0	1	0
I/O data	SB2C[3]	SB2C[2]	SB2C[1]	SB2C[0]	SB2[3]	SB2[2]	SB2[1]	SB2[0]

The SB2 direction control bits SB2C[3:0] in this register determine the directions of the SB2 pins of Channel 4 to Channel 1 respectively.
SB2C[0] = 0: the SB2 pin of Channel 1 is configured as input (default);
SB2C[0] = 1: the SB2 pin of Channel 1 is configured as output;
SB2C[1] = 0: the SB2 pin of Channel 2 is configured as input (default);
SB2C[1] = 1: the SB2 pin of Channel 2 is configured as output;
SB2C[2] = 0: the SB2 pin of Channel 3 is configured as input (default);
SB2C[2] = 1: the SB2 pin of Channel 3 is configured as output;
SB2C[3] = 0: the SB2 pin of Channel 4 is configured as input (default);
SB2C[3] = 1: the SB2 pin of Channel 4 is configured as output.

When the SB2 pins of Channel 1 to Channel 4 are configured as inputs, the SB2[0] to SB2[3] bits contain the status of these four SB2 pins respectively. When the SB2 pins of Channel 1 to Channel 4 are configured as outputs, the control data is written to these four SB2 pins via the SB2[0] to SB2[3] bits respectively.

GREG12: SB3 Direction Control and SB3 Status/Control Data, Read/Write (2BH/ABH)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	0	1	0	1	1
I/O data	SB3C[3]	SB3C[2]	SB3C[1]	SB3C[0]	SB3[3]	SB3[2]	SB3[1]	SB3[0]

The SB3 direction control bits SB3C[3:0] in this register determine the directions of the SB3 pins of Channel 4 to Channel 1 respectively.
SB3C[0] = 0: the SB3 pin of Channel 1 is configured as input (default);
SB3C[0] = 1: the SB3 pin of Channel 1 is configured as output;
SB3C[1] = 0: the SB3 pin of Channel 2 is configured as input (default);
SB3C[1] = 1: the SB3 pin of Channel 2 is configured as output;
SB3C[2] = 0: the SB3 pin of Channel 3 is configured as input (default);
SB3C[2] = 1: the SB3 pin of Channel 3 is configured as output;
SB3C[3] = 0: the SB3 pin of Channel 4 is configured as input (default);
SB3C[3] = 1: the SB3 pin of Channel 4 is configured as output.

When the SB3 pins of Channel 1 to Channel 4 are configured as inputs, the SB3[0] to SB3[3] bits contain the status of these four SB3

pins respectively. When the SB3 pins of Channel 1 to Channel 4 are configured as outputs, the control data is written to these four SB3 pins via the SB3[0] to SB3[3] bits respectively.

GREG13: FSK Flag Length, Read/Write (2CH/ACH)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	0	1	1	0	0
I/O data	FL[7]	FL[6]	FL[5]	FL[4]	FL[3]	FL[2]	FL[1]	FL[0]

The flag signal is a stream of '1' which is transmitted between two message bytes during Caller-ID messages transmission. The Flag Length bits FL[7:0] determine the number of the flag bits. The flag length can be from 0 to 255 (d) bits. The default flag length is 0 (i.e. FL[7:0] = 00H), which means that no flag signal will be transmitted.

GREG14: FSK Data Length, Read/Write (2DH/ADH)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	0	1	1	0	1
I/O data	DL[7]	DL[6]	DL[5]	DL[4]	DL[3]	DL[2]	DL[1]	DL[0]

The Data Length bits DL[7:0] determine the number of the data bytes that will be transmitted except the flag signal. The data length can be from 0 to 64 (d) bytes. Any value larger than 64 (d) in this register will be taken as 64 (d) by the CODEC. The default data length is 0 (d), which means that no data bytes will be transmitted.

GREG15: FSK Seizure Length, Read/Write (2EH/AEH)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	0	1	1	1	0
I/O data	SL[7]	SL[6]	SL[5]	SL[4]	SL[3]	SL[2]	SL[1]	SL[0]

The Seizure Length is the number of '01' pairs that represent the seizure phase. The Seizure Length is two times of the value of the SL[7:0] bits. The value of the SL[7:0] bits can be from 0 to 255 (d), corresponding to Seizure Length of 0 to 510 (d). The default value is 0 (d), which means that no seizure signal will be transmitted.

GREG16: FSK Mark Length, Read/Write (2FH/AFH)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	0	1	1	1	1
I/O data	ML[7]	ML[6]	ML[5]	ML[4]	ML[3]	ML[2]	ML[1]	ML[0]

The Mark Length bits ML[7:0] determine the number of the mark bits of '1', which is transmitted in initial flag phase. The Mark Length can be from 0 to 255 (d). The default value is 0 (d), which means that no mark signal will be transmitted.

GREG17: FSK Start, Mark After Send, BT/Bellcore Selection, FSK Channel Selection and FSK On/Off, Read/Write (30H/B0H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	1	0	0	0	0
I/O data	Reserved		FCS[1]	FCS[0]	FO	BS	MAS	FS

The FSK Channel Select bits (FCS[1:0]) select a channel on which the FSK signal is generated.
FCS[1:0] = 00: Channel 1 is selected (default);
FCS[1:0] = 01: Channel 2 is selected;
FCS[1:0] = 10: Channel 3 is selected;
FCS[1:0] = 11: Channel 4 is selected.

The FSK On/Off bit (FO) enables or disables the FSK function block.
FO = 0: The FSK function block is disabled (default);

FO = 1: The FSK function block is enabled.

The BT/Bellcore Select bit (BS) determines which specification the IDT821054 will follow:
BS = 0: Bellcore specification is selected (default);
BS = 1: BT specification is selected.

The Mark After Send bit (MAS) determines if the FSK generator will keep on sending a mark-after-send signal (a stream of '1') after sending out all data in the FSK-RAM.
MAS = 0: The output will be muted after all data in the FSK-RAM has been sent out (default);
MAS = 1: The FSK generator keeps on sending out a mark-after-send signal after sending out all data in the FSK-RAM.
If the MAS bit is set to '0' and the FS bit is set to '1', the mark-after-send signal will be stopped.

The FSK Start bit (FS) should be set to '1' to start sending FSK signal. It will be automatically reset after all data in the FSK-RAM has been sent out. If the Seizure Length, Mark Length and Data Length are set to 0, the FS bit will be reset to '0' immediately after it is set to '1'.
FS = 0: FSK transmission is disabled (default);
FS = 1: FSK transmission starts.

GREG18: Level Meter Result Low Byte, Read Only (31H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	0	0	1	1	0	0	0	1
I/O data	LVLL[7]	LVLL[6]	LVLL[5]	LVLL[4]	LVLL[3]	LVLL[2]	LVLL[1]	LVLL[0]

This register contains the low byte of the level meter result. The default value is 00H.
The LVLL[0] bit in this register will be set to '1' when the level meter result (both high and low bytes) is ready, and it will be reset to '0' immediately after the high byte of result is read. To read the level meter result, it is recommended to the low byte first, then read the high byte (LVLH[7:0] in GREG19).

GREG19: Level Meter Result High Byte, Read Only (32H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	0	0	1	1	0	0	1	0
I/O data	LVLH[7]	LVLH[6]	LVLH[5]	LVLH[4]	LVLH[3]	LVLH[2]	LVLH[1]	LVLH[0]

This register contains the high byte of the level meter result. The default value is 00H.

GREG20: Level Meter Count Number, Read/Write (33H/B3H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	1	0	0	1	1
I/O data	CN[7]	CN[6]	CN[5]	CN[4]	CN[3]	CN[2]	CN[1]	CN[0]

The CN[7:0] bits are used to set the number of time cycles for sampling the PCM data.
CN[7:0] = 0 (d): the PCM data is output to the result registers GREG18 and GREG19 directly;
CN[7:0] = N (d): the PCM data is sampled for N × 125 μs (N is from 1 to 255).

GREG21: Level Meter Channel and Linear/Compressed Mode Selection, Level Meter On/Off, Read/Write (34H/B4H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	1	0	1	0	0
I/O data	Reserved				LMO	L/C	CS[1]	CS[0]

The Level Meter On/Off bit (LMO) enables/disables the level meter.
LMO = 0: The level meter is disabled (default);
LMO = 1: The level meter is enabled.

The Linear/Compressed bit (L/C) determines the mode of level meter operation.
L/C = 0: Message mode is selected. The compressed PCM data will be output to GREG19 transparently (default).
L/C = 1: Metering mode is selected. The linear PCM data will be metered and the result will be output to the registers GREG18 and GREG19.

The Level Meter Channel Select bits (CS[1:0]) select a channel, data on which will be level metered.
CS[1:0] = 00: Channel 1 is selected (default);
CS[1:0] = 01: Channel 2 is selected;
CS[1:0] = 10: Channel 3 is selected;
CS[1:0] = 11: Channel 4 is selected.

GREG22: Global Loopback Control and PLL Power Down, Read/Write (35H/B5H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	1	0	1	0	1
I/O data	Reserved		PPD	DLB_ANA	ALB_8k	DLB_8k	DLB_DI	ALB_DI

The PLL Power Down bit (PPD) controls the operation state of the PLL block.
PPD = 0: The PLL is disabled. The device is in normal operation state (default);
PPD = 1: The PLL is powered down. The device works in power-saving mode. All clocks stop running.

The Loop Control bits determine the loopback status. Refer to Figure - 4 on page 11 for detailed information.
DLB_ANA = 0: The Digital Loopback via Analog Interface is disabled (default);
DLB_ANA = 1: The Digital Loopback via Analog Interface is enabled.

ALB_8k = 0: The Analog Loopback via 8 kHz Interface is disabled (default);
ALB_8k = 1: The Analog Loopback via 8 kHz Interface is enabled.

DLB_8k = 0: The Digital Loopback via 8 kHz Interface is disabled (default);
DLB_8k = 1: The Digital Loopback via 8 kHz Interface is enabled.

DLB_DI = 0: The Digital Loopback from DR to DX is disabled (default);
DLB_DI = 1: The Digital Loopback from DR to DX is enabled.

ALB_DI = 0: The Analog Loopback from DX to DR is disabled (default);
ALB_DI = 1: The Analog Loopback from DX to DR is enabled.

GREG23: Over-sampling Timing Tuning, Read/Write (37H/B7H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	1	0	1	1	1

To improve the performance of total distortion, it is recommended to write a data byte of 40H to this register. The default value is 00H.

3.4.3 LOCAL REGISTERS LIST

LREG1: Coefficient Selection, Read/Write (00H/80H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	0	0	0	0	0	0
I/O data	CS[7]	CS[6]	CS[5]	CS[4]	CS[3]	CS[2]	CS[1]	CS[0]

The Coefficient Select bits (CS[7:0]) are used to control digital filters and function blocks on each channel. The digital filters include Impedance Matching Filter, Echo Cancellation Filter, High-Pass Filter, Gain for Impedance Scaling, Gain in the Transmit/Receive Path and Frequency Response Correction in the Transmit/Receive Path. See Figure - 4 on page 11 for details. It should be noted that the Impedance Matching Filter and Gain for Impedance Scaling are working together to adjust the impedance. So the CS[0] and CS[2] bits should be set to the same value to ensure proper operation.
CS [7] = 0: The Digital Gain Filter in the Receive path (GRX) is disabled (default);
CS [7] = 1: The Digital Gain in the Receive path (GRX) is programmed by the Coe-RAM.

CS [6] = 0: The Frequency Response Correction filter in the Receive path (FRR) is disabled (default);
CS [6] = 1: The coefficient of the Frequency Response Correction filter in the Receive path (FRR) is programmed by the Coe-RAM.

CS [5] = 0: The Digital Gain Filter in the Transmit path (GTX) is disabled (default);
CS [5] = 1: The Digital Gain in the Transmit path (GTX) is set by the Coe-RAM.

CS [4] = 0: The Frequency Response Correction filter in the Transmit path (FRX) is disabled (default);
CS [4] = 1: The coefficient of the Frequency Response Correction filter in the Transmit path (FRX) is programmed by the Coe-RAM.

CS [3] = 0: The High-Pass Filter (HPF) is bypassed/disabled;
CS [3] = 1: The High-Pass Filter (HPF) is enabled (default).

CS [2] = 0: The Gain for Impedance Scaling filter (GIS) is disabled (default);
CS [2] = 1: The coefficient of the Gain for Impedance Scaling filter (GIS) is programmed by the Coe-RAM.

CS [1] = 0: The Echo Cancellation Filter (ECF) is disabled (default);
CS [1] = 1: The coefficient of the Echo Cancellation Filter (ECF) is programmed by the Coe-RAM.

CS [0] = 0: The Impedance Matching Filter (IMF) is disabled (default);
CS [0] = 1: The coefficient of theImpedance Matching Filter (IMF) is programmed by the Coe-RAM.

LREG2: Local Loopback Control and SLIC Input Interrupt Enable, Read/Write (01H/81H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	0	0	0	0	0	1
I/O data	IE[4]	IE[3]	IE[2]	IE[1]	IE[0]	DLB_PCM	ALB_1BIT	DLB_1BIT

The SLIC Input Interrupt Enable bits IE[4:0] enable or disable the interrupt signal on each channel.
IE[4] = 0: Interrupt disabled. The interrupt generated by changes of SB3 (when SB3 is selected as an input) will be ignored (default);
IE[4] = 1: Interrupt enabled. The interrupt generated by changes of SB3 (when SB3 is selected as an input) will be recognized.

IE[3] = 0: Interrupt disabled. The interrupt generated by changes of SB2 (when SB2 is selected as an input) will be ignored (default);
IE[3] = 1: Interrupt enabled. The interrupt generated by changes of SB2 (when SB2 is selected as an input) will be recognized.

IE[2] = 0: Interrupt disabled. The interrupt generated by changes of SB1 (when SB1 is selected as an input) will be ignored (default);
IE[2] = 1: Interrupt enabled. The interrupt generated by changes of SB1 (when SB1 is selected as an input) will be recognized.

IE[1] = 0: Interrupt disabled. The interrupt generated by changes of SI2 will be ignored (default);
IE[1] = 1: Interrupt enabled. The interrupt generated by changes of SI2 will be recognized.

IE[0] = 0: Interrupt disabled. The interrupt generated by changes of SI1 will be ignored (default);

IE[0] = 1: Interrupt enabled. The interrupt generated by changes of SI1 will be recognized.

The Loopback Control Bits (DLB_PCM, ALB_1BIT and DLB_1BIT) determine the loopback status on the corresponding channel. Refer to Figure - 4 on page 11 for details.
DLB_PCM = 0: Digital Loopback via Time Slots on the corresponding channel is disabled (default);
DLB_PCM = 1: Digital Loopback via Time Slots on the corresponding channel is enabled.

ALB_1BIT = 0: Analog Loopback via Onebit on the corresponding channel is disabled (default);
ALB_1BIT = 1: Analog Loopback via Onebit on the corresponding channel is enabled;

DLB_1BIT = 0: Digital Loopback via Onebit on the corresponding channel is disabled (default);
DLB_1BIT = 1: Digital loopback via Onebit on the corresponding channel is enabled;

LREG3: DSH and GK Debounce Filters Configuration, Read/Write (02H/82H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	0	0	0	0	1	0
I/O data	GK[3]	GK[2]	GK[1]	GK[0]	DSH[3]	DSH[2]	DSH[1]	DSH[0]

The DSH Debounce bits DSH[3:0] are used to set the debounce time of SI1 input of the corresponding channel.
DSH[3:0] = 0000: The debounce time is 0 ms (default);
DSH[3:0] = 0001: The debounce time is 2 ms;
DSH[3:0] = 0010: The debounce time is 4 ms;
DSH[3:0] = 0011: The debounce time is 6 ms;
DSH[3:0] = 0100: The debounce time is 8 ms;
DSH[3:0] = 0101: The debounce time is 10 ms;
DSH[3:0] = 0110: The debounce time is 12 ms;
DSH[3:0] = 0111: The debounce time is 14 ms;
DSH[3:0] = 1000: The debounce time is 16 ms;
DSH[3:0] = 1001: The debounce time is 18 ms;
DSH[3:0] = 1010: The debounce time is 20 ms;
DSH[3:0] = 1011: The debounce time is 22 ms;
DSH[3:0] = 1100: The debounce time is 24 ms;
DSH[3:0] = 1101: The debounce time is 26 ms;
DSH[3:0] = 1110: The debounce time is 28 ms;
DSH[3:0] = 1111: The debounce time is 30 ms.

The GK Debounce bits GK[3:0] are used to set the debounce interval of SI2 input of the corresponding channel. The debounce interval is programmable from 0 to 30 ms, corresponding to the minimal debounce time of 0 to 180 ms.
GK[3:0] = 0000: The debounce interval is 0 ms (default);
GK[3:0] = 0001: The debounce interval is 2 ms;
GK[3:0] = 0010: The debounce interval is 4 ms;
GK[3:0] = 0011: The debounce interval is 6 ms;
GK[3:0] = 0100: The debounce interval is 8 ms;
GK[3:0] = 0101: The debounce interval is 10 ms;
GK[3:0] = 0110: The debounce interval is 12 ms;
GK[3:0] = 0111: The debounce interval is 14 ms;
GK[3:0] = 1000: The debounce interval is 16 ms;
GK[3:0] = 1001: The debounce interval is 18 ms;
GK[3:0] = 1010: The debounce interval is 20 ms;
GK[3:0] = 1011: The debounce interval is 22 ms;
GK[3:0] = 1100: The debounce interval is 24 ms;
GK[3:0] = 1101: The debounce interval is 26 ms;
GK[3:0] = 1110: The debounce interval is 28 ms;
GK[3:0] = 1111: The debounce interval is 30 ms;

LREG4: Channel I/O Data, Read/Write (03H/83H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	0	0	0	0	1	1
I/O data	Reserved	SO2	SO1	SB3	SB2	SB1	SI2	SI1

The Channel I/O Data bits contain the information of the SLIC I/O pins (SI1, SI2, SB1, SB2, SB3, SO1 and SO2) of the corresponding channel.
If SB1, SB2 and SB3 are configured as outputs, data can only be written to them by global registers GREG10, GREG11 and GREG12 respectively, and not by this register.

LREG5: Transmit Timeslot and Transmit Highway Selection, Read/Write (04H/84H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	0	0	0	1	0	0
I/O data	THS	TT[6]	TT[5]	TT[4]	TT[3]	TT[2]	TT[1]	TT[0]

The Transmit Time Slot Bits TT[6:0] select a time slot (compressed code) or a time slot group (linear code) for the corresponding channel to transmit the PCM data. The valid value is from 0 to 127(d), corresponding to TS0 to TS127. The default value is 0 (d).

The Transmit Highway Selection bit THS selects a PCM highway for the corresponding channel to transmit the PCM data.
THS = 0: DX1 is selected (default);
THS = 1: DX2 is selected.

LREG6: Receive Timeslot and Receive PCM Highway Selection, Read/Write (05H/85H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	0	0	0	1	0	1
I/O data	RHS	RT[6]	RT[5]	RT[4]	RT[3]	RT[2]	RT[1]	RT[0]

The Receive Time Slot Bits RT[6:0] select a time slot (compressed code) or a time slot group (linear code) for the corresponding channel to receive the PCM data. The valid value is from 0 to 127(d), corresponding to TS0 to TS127. The default value is 0 (d).

The Receive Highway Selection bit RHS selects a PCM highway for the corresponding channel to receive the PCM data.
RHS = 0: DR1 is selected (default);
RHS = 1: DR2 is selected.

LREG7: PCM Data Low Byte, Read Only (06H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	0	0	0	0	0	1	1	0
I/O data	PCM[7]	PCM[6]	PCM[5]	PCM[4]	PCM[3]	PCM[2]	PCM[1]	PCM[0]

This register is used for MCU to monitor the transmit (A to D) PCM data. For linear code, this register contains the low byte of the transmit PCM data and LREG8 contains the high byte of the transmit PCM data. For compressed code (A/μ-Law), this register contains total 8 bits of the transmit PCM data.
The low byte or total 8 bits of transmit PCM data will be read out by applying a read command to this register, and at the same time, it will be transmitted to the PCM highway without any interference.

LREG8: PCM Data High Byte, Read Only (07H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	0	0	0	0	0	1	1	1
I/O data	PCM[15]	PCM[14]	PCM[13]	PCM[12]	PCM[11]	PCM[10]	PCM[9]	PCM[8]

This register is used for MCU to monitor the transmit (A to D) PCM data. For linear code, this register contains the high byte of the

transmit PCM data. For compressed code (A/μ-Law), this register is not used (when being read, it will output a data byte of 00H).
The high byte of transmit PCM data will be read out by applying a read command to this register, and at the same time, it will be transmitted to the PCM highway without any interference.

LREG9: A/D Gain, D/A Gain, Channel Power Down and PCM Receive Path Cutoff, Read/Write (08H/88H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	0	0	1	0	0	0
I/O data	PD	PCMCT	GAD	GDA	0	0	0	0

The Channel Power Down bit (PD) selects the operation mode for the corresponding channel:
PD = 0: The corresponding channel is in normal operation state;
PD = 1: The corresponding channel is powered down (default).

The PCMCT bit determines the operation of PCM Receive Path of the corresponding channel:
PCMCT = 0: The PCM Receive Path of the corresponding channel is in normal operation state (default);
PCMCT = 1: The PCM Receive Path of the corresponding channel is cut off.

The A/D Gain bit (GAD) sets the gain of analog A/D for the corresponding channel:
GAD = 0: 0 dB (default);
GAD = 1: +6 dB.

The D/A Gain bit (GDA) sets the gain of analog D/A for the corresponding channel:
GDA = 0: 0 dB (default);
GDA = 1: -6 dB.

Attention: To ensure proper operation, the lower 4 bits of the I/O data byte following the write command (88H) must be '0000'.

LREG10: Tone Generator Enable, Read/Write (09H/89H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	0	0	1	0	0	1
I/O data	Reserved				1	1	TEN1	TEN0

TEN1 = 0: Tone generator 1 is disabled (default);
TEN1 = 1: Tone generator 1 is enabled.

TEN0 = 0: Tone generator 0 is disabled (default);
TEN0 = 1: Tone generator 0 is enabled.

Attention: To ensure proper operation, the b3 and b2 of the I/O data byte following the write command (89H) must be ‘11’.

4 ABSOLUTE MAXIMUM RATINGS

Ratings	Min.	Max.	Unit
Power supply voltage		6.5	V
Voltage on Any Pin with respect to ground	-0.5	5.5	V
Package power dissipation		1.5	W
Storage temperature	-65	+150	°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

5 RECOMMENDED DC OPERATING CONDITIONS

Parameter	Min.	Max.	Unit
Operating temperature	–40	+85	°C
Power supply voltage	4.75	5.25	V

Note: MCLK: 1.536 MHz, 1.544 MHz, 2.048 MHz, 3.072 MHz, 3.088 MHz, 4.096 MHz, 6.144 MHz, 6.176 MHz or 8.192 MHz with tolerance of ± 50 ppm.

6 ELECTRICAL CHARACTERISTICS

6.1 DIGITAL INTERFACE

Parameter	Description	Min.	Typ.	Max.	Units	Test Conditions
V_{IL}	Input low voltage			0.8	V	All digital inputs
V_{IH}	Input high voltage	2.0			V	All digital inputs
V_{OL}	Output low voltage			0.8	V	DX, I_L = 8 mA, All other digital outputs, I_L = 4 mA
V_{OH}	Output high voltage	VDD – 0.6			V	DX, I_L = –8 mA, All other digital outputs, I_L = –4 mA
I_I	Input current	–10		10	µA	All digital inputs, GND<VIN<VDD
I_{OZ}	Output current in high-impedance state	–10		10	µA	DX
C_I	Input capacitance			5	pF	

6.2 POWER DISSIPATION

Parameter	Description	Min.	Typ.	Max.	Units	Test Conditions
I_{DD1}	Operating current		50		mA	All channels are active.
I_{DD0}	Standby current			6	mA	All channels are powered down, with MCLK present.

Note: Power measurements are made at MCLK = 2.048MHz, outputs unloaded.

6.3 ANALOG INTERFACE

Parameter	Description	Min.	Typ.	Max.	Units	Test Conditions
V_{OUT1}	Output voltage, VOUT	2.25	2.4	2.6	V	Alternating ±zero, μ-law PCM code applied to DR
V_{OUT2}	Output voltage swing, VOUT	3.25			Vp-p	R_L = 300 Ω
R_I	Input resistance, VIN	30	40	60	kΩ	0.25 V < VIN < 4.75 V
R_O	Output resistance, VOUT			20	Ω	0 dBm0, 1020 Hz PCM code applied to DR
R_L	Load resistance, VOUT	300			Ω	External loading
C_L	Load capacitance, VOUT			100	pF	External loading

7 TRANSMISSION CHARACTERISTICS

0 dBm0 is defined as 0.775 Vrms for A-law and 0.769 Vrms for μ-law, both for 600 Ω load. Unless otherwise noted, the analog input is a 0 dBm0, 1020 Hz sine wave; the input amplifier is set for unity gain. The digital input is a PCM bit stream equivalent to that obtained by passing a 0 dBm0, 1020 Hz sine wave through an ideal encoder. The output level is sin(x)/x-corrected. Typical values are for V_{DD} = +5 V and T_A = 25°C.

7.1 ABSOLUTE GAIN

Parameter	Description	Min.	Typ.	Max.	Units	Test Conditions
G_{XA}	Transmit gain, absolute	–0.25		0.25	dB	Signal output of 0 dBm0, μ-law or A-law
G_{RA}	Receive gain, absolute	–0.25		0.25	dB	Measured relative to 0 dBm0, μ-law or A-law, PCM input of 0 dBm0, 1020 Hz. R_L = 10 kΩ.

7.2 GAIN TRACKING

Parameter	Description	Min.	Typ.	Max.	Units	Test Conditions
G_{TX}	Transmit gain tracking					Tested by sinusoidal method, A-law or μ-law.
	+3 dBm0 to –37 dBm0 (exclude –37 dBm0)	–0.25		0.25	dB	
	–37 dBm0 to –50 dBm0 (exclude –50 dBm0)	–0.50		0.50	dB	
	–50 dBm0 to –55 dBm0	–1.40		1.40	dB	
G_{TR}	Receive gain tracking					Tested by sinusoidal method, A-law or μ-law.
	+3 dBm0 to –40 dBm0 (exclude –40 dBm0)	–0.10		0.10	dB	
	–40 dBm0 to –50 dBm0 (exclude –50 dBm0)	–0.25		0.50	dB	
	–50 dBm0 to –55 dBm0	–0.50		0.50	dB	

7.3 FREQUENCY RESPONSE

Parameter	Description	Min.	Typ.	Max.	Units	Test Conditions
G_{XR}	Transmit gain, relative to G_{XA}					The high-pass filter is enabled.
	f = 50 Hz			–30	dB	
	f = 60 Hz			–30	dB	
	f = 300 Hz	–0.10		0.20	dB	
	f = 300 to 3000 Hz (exclude 3000 Hz)	–0.15		0.15	dB	
	f = 3000 Hz to 3400 Hz	–0.60		0.15	dB	
	f = 3600 Hz			–0.10	dB	
	f ≥ 4600 Hz			–35	dB	
G_{RR}	Receive gain, relative to G_{RA}					
	f < 300 Hz			0	dB	
	f = 300 to 3000 Hz (exclude 3000 Hz)	–0.15		0.15	dB	
	f = 3000 Hz to 3400 Hz	–0.60		0.15	dB	
	f = 3600 Hz			–0.20	dB	
	f ≥ 4600 Hz			–35	dB	

7.4 GROUP DELAY

Parameter	Description	Min.	Typ.	Max.	Units	Test Conditions
D_{XR}	Transmit delay, relative to 1800 Hz f = 500 to 600 Hz f = 600 to 1000 Hz f = 1000 to 2600 Hz f = 2600 to 2800 Hz			 280 150 80 280	 µs µs µs µs	
D_{RR}	Receive delay, relative to 1800 Hz f = 500 to 600 Hz f = 600 to 1000 Hz f = 1000 to 2600 Hz f = 2600 to 2800 Hz			 50 80 120 150	 µs µs µs µs	

7.5 DISTORTION

Parameter	Description	Min.	Typ.	Max.	Units	Test Conditions
STD_X	Transmit signal to total distortion ratio A-law: input level = 0 dBm0 input level = –30 dBm0 input level = –40 dBm0 input level = –45 dBm0 µ-law: input level = 0 dBm0 input level = –30 dBm0 input level = –40 dBm0 input level = –45 dBm0	 36 36 30 24 36 36 31 27			 dB dB dB dB dB dB dB dB	ITU-T O.132 Sine wave method, psophometrically weighted for A-law and C-message weighted for µ-law.
STD_R	Receive signal to total distortion ratio A-law: input level = 0 dBm0 input level = –30 dBm0 input level = –40 dBm0 input level = –45 dBm0 µ-law: input level = 0 dBm0 input level = –30 dBm0 input level = –40 dBm0 input level = –45 dBm0	 36 36 30 24 36 36 31 27			 dB dB dB dB dB dB dB dB	ITU-T O.132 Sine wave method, psophometrically weighted for A-law and C-message weighted for µ-law.
SFD_X	Single frequency distortion, transmit			–42	dBm0	200 to 3400 Hz, 0 dBm0 input, output any other single frequency ≤ 3400 Hz
SFD_R	Single frequency distortion, receive			–42	dBm0	200 to 3400 Hz, 0 dBm0 input, output any other single frequency ≤ 3400 Hz
IMD	Intermodulation distortion			–42	dBm0	Transmit or receive, two frequencies in the range of 300 to 3400 Hz at –6 dBm0

7.6 NOISE

Parameter	Description	Min.	Typ.	Max.	Units	Test Conditions
N_{XC}	Transmit noise, C-message weighted for µ-law			15	dBrnC0	
N_{XP}	Transmit noise, psophometrically weighted for A-law			–70	dBm0p	
N_{RC}	Receive noise, C-message weighted for µ-law			10	dBrnC0	
N_{RP}	Receive noise, psophometrically weighted for A-law			–80	dBm0p	
N_{RS}	Noise, single frequency f = 0 kHz to 100 kHz			–53	dBm0	VIN = 0 Vrms, tested at VOUT
PSR_X	Power supply rejection, transmit f = 300 Hz to 3.4 kHz f = 3.4 kHz to 20 kHz	 40 25			 dB dB	VDD = 5.0 VDC+100 mVrms
PSR_R	Power supply rejection, receive f = 300 Hz to 3.4 kHz f = 3.4 kHz to 20 kHz	 40 25			 dB dB	VDD = 5.0 VDC+100 mVrms, PCM code is positive one LSB
SOS	Spurious out-of-band signals at VOUT, relative to input PCM code applied: f = 4.6 kHz to 20 kHz f = 20 kHz to 50 kHz			 –40 –30	 dB dB	0 dBm0, 300 Hz to 3400 Hz input

7.7 INTERCHANNEL CROSSTALK

Parameter	Description	Min.	Typ.	Max.	Units	Test Conditions
XT_{X-R}	Transmit to receive crosstalk		–85	–78	dB	300 Hz to 3400 Hz, 0 dBm0 signal into VIN of the interfering channel. Idle PCM code into the channel under test.
XT_{R-X}	Receive to transmit crosstalk		–85	–80	dB	300 Hz to 3400 Hz, 0 dBm0 PCM code into the interfering channel. VIN = 0 Vrms for the channel under test.
XT_{X-X}	Transmit to transmit crosstalk		–85	–78	dB	300 Hz to 3400 Hz, 0 dBm0 signal into VIN of the interfering channel. VIN = 0 Vrms for the channel under test.
XT_{R-R}	Receive to receive crosstalk		–85	–80	dB	300 Hz to 3400 Hz, 0 dBm0 PCM code into the interfering channel. Idle PCM code into the channel under test.

7.8 INTRACHANNEL CROSSTALK

Parameter	Description	Min.	Typ.	Max.	Units	Test Conditions
XT_{X-R}	Transmit to receive crosstalk		–80	–70	dB	300 Hz to 3400 Hz, 0 dBm0 signal into VIN. Idle PCM code into DR.
XT_{R-X}	Receive to transmit crosstalk		–80	–70	dB	300 Hz to 3400 Hz, 0 dBm0 PCM code into DR. VIN = 0 Vrms.

Note: Crosstalk into transmit channels (VIN) can be significantly affected by parasitic capacitive coupling from VOUT outputs. PCB layouts should be arranged to minimize the parasitics.

8 TIMING CHARACTERISTICS

8.1 CLOCK TIMING

Symbol	Description	Min.	Typ.	Max.	Units	Test Conditions
t1	CCLK period	122		100k	ns	
t2	CCLK pulse width	48			ns	
t3	CCLK rise and fall time			25	ns	
t4	BCLK period	122			ns	
t5	BCLK pulse width	48			ns	
t6	BCLK rise and fall time			15	ns	
t7	MCLK pulse width	48			ns	
t8	MCLK rise and fall time			15	ns	

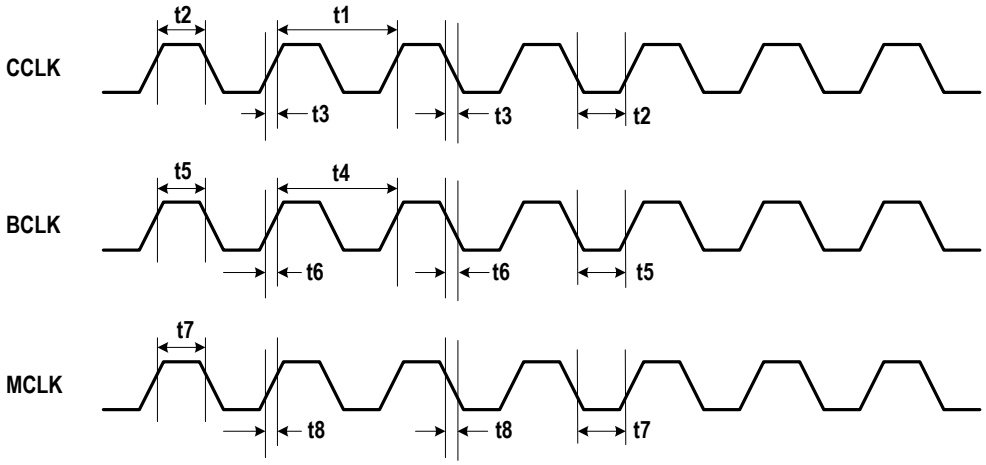


Figure - 8 Clock Timing

8.2 MICROPROCESSOR INTERFACE TIMING

Symbol	Description	Min.	Typ.	Max.	Units	Test Conditions
t11	$\overline{CS}$ setup time	15			ns	
t12	$\overline{CS}$ pulse width		8 * n * t1 (n ≥ 2)		ns	
t13	$\overline{CS}$ off time	250			ns	
t14	Input data setup time	30			ns	
t15	Input data hold time	30			ns	
t16	SLIC output latch valid			1000	ns	
t17	Output data turn on delay			50	ns	
t18	Output data hold time	0			ns	
t19	Output data turn off delay			50	ns	
t20	output data valid	0		50	ns	

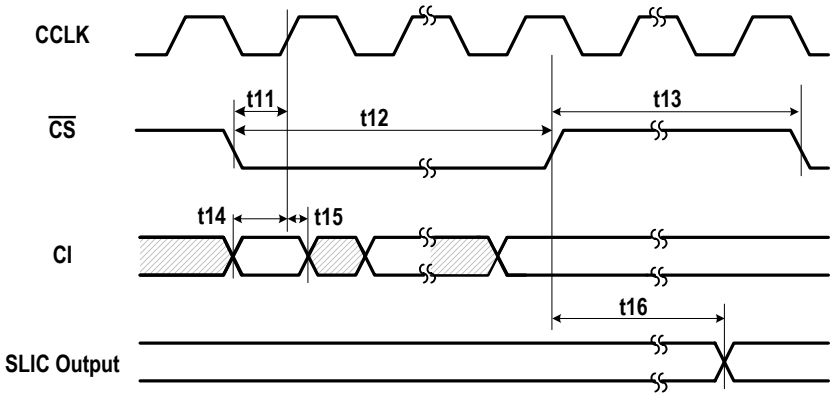


Figure - 9 MPI Input Timing

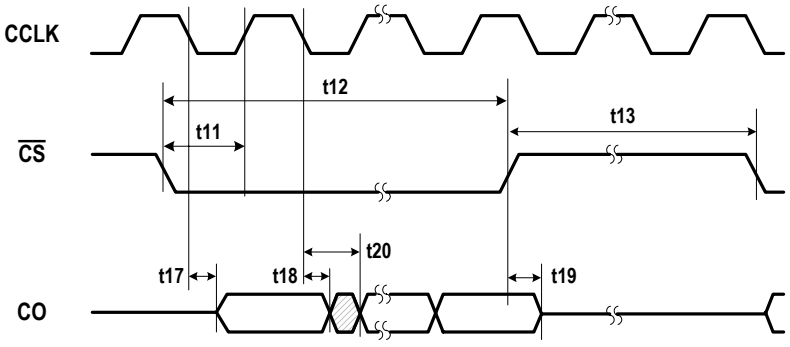
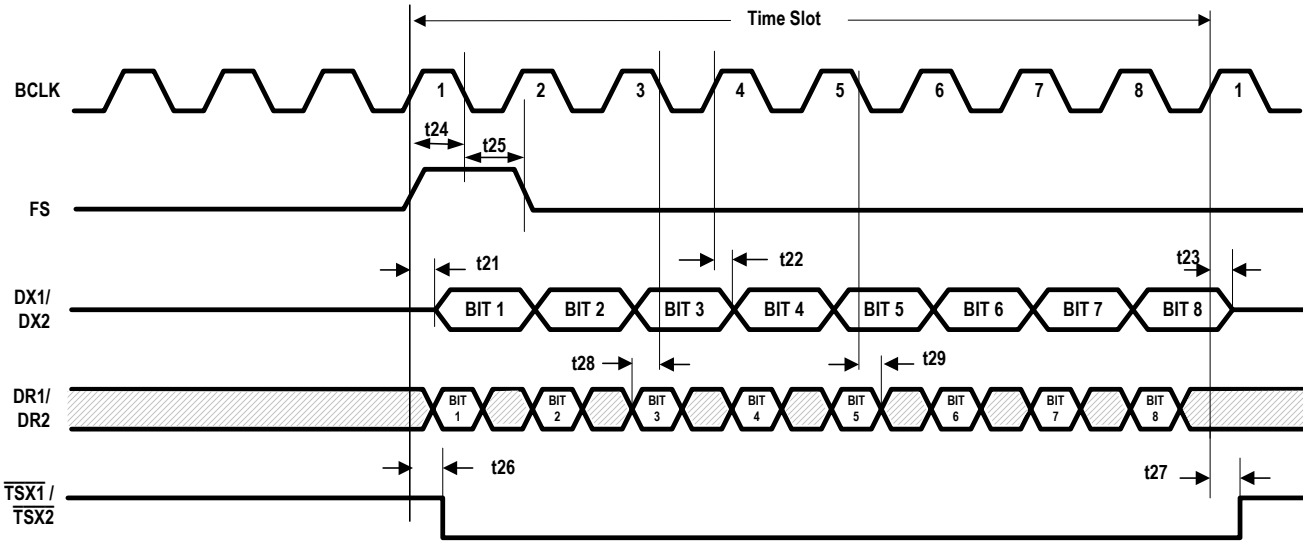


Figure - 10 MPI Output Timing

8.3 PCM INTERFACE TIMING

Symbol	Description	Min.	Typ.	Max.	Units	Test Conditions
t21	Data enable delay time	5		70	ns	
t22	Data delay time from BCLK	5		70	ns	
t23	Data float delay time	5		70	ns	
t24	Frame sync setup time	25		t4 – 50	ns	
t25	Frame sync hold time	50			ns	
t26	$\overline{TSX1}$ or $\overline{TSX2}$ enable delay time	5		80	ns	
t27	$\overline{TSX1}$ or $\overline{TSX2}$ disable delay time	5		80	ns	
t28	Receive data setup time	25			ns	
t29	Receive data hold time	5			ns	



Note: This timing diagram only applies to the situation of receiving data on falling edges and transmitting data on rising edges.

Figure - 11 Transmit and Receive Timing

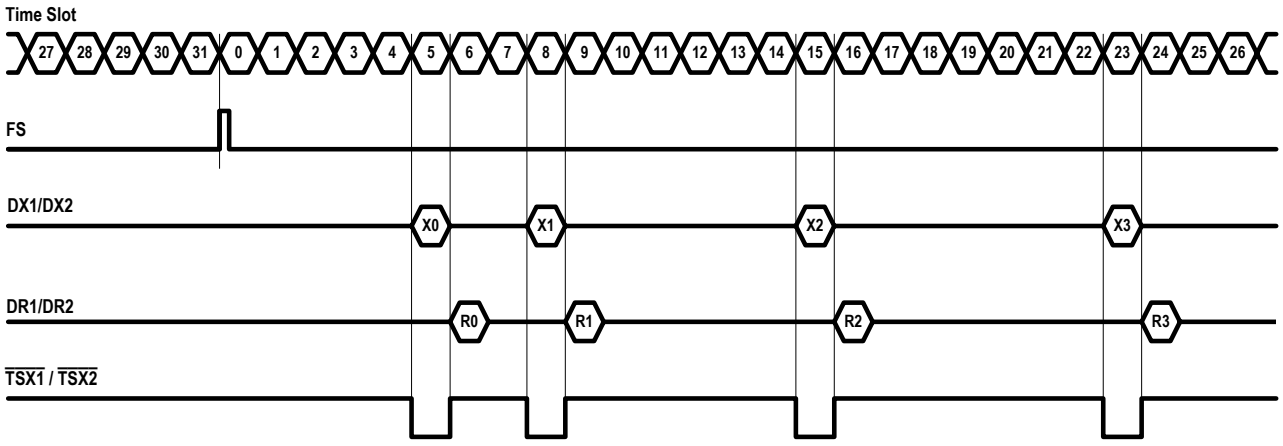


Figure - 12 Typical Frame Sync Timing (2 MHz Operation)

9 APPENDIX: IDT821054 COE-RAM MAPPING

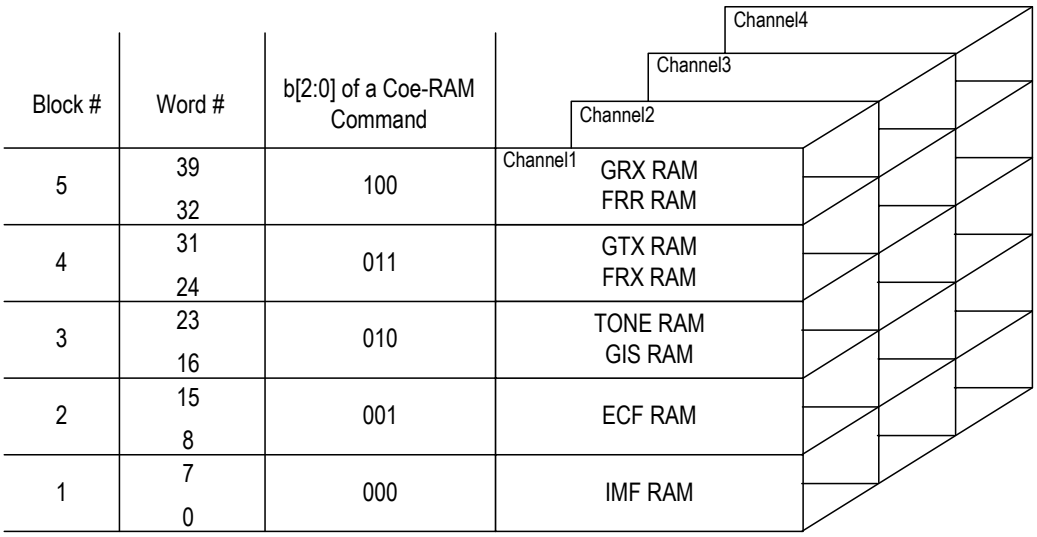


Figure - 13 Coe-RAM Mapping

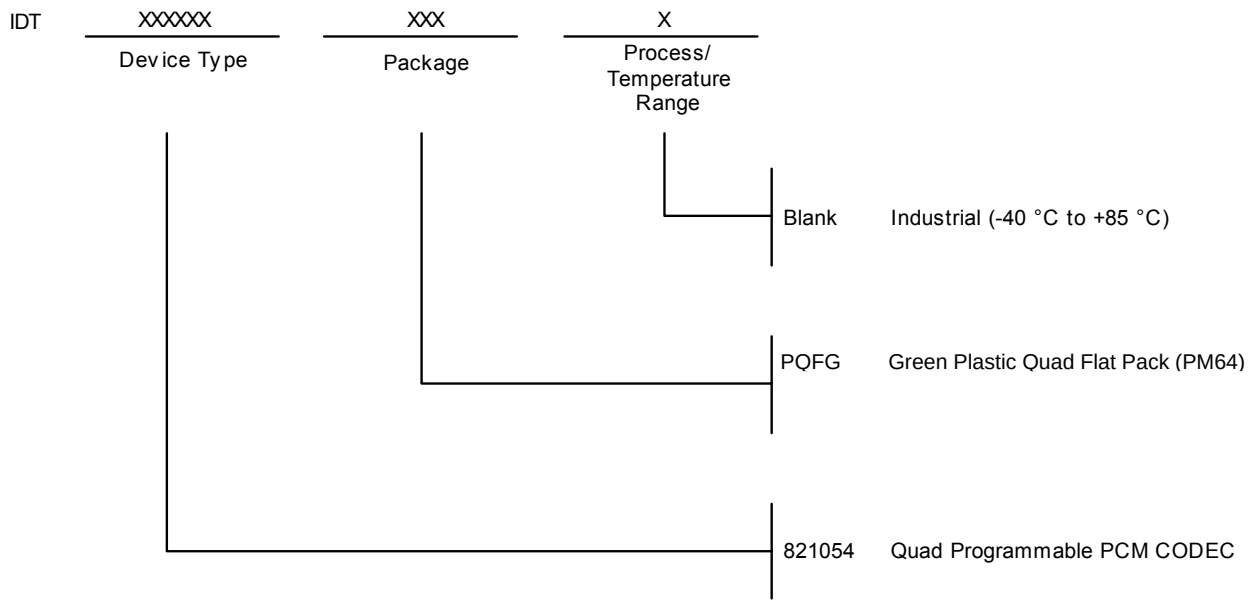
Generally, 6 bits of address are needed to locate each word of the 40 Coe-RAM words. In the IDT821054, the 40 words of Coe-RAM are divided into 5 blocks with 8 words per block, so, only 3 address bits are needed to locate each of the block. When the address of a Coe-RAM block (b[2:0]) is specified in a Coe-RAM command, all 8 words of this block will be addressed automatically, with the highest order word first (The IDT821054 will count down from '111' to '000' so that it accesses the 8 words successively). Refer to "3.1.4 Addressing the Coe-RAM" for details.

The address assignment for the 40 words of Coe-RAM is as shown in Table - 5. The number in the "Address" column is the actual address of each Coe-RAM word. As the IDT821054 handles the lower 3 bits of address automatically, only the higher 3 bits of address (in bold style) are needed for a Coe-RAM Command. It should be noted that, when addressing the GRX RAM, the FRR RAM will be addressed at the same time.

Table - 5 Coe-RAM Address Allocation

Block #	Word #	Address	Function	Block #	Word #	Address	Function
5	39	**100**,111	GRX RAM	3	19	**010**,011	GIS RAM
	38	**100**,110	FRR RAM		18	**010**,010	
	37	**100**,101			17	**010**,001	
	36	**100**,100			16	**010**,000	
	35	**100**,011		2	15	**001**,111	ECF RAM
	34	**100**,010			14	**001**,110	
	33	**100**,001			13	**001**,101	
	32	**100**,000			12	**001**,100	
4	31	**011**,111	GTX RAM		11	**001**,011	
	30	**011**,110	FRX RAM		10	**001**,010	
	29	**011**,101			9	**001**,001	
	28	**011**,100			8	**001**,000	
	27	**011**,011		1	7	**000**,111	IMF RAM
	26	**011**,010			6	**000**,110	
	25	**011**,001			5	**000**,101	
	24	**011**,000			4	**000**,100	
3	23	**010**,111	Amplitude Coefficient of Tone Generator 1		3	**000**,011	
	22	**010**,110	Frequency Coefficient of Tone Generator 1		2	**000**,010	
	21	**010**,101	Amplitude Coefficient of Tone Generator 0		1	**000**,001	
	20	**010**,100	Frequency Coefficient of Tone Generator 0		0	**000**,000	

10 ORDERING INFORMATION



DATA SHEET DOCUMENT HISTORY

12/21/2001	pgs. 8, 22, 26, 27
01/03/2002	pg. 24
01/23/2002	pgs. 1, 2, 5, 7, 11, 15, 21
02/19/2002	pg. 27
10/30/2002	pgs. 14, 21, 22, 25, 27
01/10/2003	pgs. 8, 11, 16, 23, 44
02/20/2003	pg. 37
02/26/2003	pg. 13
09/24/2014	pg. 44 Replaced leaded with lead-free device

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