

LOW SKEW, 1-TO-16, LVCMOS/LVTTL FANOUT BUFFER W/1.2V LVCMOS OUTPUTS

ICS8316

GENERAL DESCRIPTION

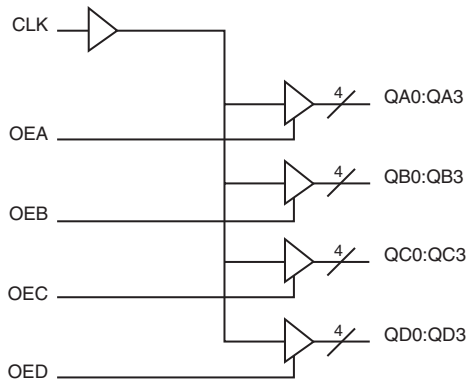
The ICS8316 is a low skew, 1-to-16 LVCMOS/LVTTL Fanout Buffer with 1.2V LVCMOS Outputs and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The ICS8316 single ended clock input accepts LVCMOS or LVTTL input levels. The low impedance LVCMOS outputs are designed to drive 50Ω series or parallel terminated transmission lines.

Guaranteed output and part-to-part skew characteristics along with the 1.2V output makes the ICS8316 ideal for high performance, single ended applications that also require a limited output voltage.

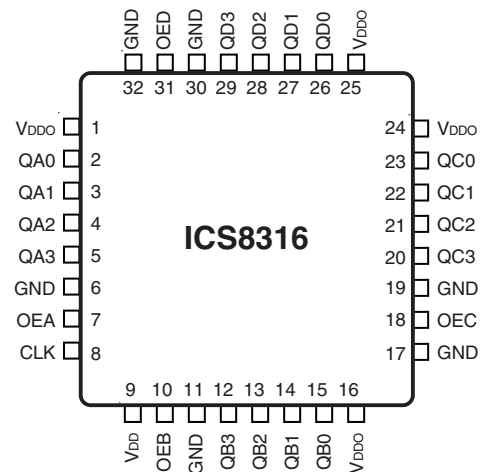
FEATURES

- Sixteen 1.2V LVCMOS / LVTTL outputs
- LVCMOS / LVTTL clock input
- Maximum output frequency: 150MHz
- Output skew: 380ps (maximum)
- Propagation delay: 4.6ns (maximum)
- 3.3V core/1.2V output operating supply mode
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request

BLOCK DIAGRAM



PIN ASSIGNMENT



32-Lead VFQFN
5mm x 5mm x 0.925 package body
K Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 16, 24, 25	V _{DDO}	Power		Output supply pins.
2, 3, 4, 5	QA0, QA1, QA2, QA3	Output		Bank A clock outputs. LVCMOS / LVTTL interface levels.
6, 11, 17, 19, 30, 32	GND	Power		Power supply ground.
7	OEA	Input	Pullup	Bank A output enable pin. Controls enabling and disabling of QA0:QA3 outputs. LVCMOS / LVTTL interface levels.
8	CLK	Input	Pulldown	Clock input. LVCMOS / LVTTL interface levels.
9	V _{DD}	Power		Power supply pin.
10	OEB	Input	Pullup	Bank B output enable pin. Controls enabling and disabling of QB0:QB3 outputs. LVCMOS / LVTTL interface levels.
12, 13, 14, 15	QB3, QB2, QB1, QB0	Output		Bank B clock outputs. LVCMOS / LVTTL interface levels.
18	OEC	Input	Pullup	Bank C output enable pin. Controls enabling and disabling of QC0:QC3 outputs. LVCMOS / LVTTL interface levels.
20, 21, 22, 23	QC3, QC2, QC1, QC0	Output		Bank C clock outputs. LVCMOS / LVTTL interface levels.
26, 27, 28, 29	QD0, QD1, QD2, QD3	Output		Bank D clock outputs. LVCMOS / LVTTL interface levels.
31	OED	Input	Pullup	Bank D output enable pin. Controls enabling and disabling of QD0:QD3 outputs. LVCMOS / LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance			4		pF
C _{PD}	Power Dissipation Capacitance (per output)	V _{DDO} = 1.26V			15	pF
R _{PULLUP}	Input Pullup Resistor			51		kΩ
R _{PULLDOWN}	Input Pulldown Resistor			51		kΩ
R _{OUT}	Output Impedance	V _{DDO} = 1.2 ± 5%	8	13	21	Ω

TABLE 3A. OUTPUT ENABLE AND CLOCK ENABLE FUNCTION TABLE

Control Inputs	Outputs
OE[A:D]	Qx0:Qx3
0	Hi-Z
1	Active

TABLE 3B. CLOCK INPUT FUNCTION TABLE

Inputs		Outputs
OE[A:D]	CLK	Qx0:Qx3
1	0	LOW
1	1	HIGH

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to $V_{DD} + 0.5V$
Outputs, V_O	-0.5V to $V_{DDO} + 0.5V$
Package Thermal Impedance, θ_{JA}	34.8°C/W (0 lfm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = 3.3V$, $V_{DDO} = 1.2V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		1.14	1.2	1.26	V
I_{DD}	Power Supply Current				10	μA
I_{DDO}	Output Supply Current				10	μA

TABLE 4B. LVCMOS DC CHARACTERISTICS, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IH}	Input High Current	CLK	$V_{DD} = V_{IN} = 3.465V$		150	μA
		OEA:OED	$V_{DD} = V_{IN} = 3.465V$		5	μA
I_{IL}	Input Low Current	CLK	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-5		μA
		OEA:OED	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-150		μA
V_{OH}	Output High Voltage	$V_{DDO} = 1.2V \pm 5\%$; NOTE 1	$V_{DDO} * 0.7$			V
V_{OL}	Output Low Voltage	$V_{DDO} = 1.2V \pm 5\%$; NOTE 1			$V_{DDO} * 0.3$	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}/2$. See Parameter Measurement section, "Load Test Circuit" diagram.

TABLE 5. AC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 1.2V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				150	MHz
tp_{LH}	Propagation Delay Low to High; NOTE 1		2.3	3.45	4.6	ns
$tsk(o)$	Output Skew; NOTE 2, 3				380	ps
$tsk(b)$	Bank Skew; NOTE 3, 4				70	ps
$tsk(pp)$	Part-to-Part Skew; NOTE 3, 5				1.2	ns
t_r/t_f	Output Rise Time	20% to 80%	350		850	ps
odc	Output Duty Cycle	$F_{out} \leq 100MHz$	47		53	%

All parameters measured at f_{MAX} unless noted otherwise.

NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.

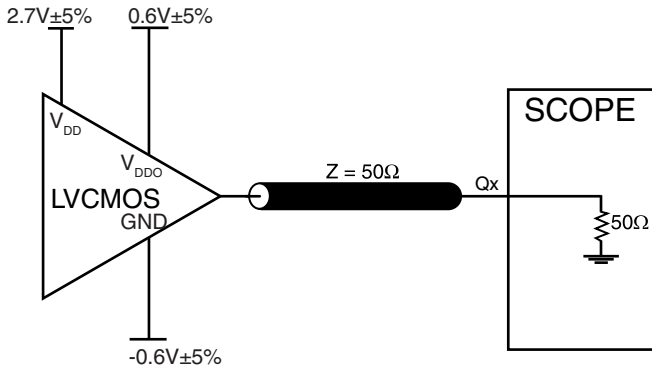
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

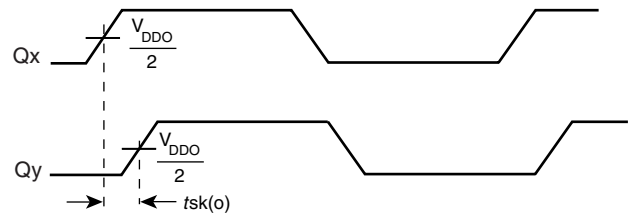
NOTE 4: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.

NOTE 5: Defined as the skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.

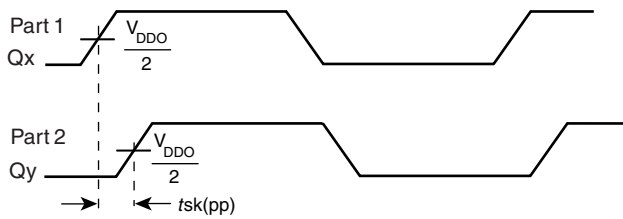
PARAMETER MEASUREMENT INFORMATION



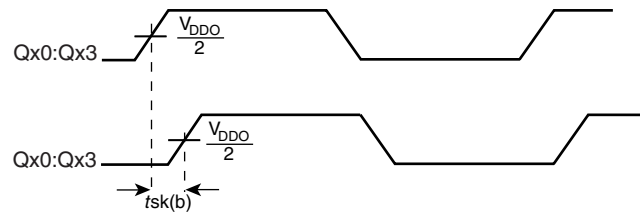
3.3V CORE/1.2V OUTPUT LOAD AC TEST CIRCUIT



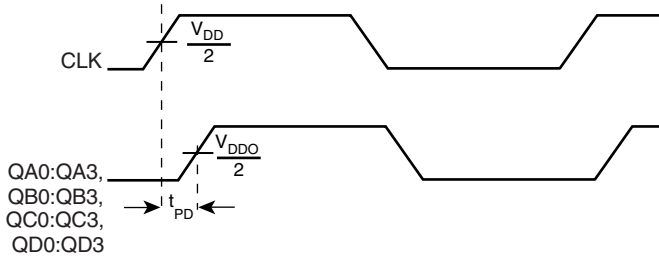
OUTPUT SKEW



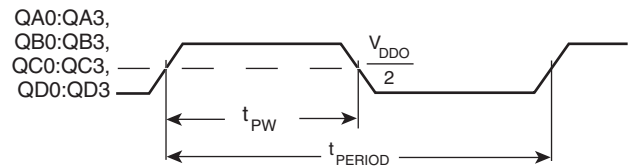
PART-TO-PART SKEW



BANK SKEW (where x denotes outputs in the same bank)

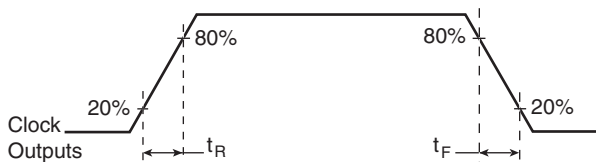


PROPAGATION DELAY



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYCLE/PLUSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

LVCMOS CONTROL PINS

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1k Ω resistor can be used.

OUTPUTS:

LVCMOS OUTPUTS

All unused LVCMOS output can be left floating. We recommend that there is no trace attached.

VFQFN EPAD THERMAL RELEASE PATH

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 1*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes")

are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor's Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

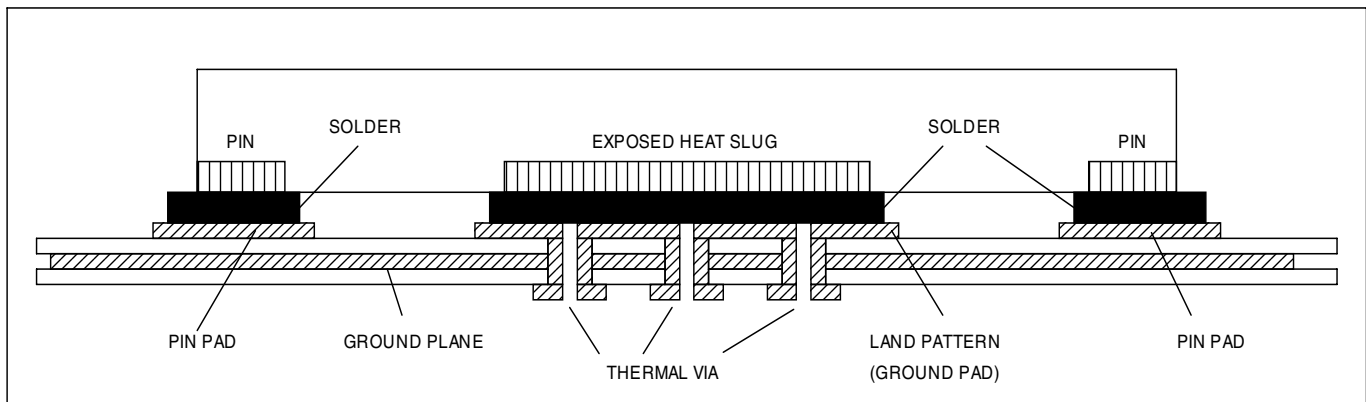


FIGURE 1. P.C. ASSEMBLY FOR EXPOSED PAD THERMAL RELEASE PATH -SIDE VIEW (DRAWING NOT TO SCALE)

RELIABILITY INFORMATION

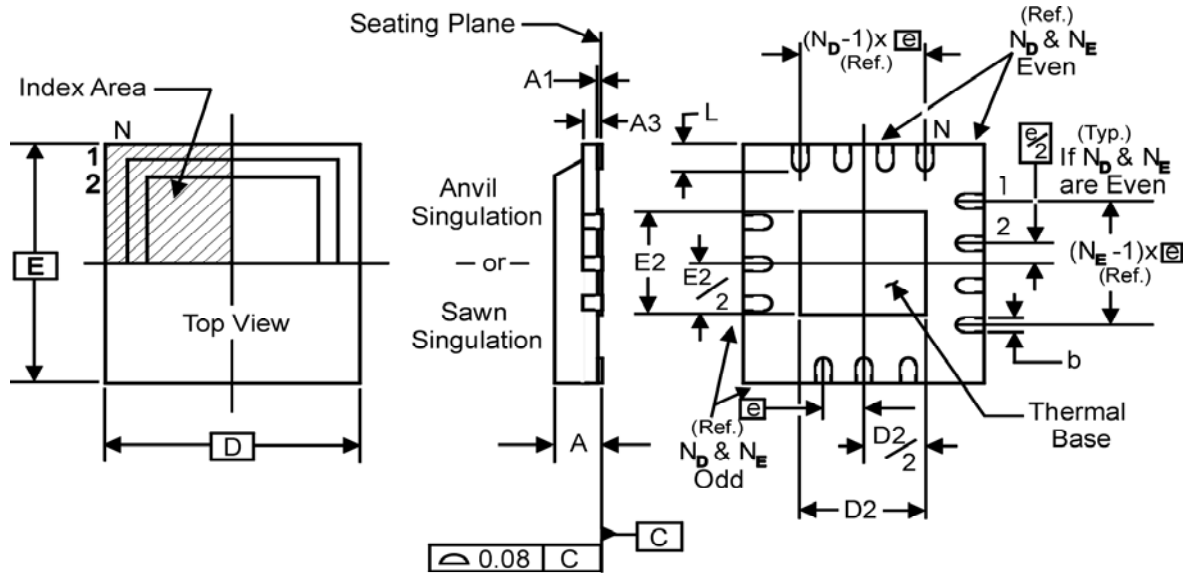
TABLE 6. θ_{JA} vs. AIR FLOW TABLE FOR 32 LEAD VFQFN

θ_{JA} vs. 0 Air Flow (Linear Feet per Minute)	
Multi-Layer PCB, JEDEC Standard Test Boards	0 34.8°C/W

TRANSISTOR COUNT

The transistor count for ICS8316 is: 416

PACKAGE OUTLINE AND DIMENSIONS - K SUFFIX FOR 32 LEAD VFQFN



NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of

this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 11 below.

TABLE 7. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	VHHD-2		
	MINIMUM	NOMINAL	MAXIMUM
N	32		
A	0.80	--	1.00
A1	0	--	0.05
A3	0.25 Ref.		
b	0.18	0.25	0.30
ND	8		
NE	8		
D	5.00 BASIC		
D2	3.0		3.3
E	5.00 BASIC		
E2	3.0		3.3
e	0.50 BASIC		
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS8316AKLF	ICS8316AKLF	32 Lead "Lead-Free" VFQFN	tray	0°C to 70°C
ICS8316AKLFT	ICS8316AKLF	32 Lead "Lead-Free" VFQFN	2500 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET

Rev	Table	Page	Description of Change	Date
B	T5	1	Features section - updated Output Skew bullet.	2/29/08
		3	AC Characteristics Table - per PCN changed Output Skew parameter from 140ps max. to 380ps max. And changed Bank Skew from 60ps max. to 70ps max.	
	5	Added VFQFN Thermal Release Path section.		
	7	Added note to Package Outline.		
	T7	7	Package Dimensions Table - corrected D2/E2 measurements.	

ICS8316

LOW SKEW, 1-TO-16, LVCMOS/LVTTL FANOUT BUFFER W/1.2V LVCMOS OUTPUTS

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.