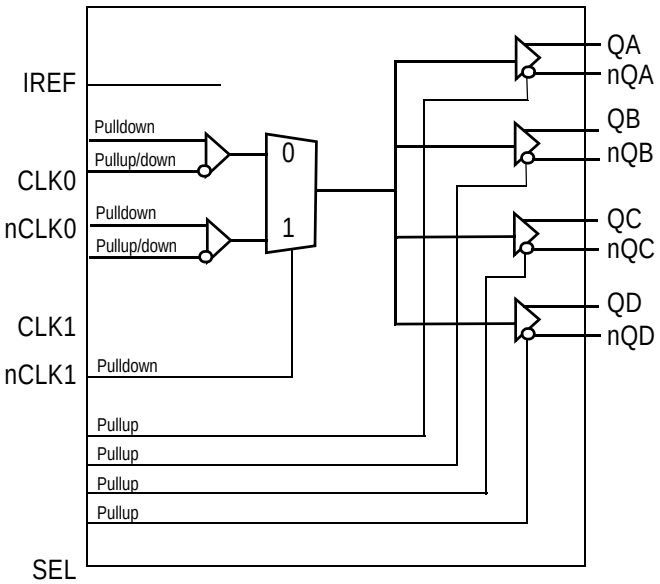
General Description

The 831724 is a high-performance, differential HCSL clock/data multiplexer and fanout buffer. The device is designed for the multiplexing and fanout of high-frequency clock and data signals. The device has two differential, selectable clock/data inputs. The selected input signal is distributed to four low-skew differential HCSL outputs. Each input pair accepts HCSL, LVDS and LVPECL levels. The 831724 is characterized to operate from a 3.3V power supply. Guaranteed input, output-to-output and part-to-part skew characteristics make the 831724 ideal for those clock and data distribution applications demanding well-defined performance and repeatability. The 831724 supports the clock multiplexing and distribution of PCI Express Generation 1, 2, and 3 clock signals.

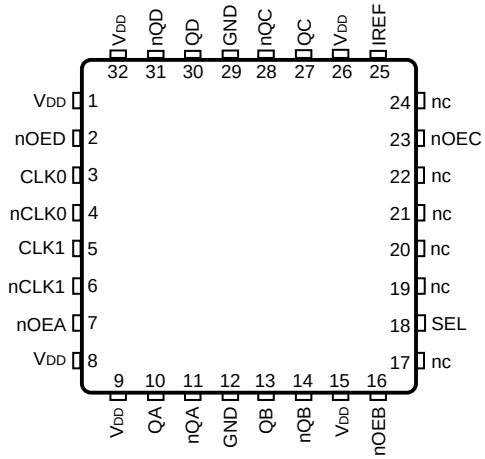
Features

- 2:1 differential clock/data multiplexer with fanout
- Two selectable, differential inputs
- Each differential input pair can accept the following levels: HCSL, LVDS, LVPECL.
- Four differential HCSL outputs
- Maximum input/output clock frequency: 350MHz
- Maximum input/output data rate: 700Mb/s (NRZ)
- LVCMOS interface levels for all control inputs
- PCI Express Gen 1,2,3 jitter compliant
- Input skew: 165ps (maximum)
- Output skew: 175ps (maximum)
- Part-to-part skew: 450ps (maximum)
- Full 3.3V supply voltage
- Available in lead-free (RoHS 6) package
- -40°C to 85°C ambient operating temperature

Block Diagram



Pin Assignment



831724I
32-Lead VFQFN
5mm x 5mm x 0.925mm package body
K Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 8, 9, 15, 26, 32	V_{DD}	Power		Positive power supply pins.
2	nOED	Input	Pullup	Output enable for the QD output. See Table 3D for function. LVCMOS/LVTTL interface levels.
3	CLK0	Input	Pulldown	Non-inverting clock/data input 0.
4	nCLK0	Input	Pulldown/Pullup	Inverting differential clock input 0. $V_{DD}/2$ default when left floating.
5	CLK1	Input	Pulldown	Non-inverting clock/data input 1.
6	nCLK1	Input	Pulldown/Pullup	Inverting differential clock input 1. $V_{DD}/2$ default when left floating.
7	nOEA	Input	Pullup	Output enable for the QA output. See Table 3A for function. LVCMOS/LVTTL interface levels.
10, 11	QA, nQA	Output		Differential output pair A. HCSL interface levels.
12, 29	GND	Power		Power supply ground.
13, 14	QB, nQB	Output		Differential output pair B. HCSL interface levels.
16	nOEB	Input	Pullup	Output enable for the QB output. See Table 3B for function. LVCMOS/LVTTL interface levels.
17, 19, 20, 21, 22, 24	nc	Unused		No connect pins.
18	SEL	Input	Pulldown	Input select. See Table 3E for function. LVCMOS/LVTTL interface levels.
23	nOEC	Input	Pullup	Output enable for the QC output. See Table 3C for function. LVCMOS/LVTTL interface levels.
25	IREF	Input		An external fixed precision resistor (475Ω) from this pin to ground provides a reference current used for the differential current-mode QX, nQX outputs.
27, 28	QC, nQC	Output		Differential output pair C. HCSL interface levels.
30, 31	QD, nQD	Output		Differential output pair D. HCSL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3A. nOEA Configuration Table

Input	
nOEA	**Operation**
0	Output QA, nQA is enabled.
1 (default)	Output QA, nQA is in high-impedance state.

NOTE: nOEA is an asynchronous control.

Table 3B. nOEB Configuration Table

Input	
nOEB	**Operation**
0	Output QB, nQB is enabled.
1 (default)	Output QB, nQB is in high-impedance state.

NOTE: nOEB is an asynchronous control.

Table 3C. nOEC Configuration Table

Input	
nOEC	**Operation**
0	Output QC, nQC is enabled.
1 (default)	Output QC, nQC is in high-impedance state.

NOTE: nOEC is an asynchronous control.

Table 3D. nOED Configuration Table

Input	
nOED	**Operation**
0	Output QD, nQD is enabled.
1 (default)	Output QD, nQD is in high-impedance state.

NOTE: nOED is an asynchronous control.

Table 3E. SEL Configuration Table

Input	
SEL	**Selected Input**
0 (default)	CLK0, nCLK0
1	CLK1, nCLK1

NOTE: SEL is an asynchronous control

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	37°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 0.3V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.0	3.3	3.6	V
I_{DD}	Power Supply Current				128	mA

Table 4B. LVCMOS/LVTTL Input DC Characteristics, V_{DD} = 3.3V ± 0.3V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2.4		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	nOEA, nOEB, nOEC, nOED	V_{IN} = V_{DD}			5	µA
		SEL	V_{IN} = V_{DD}			150	µA
I_{IL}	Input Low Current	nOEA, nOEB, nOEC, nOED	V_{IN} = 0V	-150			µA
		SEL	V_{IN} = 0V	-5			µA

Table 4C. Differential DC Characteristics, V_{DD} = 3.3V ± 0.3V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK0, nCLK0, CLK1, nCLK1	V_{IN} = V_{DD}= 3.3V ± 0.3V			150	µA
I_{IL}	Input Low Current	CLK0, CLK1	V_{DD} = 3.3V ± 0.3V, V_{IN} = 0V	-5			µA
		nCLK0, nCLK1	V_{DD} = 3.3V ± 0.3V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			0.5		V_{DD} – 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.

AC Electrical Characteristics

Table 5A. PCI Express Jitter Specifications, V_{DD} = 3.3V ± 0.3V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	PCIe Industry Specification	Units
t_j (PCIe Gen 1)	Phase Jitter Peak-to-Peak; NOTE 1, 4	f = 100MHz, Evaluation Band: 0Hz - Nyquist (clock frequency/2)		11.48	27	86	ps
$t_{REFCLK\_HF\_RMS}$ (PCIe Gen 2)	Phase Jitter RMS; NOTE 2, 4	f = 100MHz, High Band: 1.5MHz - Nyquist (clock frequency/2)		0.76	1.0	3.1	ps
$t_{REFCLK\_LF\_RMS}$ (PCIe Gen 2)	Phase Jitter RMS; NOTE 2, 4	f = 100MHz, Low Band: 10kHz - 1.5MHz		0.15	1.3	3.0	ps
t_{REFCLK_RMS} (PCIe Gen 3)	Phase Jitter RMS; NOTE 3, 4	f = 100MHz, Evaluation Band: 0Hz - Nyquist (clock frequency/2)		0.16	0.4	0.8	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions. The phase noise is dependent on the input signal source. The input signal was generated using a Tektronix HFS9000 Stimulus System. For additional information, refer to the *PCI Express Application Note section* in the datasheet.
NOTE 1: Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1 is 86ps peak-to-peak for a sample size of 10^6 clock periods.
NOTE 2: RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps RMS for $t_{REFCLK\_HF\_RMS}$ (High Band) and 3.0ps RMS for $t_{REFCLK\_LF\_RMS}$ (Low Band).
NOTE 3: RMS jitter after applying system transfer function for the common clock architecture. This specification is based on the *PCI Express Base Specification Revision 0.7, October 2009* and is subject to change pending the final release version of the specification.
NOTE 4: This parameter is guaranteed by characterization. Not tested in production.

Table 5B. HCSL AC Characteristics, V_{DD} = 3.3V ± 0.3V, T_A = -40°C to 85°C

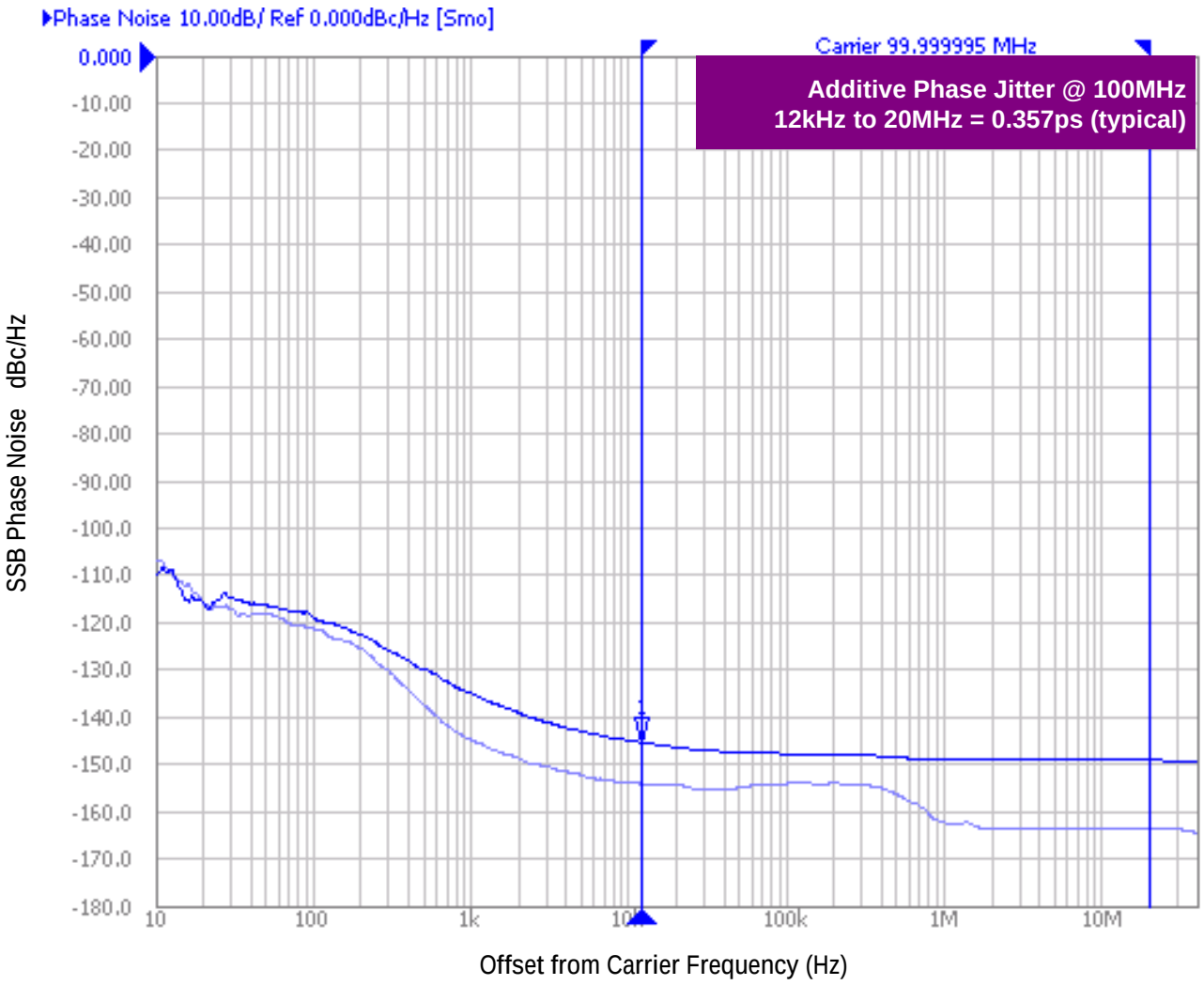
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				350	MHz
*t*jit	Buffer Additive Phase Jitter, RMS	100MHz, Integration Range: 12kHz – 20MHz		0.357	0.480	ps
t_{PD}	Propagation Delay; NOTE 1, 3	Any CLK, nCLK to any Q, nQ	2.7		3.9	ns
*t*sk(o)	Output Skew; NOTE 3,15	Across all outputs			175	ps
tsk(i)	Input Skew; NOTE 2, 3				165	ps
tsk(pp)	Part-to-Part Skew; NOTE 3, 4				450	ps
MUX_{ISOL}	Mux Isolation	*f* = 100MHz		94		dB
Rising Edge Rate	Rising Edge Rate; NOTE 5, 6	$f_{OUT} \leq 125MHz$	0.6		4.2	V/ns
		$f_{OUT} > 125MHz$	0.6		6.8	V/ns
Falling Edge Rate	Falling Edge Rate; NOTE 5, 6	$f_{OUT} \leq 125MHz$	0.6		4.5	V/ns
		$f_{OUT} > 125MHz$	0.6		6.7	V/ns
T_{STABLE}	Time before VRB is allowed; NOTE 5, 7		500			ps
V_{RB}	Ringback Voltage; NOTE 5, 7		-100		100	mV
V_{MAX}	Absolute Maximum Output Voltage; NOTE 8, 9				1150	mV
V_{MIN}	Absolute Minimum Output Voltage; NOTE 8, 10		-300			mV
V_{CROSS}	Absolute Crossing Voltage; NOTE 8, 11, 12		200		550	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all edges; NOTE 8, 11, 13				140	mV
odc	Output Duty Cycle; NOTE 14	$f_{OUT} \leq 125MHz$	46		54	%
		$f_{OUT} > 125MHz$	40		60	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between input paths on the same device, using the same input signal levels, measured at one specific output at the differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 5: Measurement taken from differential waveform.
NOTE 6: Measurement from -150mV to +150mV on the differential waveform (derived from Q minus nQ). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.
NOTE 7: T_{STABLE} is the time the differential clock must maintain a minimum ±150mV differential voltage after rising/falling edges before it is allowed to drop back into the V_{RB} ±100 differential range. See Parameter Measurement Information Section.
NOTE 8: Measurement taken from single-ended waveform.
NOTE 9: Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.
NOTE 10: Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.
Notes continued on next page.
NOTE 11: Measured at crossing point where the instantaneous voltage value of the rising edge of Q equals the falling edge of nQ. See Parameter Measurement Information Section

NOTE 12: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Parameter Measurement Information Section.
NOTE 13: Defined as the total variation of all crossing voltage of rising Q and falling nQ. This is the maximum allowed variance in the V_{CROSS} for any particular system. See Parameter Measurement Information Section.
NOTE 14: Input duty cycle must be 50%.
NOTE 15: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.

Additive Phase Jitter

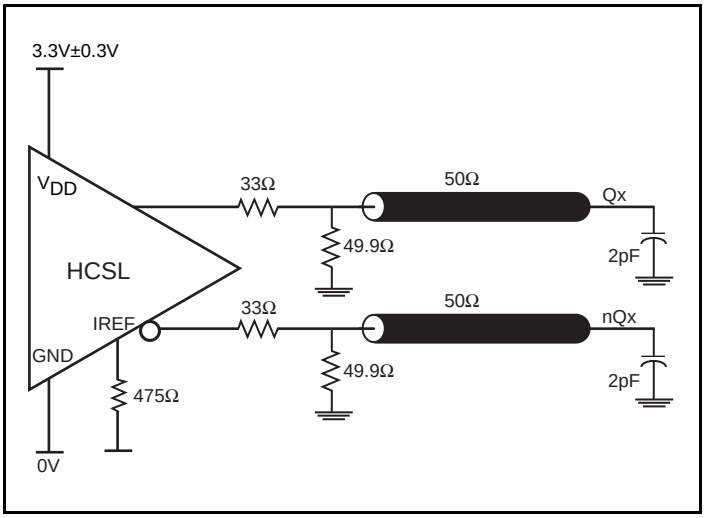
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the *dBc Phase Noise.* This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a *dBc* value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



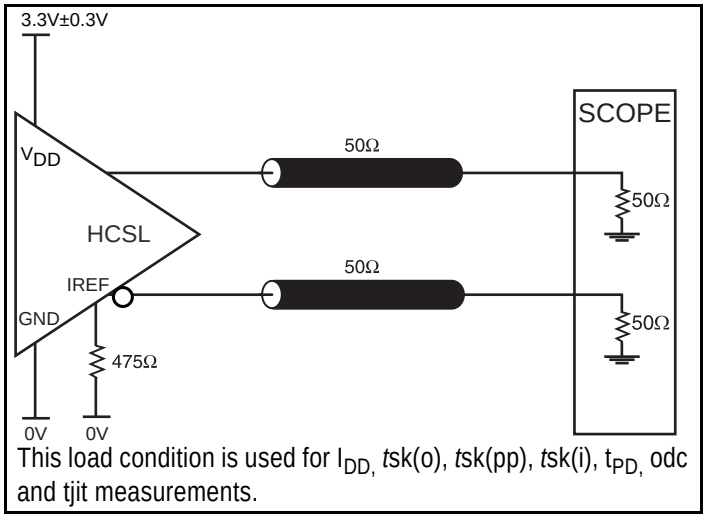
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower.

The phase noise is dependent on the input source and measurement equipment. The source generator is the Rohde & Schwarz SMA 100A. Phase noise is measured using an Agilent E5052A Signal Source Analyzer.

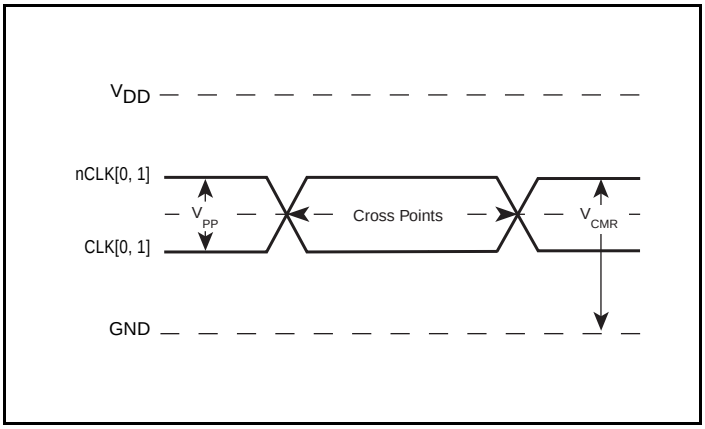
Parameter Measurement Information



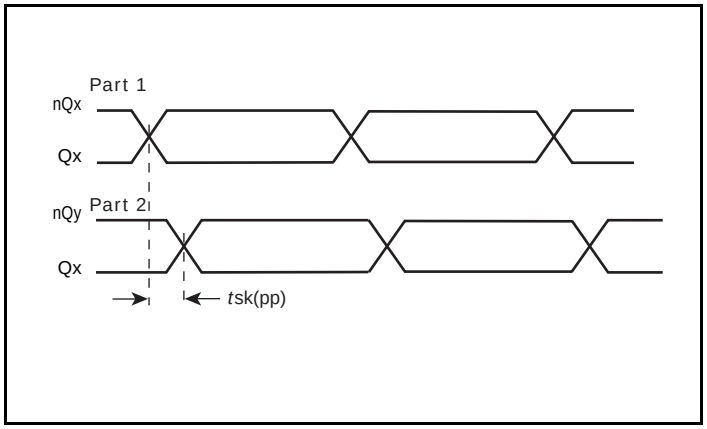
3.3V HCSL Output Load AC Test Circuit 1



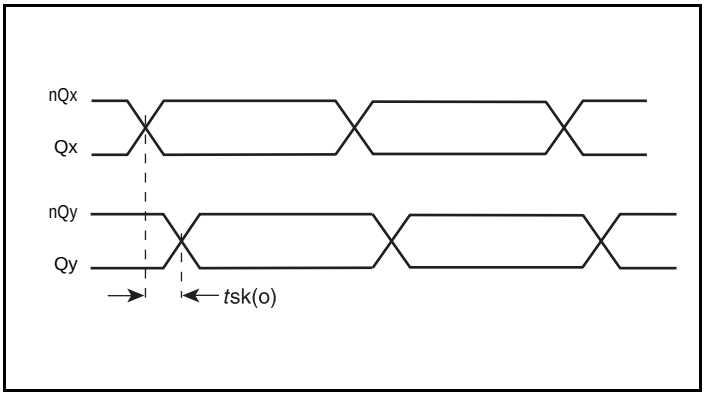
3.3V HCSL Output Load AC Test Circuit 2



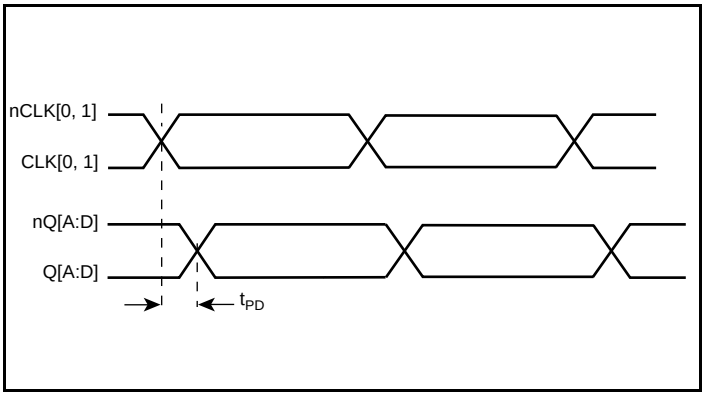
Differential Input Level



Part-to-Part Skew

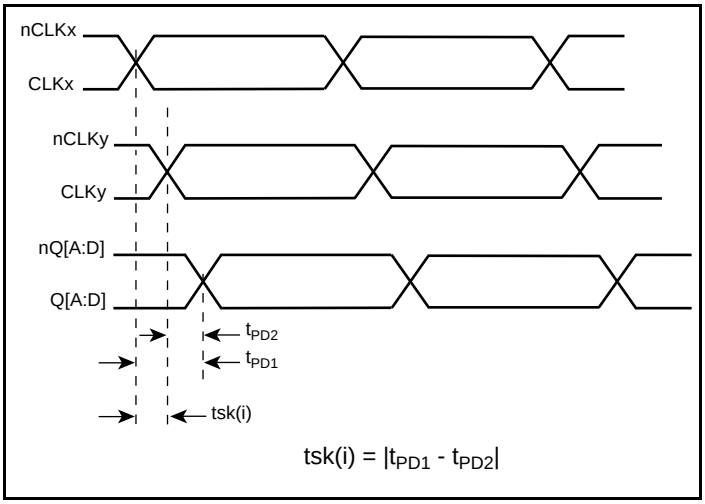


Output Skew

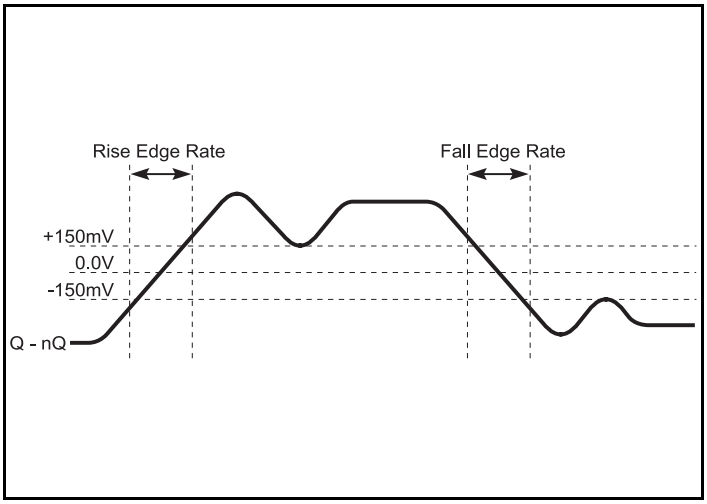


Propagation Delay

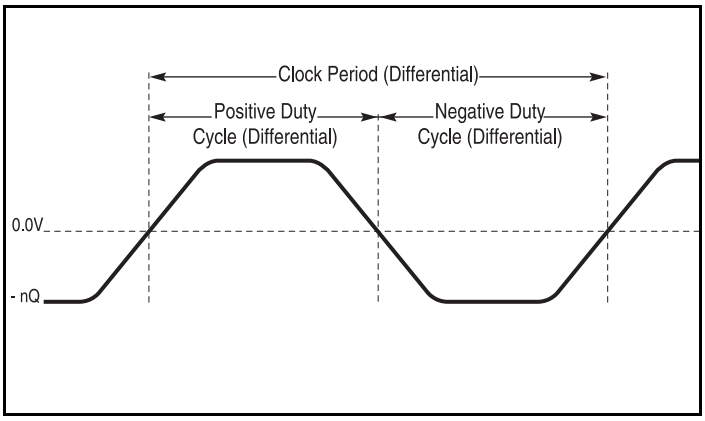
Parameter Measurement Information, continued



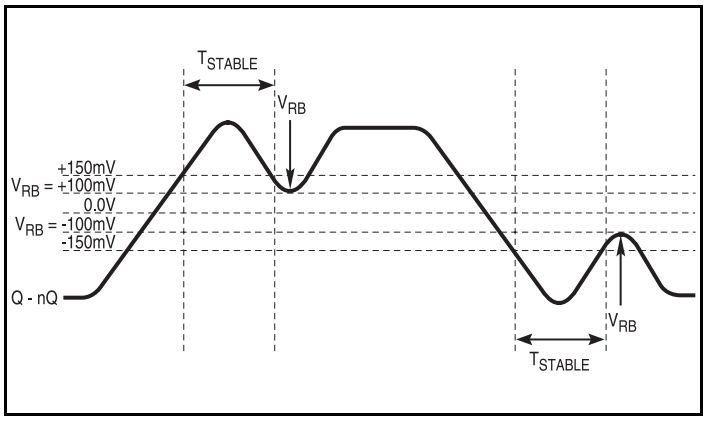
Input Skew



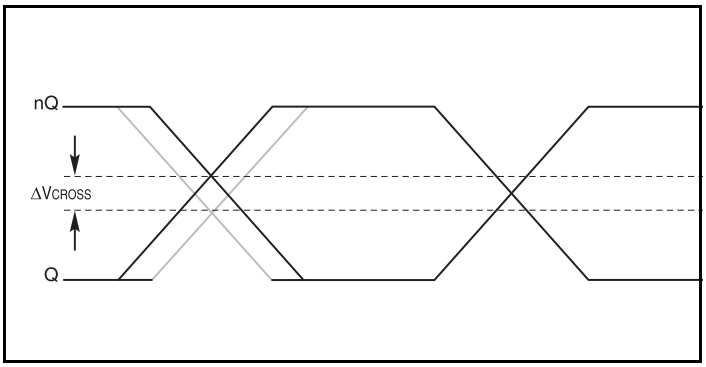
Differential Measurement Points for Rise/Fall Edge Rate



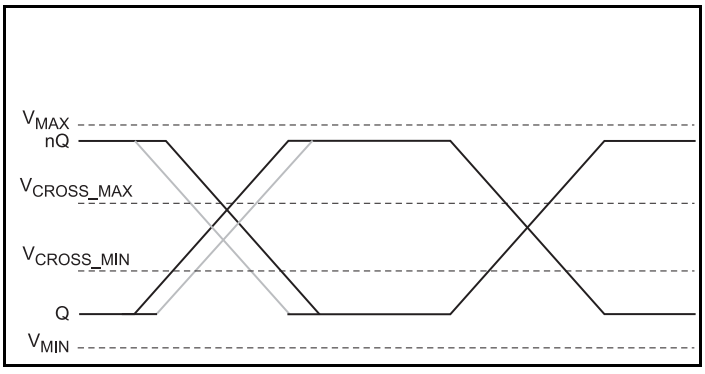
Differential Measurement Points for Duty Cycle/Period



Differential Measurement Points for Ringback

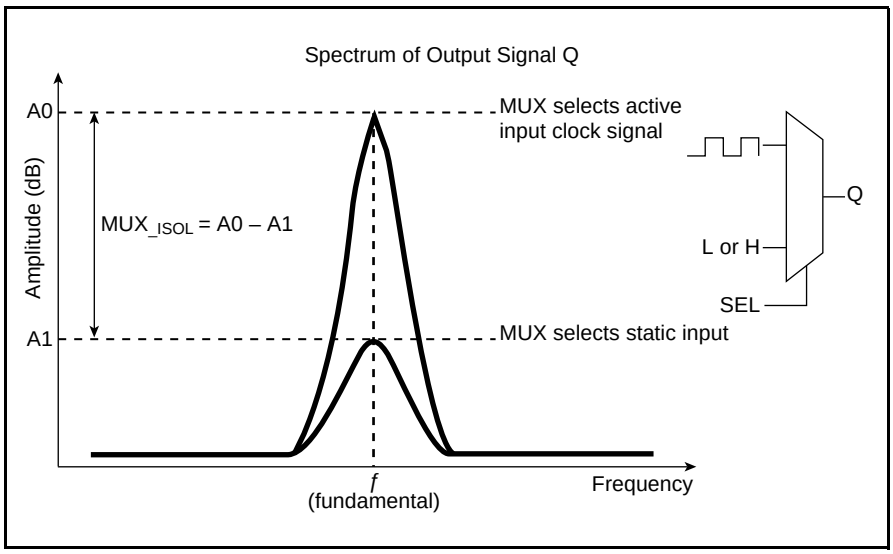


Single-ended Measurement Points for Delta Cross Point



Single-ended Measurement Points for Absolute Cross Point/Swing

Parameter Measurement Information, continued



MUX Isolation

PCI Express Application Note

PCI Express jitter analysis methodology models the system response to reference clock jitter. The block diagram below shows the most frequently used *Common Clock Architecture* in which a copy of the reference clock is provided to both ends of the PCI Express Link.

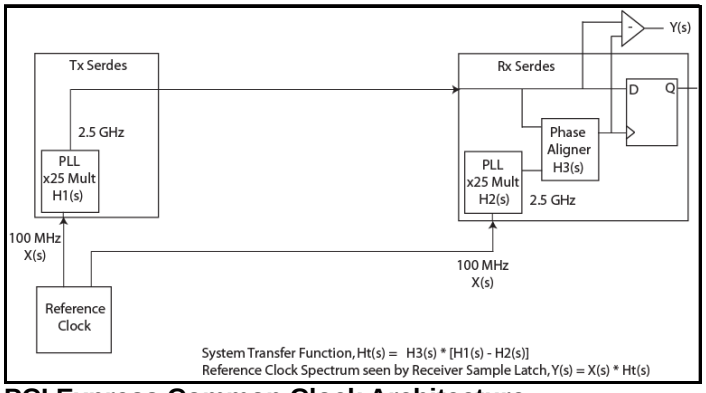
In the jitter analysis, the transmit (Tx) and receive (Rx) serdes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is:

$$Ht(s) = H3(s) \times [H1(s) - H2(s)]$$

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum X(s) and is:

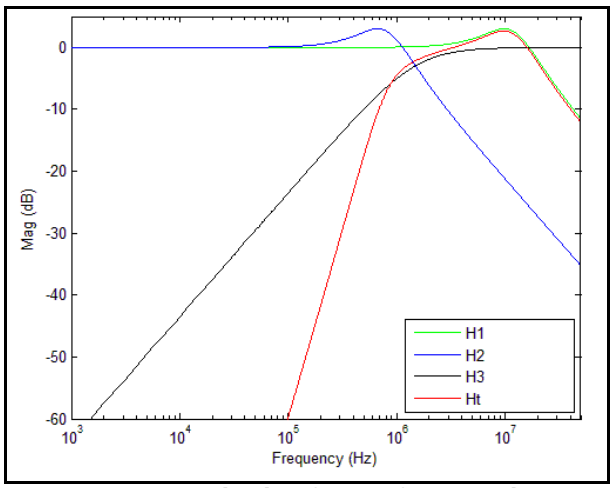
$$Y(s) = X(s) \times H3(s) \times [H1(s) - H2(s)]$$

In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on X(s)*H3(s) * [H1(s) - H2(s)].



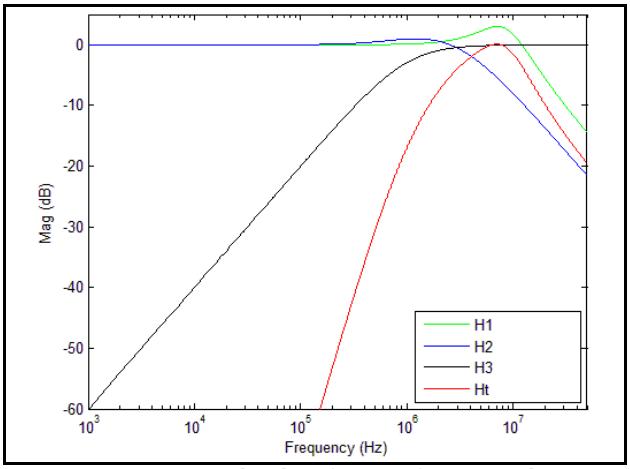
PCI Express Common Clock Architecture

For PCI Express Gen 1, one transfer function is defined and the evaluation is performed over the entire spectrum: DC to Nyquist (e.g for a 100MHz reference clock: 0Hz – 50MHz) and the jitter result is reported in peak-peak.

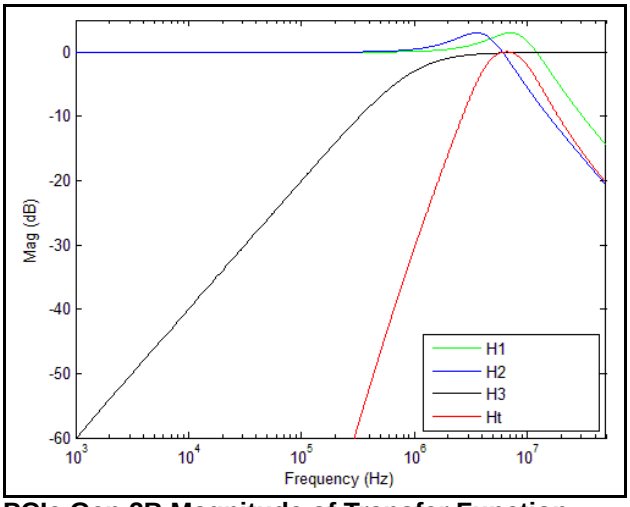


PCIe Gen 1 Magnitude of Transfer Function

For PCI Express Gen 2, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in rms. The two evaluation ranges for PCI Express Gen 2 are 10kHz – 1.5MHz (Low Band) and 1.5MHz – Nyquist (High Band). The plots show the individual transfer functions as well as the overall transfer function Ht.

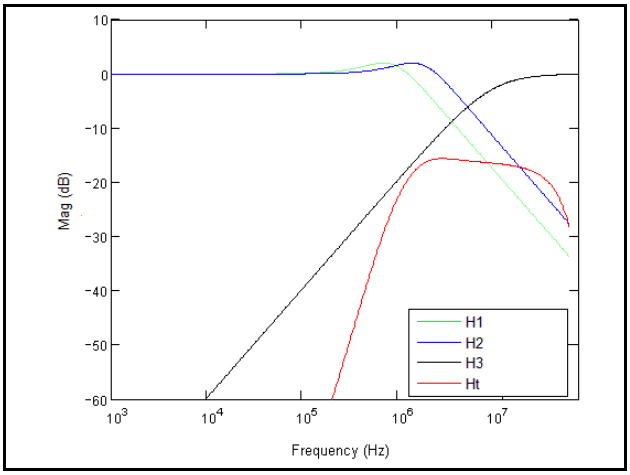


PCIe Gen 2A Magnitude of Transfer Function



PCIe Gen 2B Magnitude of Transfer Function

For PCI Express Gen 3, one transfer function is defined and the evaluation is performed over the entire spectrum. The transfer function parameters are different from Gen 1 and the jitter result is reported in RMS.



PCIe Gen 3 Magnitude of Transfer Function

For a more thorough overview of PCI Express jitter analysis methodology, please refer to IDT Application Note: *PCI Express Reference Clock Requirements.*

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pullup or pulldown; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

CLK/nCLK Inputs

For applications requiring only one differential input, the unused CLK/nCLK input can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

Outputs:

Differential Outputs

The unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{DD} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

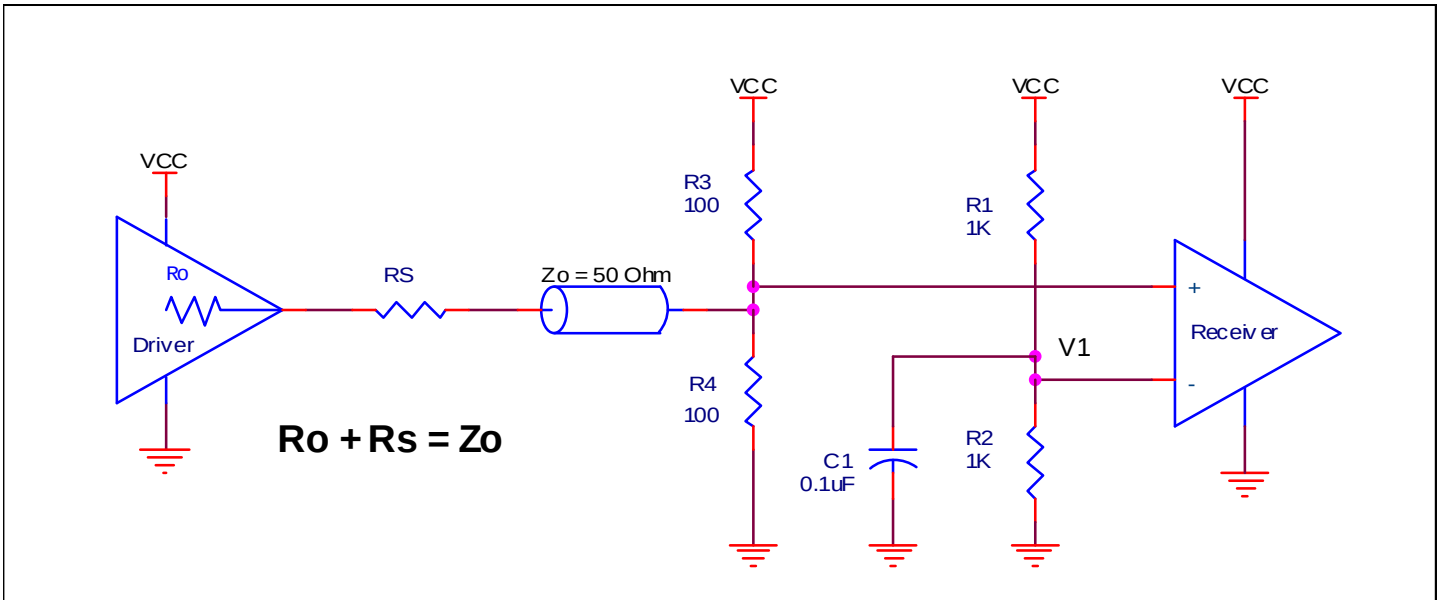


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, HCSL, and other differential signals. Both differential inputs must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2D* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 2A, the input termination applies for IDT LVPECL drivers. If you are using an LVPECL driver from another vendor, use their termination recommendation.

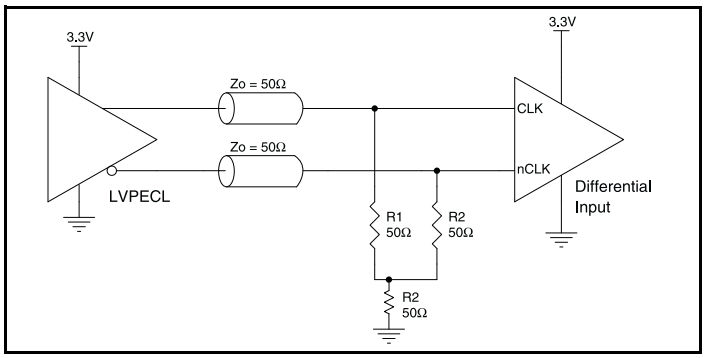


Figure 2A. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

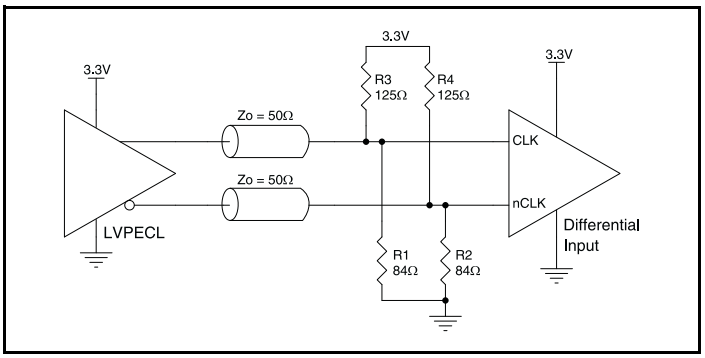


Figure 2B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

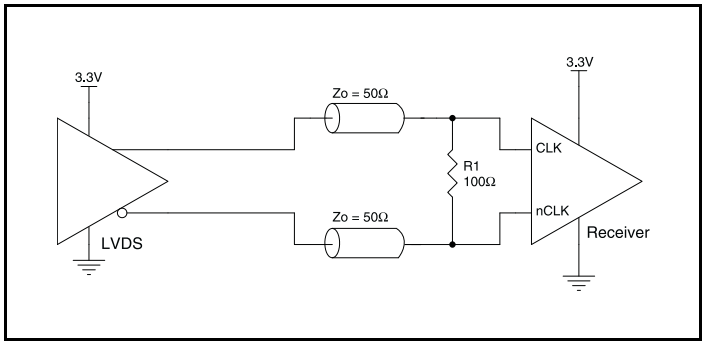


Figure 2C. CLK/nCLK Input Driven by a 3.3V LVDS Driver

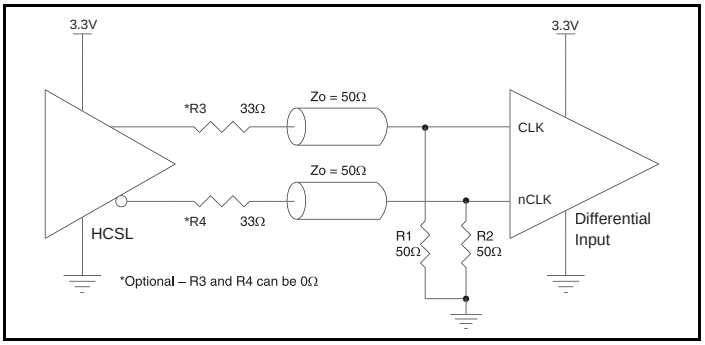


Figure 2D. CLK/nCLK Input Driven by a 3.3V HCSL Driver

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 3.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

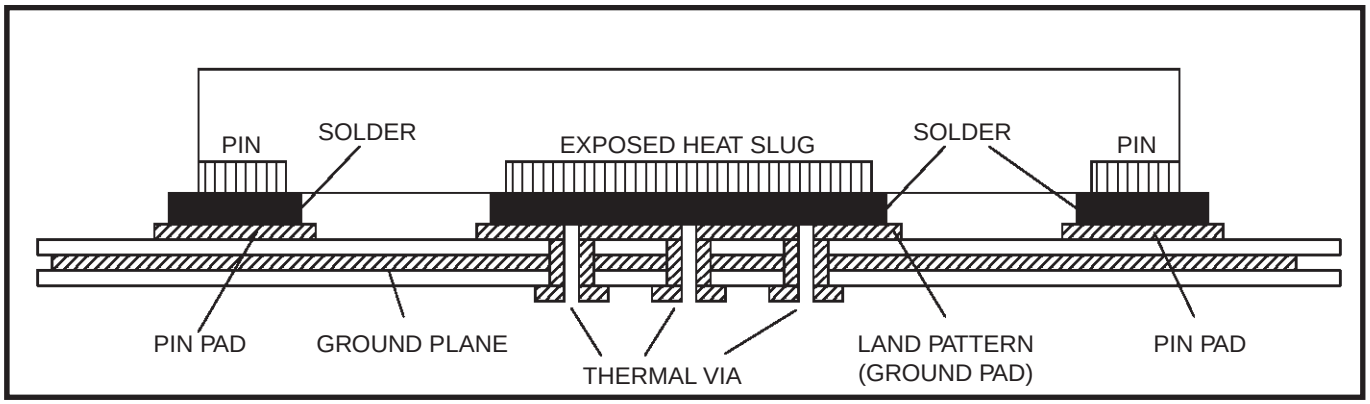


Figure 3. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Recommended Termination

Figure 4A is the recommended source termination for applications where the driver and receiver will be on a separate PCBs. This termination is the standard for PCI Express™ and HCSL output types. All traces should be 50Ω impedance single-ended or 100Ω differential.

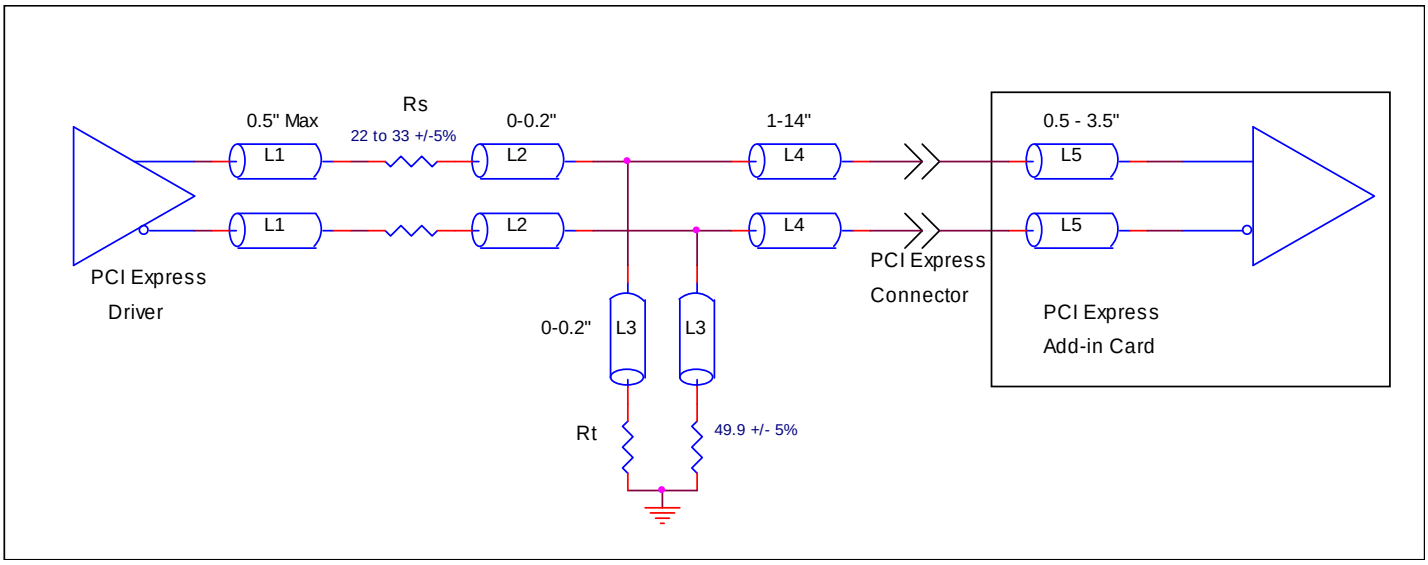


Figure 4A. Recommended Source Termination (where the driver and receiver will be on separate PCBs)

Figure 4B is the recommended termination for applications where a point-to-point connection can be used. A point-to-point connection contains both the driver and the receiver on the same PCB. With a matched termination at the receiver, transmission-line reflections will be minimized. In addition, a series resistor (Rs) at the driver offers flexibility and can help dampen unwanted reflections. The optional resistor can range from 0Ω to 33Ω. All traces should be 50Ω impedance single-ended or 100Ω differential.

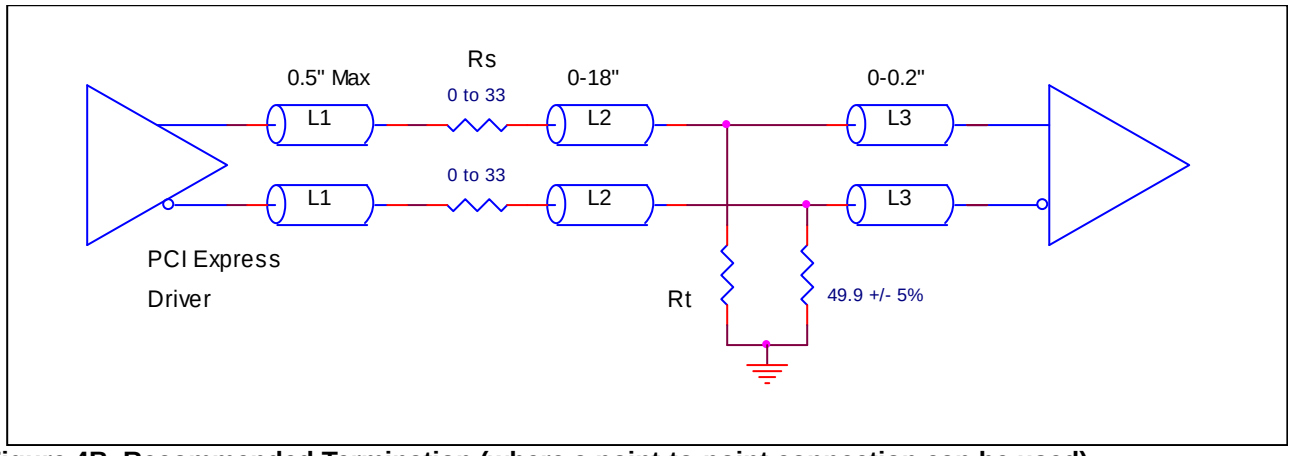


Figure 4B. Recommended Termination (where a point-to-point connection can be used)

Power Considerations

This section provides information on power dissipation and junction temperature for the 831724.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 831724 is the sum of the core power plus the power dissipated at the output(s).
The following is the power dissipation for V_{DD} = 3.3V ± 0.3V = 3.6V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated at the output(s).

Total $Power_{MAX}$ = V_{DD_MAX} * (I_{DD_MAX}) = 3.6V * 128mA = **460.8mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 37.0°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.4608W *37.0°C/W = 102.05°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 32 Lead VFQFN, Forced Convection

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

3. Calculations and Equations.

The purpose of this section is to calculate power dissipation on the IC per HCSL output pair.

HCSL output driver circuit and termination are shown in *Figure 5.*

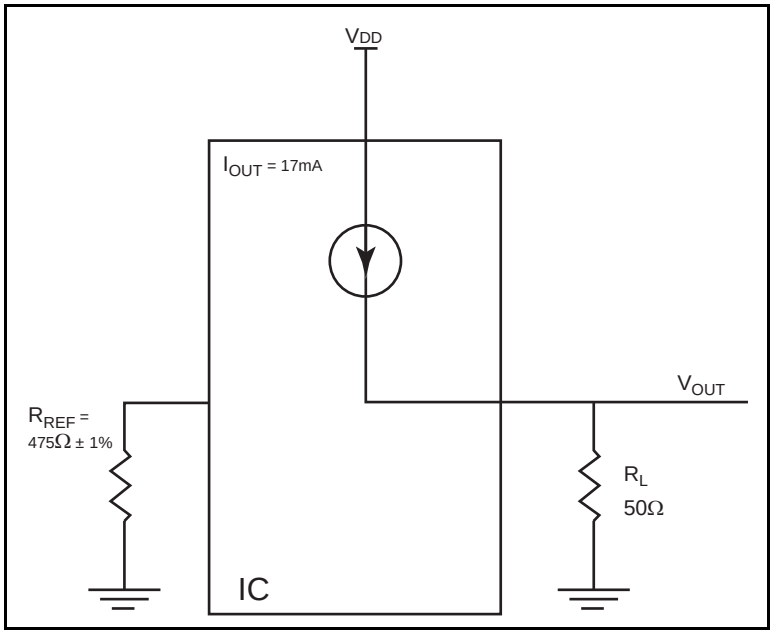


Figure 5. HCSL Driver Circuit and Termination

HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs at V_{DD_MAX}.

Power = $(V_{DD\_MAX} – V_{OUT}) * I_{OUT}$,
since $V_{OUT} = I_{OUT} * R_L$

Power = $(V_{DD\_MAX} – I_{OUT} * R_L) * I_{OUT}$

Power = (3.6V – 17mA * 50Ω) * 17mA

Total Power Dissipation per output pair = **46.8mW**

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 32 Lead VFQFN

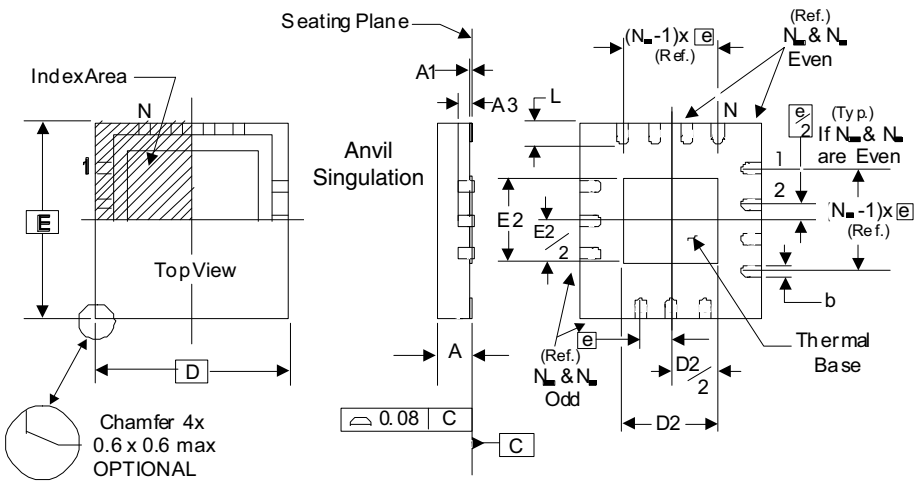
θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

Transistor Count

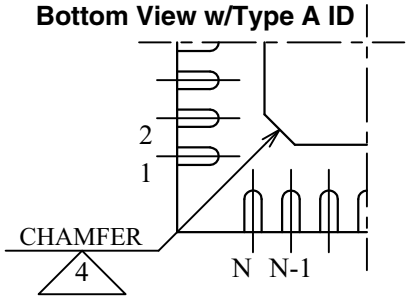
The transistor count for the 831724 is: 1571

Package Outline and Package Dimensions

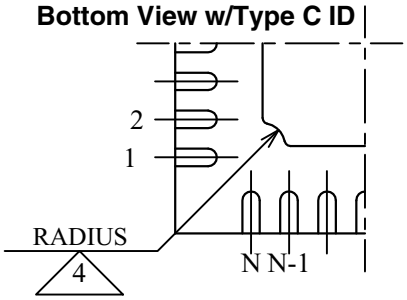
Package Outline - K Suffix for 32 Lead VFQFN



Bottom View w/Type A ID



Bottom View w/Type C ID



There are 2 methods of indicating pin 1 corner at the back of the VFQFN package:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type C: Mouse bite on the paddle (near pin 1)

Table 8. Package Dimensions

JEDEC Variation: VHHD-2/-4 All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A	0.80		1.00
A1	0		0.05
A3		0.25 Ref.	
b	0.18	0.25	0.30
N_D & N_E			8
D & E		5.00 Basic	
D2 & E2	3.0		3.3
e		0.50 Basic	
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

The package mechanical drawing shown is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device.

The pin count and pin-out are shown on the front page. The package dimensions are in Table 8.

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
831724AKILF	ICS31724AIL	“Lead-Free” 32 Lead VFQFN	Tray	-40°C to 85°C
831724AKILFT	ICS31724AIL	“Lead-Free” 32 Lead VFQFN	Tape & Reel	-40°C to 85°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T9 	footer 22	Added ‘A’ to part number. Added ‘A’ to part number, deleted quantity 2500 from Tape and Reel, deleted Lead-Free note.	10/1/12
A		Header Footer	Corrected part number Corrected part number	5/16/13
A			Removed ICS from part number where needed. Updated data sheet header and footer.	4/4/16
B		1	Block Diagram corrected diagram clock outputs. Deleted “I” prefix from part number.	11/16/16

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