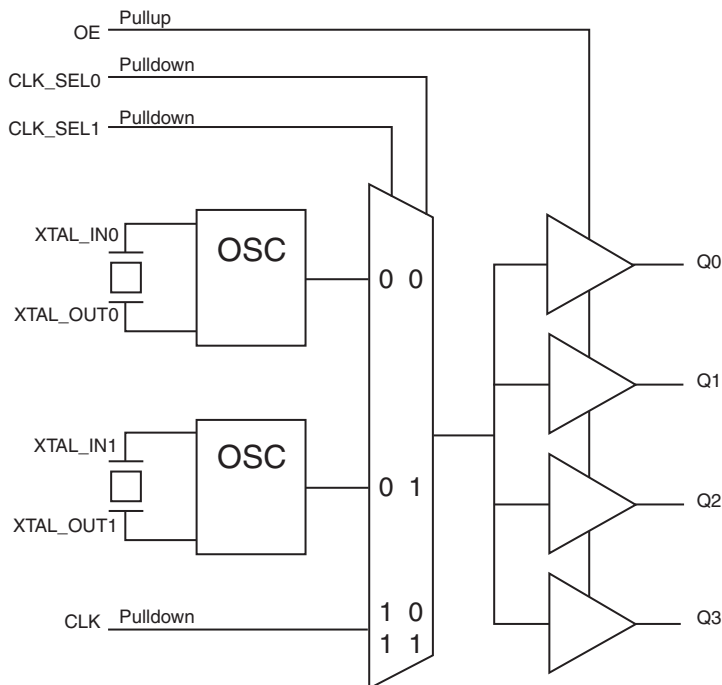


## GENERAL DESCRIPTION

The 83904-02 is a low skew, high performance 1-to-4 Crystal-to-LVCMOS Fanout Buffer. The 83904-02 has selectable single-ended clock or two crystal-oscillator inputs. There is an output enable to disable the outputs by placing them into a high-impedance state.

Guaranteed output and part-to-part skew characteristics make the 83904-02 ideal for those applications demanding well defined performance and repeatability.

## BLOCK DIAGRAM



## FEATURES

- Four LVCMOS/LVTTL outputs,  
19Ω typical output impedance @  $V_{DD} = V_{DDO} = 3.3V$
- Two Crystal oscillator input pairs  
One LVCMOS/LVTTL clock input
- Crystal input frequency range: 12MHz – 38.88MHz
- Output frequency: 200MHz (maximum)
- Output Skew: 40ps (maximum) @  $V_{DD} = V_{DDO} = 3.3V$
- RMS phase jitter @ 25MHz output, using a 25MHz crystal (100Hz – 1MHz): 0.16ps (typical) @  $V_{DD} = V_{DDO} = 3.3V$
- RMS phase noise at 25MHz:
 

Offset	Noise Power
100Hz	-118.4 dBc/Hz
1kHz	-141.5 dBc/Hz
10kHz	-157.2 dBc/Hz
100kHz	-157.2 dBc/Hz
- Supply Voltage Modes:  
(Core/Output)  
3.3V/3.3V  
3.3V/2.5V  
3.3V/1.8V  
2.5V/2.5V  
2.5V/1.8V
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package

## PIN ASSIGNMENT

CLK_SEL0	1	16	V <sub>DDO</sub>
XTAL_OUT0	2	15	Q0
XTAL_IN0	3	14	Q1
V <sub>DD</sub>	4	13	GND
XTAL_IN1	5	12	Q2
XTAL_OUT1	6	11	Q3
CLK_SEL1	7	10	V <sub>DDO</sub>
CLK	8	9	OE

**83904-02**  
**16-Lead TSSOP**  
4.4mm x 5.0mm x 0.92mm  
package body  
**G Package**  
Top View

**TABLE 1. PIN DESCRIPTIONS**

Number	Name	Type		Description
1, 7	CLK_SEL0, CLK_SEL1	Input	Pulldown	Clock select inputs. See Table 3, Input Reference Function Table. LVCMOS / LVTTTL interface levels.
2, 3	XTAL_OUT0, XTAL_IN0	Input		Crystal oscillator interface. XTAL_IN0 is the input. XTAL_OUT0 is the output.
4	V <sub>DD</sub>	Power		Positive supply pin.
5, 6	XTAL_IN1, XTAL_OUT1	Input		Crystal oscillator interface. XTAL_IN1 is the input. XTAL_OUT1 is the output.
8	CLK	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTTL interface levels.
9	OE	Input	Pullup	Output enable. When LOW, outputs are in HIGH impedance state. When HIGH, outputs are active. LVCMOS / LVTTTL interface levels.
10, 16	V <sub>DDO</sub>	Power		Output supply pins.
11, 12, 14, 15	Q3, Q2, Q1, Q0	Output		Single-ended clock outputs. LVCMOS/LVTTTL interface levels.
13	GND	Power		Power supply ground.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ
C <sub>PD</sub>	Power Dissipation Capacitance (per output)	V <sub>DDO</sub> = 3.465V		8		pF
		V <sub>DDO</sub> = 2.625V		7		pF
		V <sub>DDO</sub> = 2.0V		7		pF
R <sub>OUT</sub>	Output Impedance	V <sub>DDO</sub> = 3.3V		19		Ω
		V <sub>DDO</sub> = 2.5V		21		Ω
		V <sub>DDO</sub> = 1.8V		32		Ω

**TABLE 3. INPUT REFERENCE FUNCTION TABLE**

Control Inputs		Reference
CLK_SEL1	CLK_SEL0	
0	0	XTAL0 (default)
0	1	XTAL1
1	0	CLK
1	1	CLK

### ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5V$
Outputs, $V_O$	-0.5V to $V_{DDO} + 0.5V$
Package Thermal Impedance, $\theta_{JA}$	100.3°C/W (0 mps)
Storage Temperature, $T_{STG}$	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Power Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		3.135	3.3	3.465	V
$I_{DD}$	Power Supply Current	No Load & XTALx selected @ 12MHz			7	mA
		No Load & CLK selected			1	mA
$I_{DDO}$	Output Supply Current	No Load & CLK selected			1	mA

**TABLE 4B. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Power Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		2.375	2.5	2.625	V
$I_{DD}$	Power Supply Current	No Load & XTALx selected @ 12MHz			7	mA
		No Load & CLK selected			1	mA
$I_{DDO}$	Output Supply Current	No Load & CLK selected			1	mA

**TABLE 4C. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Power Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		1.6	1.8	2.0	V
$I_{DD}$	Power Supply Current	No Load & XTALx selected @ 12MHz			7	mA
		No Load & CLK selected			1	mA
$I_{DDO}$	Output Supply Current	No Load & CLK selected			1	mA

**TABLE 4D. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Power Supply Voltage		2.375	2.5	2.625	V
$V_{DDO}$	Output Supply Voltage		2.375	2.5	2.625	V
$I_{DD}$	Power Supply Current	No Load & XTALx selected @ 12MHz			3	mA
		No Load & CLK selected			1	mA
$I_{DDO}$	Output Supply Current	No Load & CLK selected			1	mA

**TABLE 4E. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = 2.5V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Power Supply Voltage		2.375	2.5	2.625	V
$V_{DDO}$	Output Supply Voltage		1.6	1.8	2.0	V
$I_{DD}$	Power Supply Current	No Load & XTALx selected @ 12MHz			3	mA
		No Load & CLK selected			1	mA
$I_{DDO}$	Output Supply Current	No Load & CLK selected			1	mA

**TABLE 4F. DC CHARACTERISTICS,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	$V_{DD} = 3.3V \pm 5\%$	2.2		$V_{DD} + 0.3$	V
		$V_{DD} = 2.5V \pm 5\%$	1.6		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage	$V_{DD} = 3.3V \pm 5\%$	-0.3		1.3	V
		$V_{DD} = 2.5V \pm 5\%$	-0.3		0.9	V
$I_{IH}$	Input High Current	CLK, CLK_SEL0:1 $V_{DD} = 3.3V$ or $2.5V \pm 5\%$			150	$\mu A$
		OE $V_{DD} = 3.3V$ or $2.5V \pm 5\%$			5	$\mu A$
$I_{IL}$	Input Low Current	CLK, CLK_SEL0:1 $V_{DD} = 3.3V$ or $2.5V \pm 5\%$	-5			$\mu A$
		OE $V_{DD} = 3.3V$ or $2.5V \pm 5\%$	-150			$\mu A$
$V_{OH}$	Output High Voltage	$V_{DDO} = 3.3V \pm 5\%$ ; NOTE 1	2.6			V
		$V_{DDO} = 2.5V \pm 5\%$ ; NOTE 1	1.8			V
		$V_{DDO} = 1.8V \pm 0.2V$ ; NOTE 1	1.2			V
$V_{OL}$	Output Low Voltage	$V_{DDO} = 3.3V \pm 5\%$ ; NOTE 1			0.6	V
		$V_{DDO} = 2.5V \pm 5\%$ ; NOTE 1			0.5	V
		$V_{DDO} = 1.8V \pm 0.2V$ ; NOTE 1			0.4	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{DDO}/2$ . See Parameter Measurement section, "Load Test Circuit" diagrams.

**TABLE 5. CRYSTAL CHARACTERISTICS**

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		12		38.88	MHz
Equivalent Series Resistance (ESR)				50	$\Omega$
Shunt Capacitance				7	pF
Drive Level				1	mW

**TABLE 6A. AC CHARACTERISTICS,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency	w/external XTAL	12		38.88	MHz
		w/external CLK			200	MHz
$t_{p_{LH}}$	Propagation Delay, Low-to-High; NOTE 1		1.4	1.9	2.4	ns
$t_{sk(o)}$	Output Skew; NOTE 2				40	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 2, 3				700	ps
$t_{jit}(\emptyset)$	RMS Phase Jitter, Random; NOTE 2, 4	25MHz, Integration Range: 100Hz – 1MHz		0.16		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	100		800	ps
odc	Output Duty Cycle	w/external XTAL	45		55	%
		w/external CLK	$f < 150MHz$	46	54	%
$t_{EN}$	Output Enable Time; NOTE 5				10	ns
$t_{DIS}$	Output Disable Time; NOTE 5				10	ns

NOTE 1: Measured from  $V_{DD}/2$  of the input to  $V_{DDO}/2$  of the output.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at  $V_{DDO}/2$ .

NOTE 4: Phase jitter is dependent on the input source used.

NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

**TABLE 6B. AC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency	w/external XTAL	12		38.88	MHz
		w/external CLK			200	MHz
$t_{p_{LH}}$	Propagation Delay, Low-to-High; NOTE 1		1.5	2.0	2.5	ns
$t_{sk(o)}$	Output Skew; NOTE 2				40	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 2, 3				700	ps
$t_{jit}(\emptyset)$	RMS Phase Jitter, Random; NOTE 2, 4	25MHz, Integration Range: 100Hz - 1MHz		0.16		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	100		800	ps
odc	Output Duty Cycle	w/external XTAL	45		55	%
		w/external CLK	$f < 150MHz$	46	54	%
$t_{EN}$	Output Enable Time; NOTE 5				10	ns
$t_{DIS}$	Output Disable Time; NOTE 5				10	ns

NOTE 1: Measured from  $V_{DD}/2$  of the input to  $V_{DDO}/2$  of the output.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at  $V_{DDO}/2$ .

NOTE 4: Phase jitter is dependent on the input source used.

NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

**TABLE 6C. AC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency	w/external XTAL	12		38.88	MHz
		w/external CLK			200	MHz
$t_{p_{LH}}$	Propagation Delay, Low-to-High; NOTE 1		1.7	2.2	2.7	ns
$t_{sk(o)}$	Output Skew; NOTE 2				40	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 2, 3				700	ps
$t_{jit}(\emptyset)$	RMS Phase Jitter, Random; NOTE 2, 4	25MHz, Integration Range: 100Hz - 1MHz		0.16		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	100		1000	ps
odc	Output Duty Cycle	w/external XTAL	45		55	%
		w/external CLK	$f < 150MHz$	46		54
$t_{EN}$	Output Enable Time; NOTE 5				10	ns
$t_{DIS}$	Output Disable Time; NOTE 5				10	ns

NOTE 1: Measured from  $V_{DD}/2$  of the input to  $V_{DDO}/2$  of the output.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at  $V_{DDO}/2$ .

NOTE 4: Phase jitter is dependent on the input source used.

NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

**TABLE 6D. AC CHARACTERISTICS,  $V_{DD} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency	w/external XTAL	12		38.88	MHz
		w/external CLK			200	MHz
$t_{p_{LH}}$	Propagation Delay, Low-to-High; NOTE 1		1.5	2.2	3.0	ns
$t_{sk(o)}$	Output Skew; NOTE 2				40	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 2, 3				700	ps
$t_{jit}(\emptyset)$	RMS Phase Jitter, Random; NOTE 2, 4	25MHz, Integration Range: 100Hz - 1MHz		0.20		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	100		800	ps
odc	Output Duty Cycle	w/external XTAL	45		55	%
		w/external CLK	$f < 150MHz$	48		52
$t_{EN}$	Output Enable Time; NOTE 5				10	ns
$t_{DIS}$	Output Disable Time; NOTE 5				10	ns

NOTE 1: Measured from  $V_{DD}/2$  of the input to  $V_{DDO}/2$  of the output.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at  $V_{DDO}/2$ .

NOTE 4: Phase jitter is dependent on the input source used.

NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

**TABLE 6E. AC CHARACTERISTICS,  $V_{DD} = 2.5V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency	w/external XTAL	12		38.88	MHz
		w/external CLK			200	MHz
$t_{p_{LH}}$	Propagation Delay, Low-to-High; NOTE 1		1.7	2.5	3.3	ns
$t_{sk(o)}$	Output Skew; NOTE 2				40	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 2, 3				700	ps
$t_{jit(\emptyset)}$	RMS Phase Jitter, Random; NOTE 2, 4	25MHz, Integration Range: 100Hz - 1MHz		0.19		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	100		1000	ps
odc	Output Duty Cycle	w/external XTAL	45		55	%
		w/external CLK	$f < 150MHz$	46		54
$t_{EN}$	Output Enable Time; NOTE 5				10	ns
$t_{DIS}$	Output Disable Time; NOTE 5				10	ns

NOTE 1: Measured from  $V_{DD}/2$  of the input to  $V_{DDO}/2$  of the output.

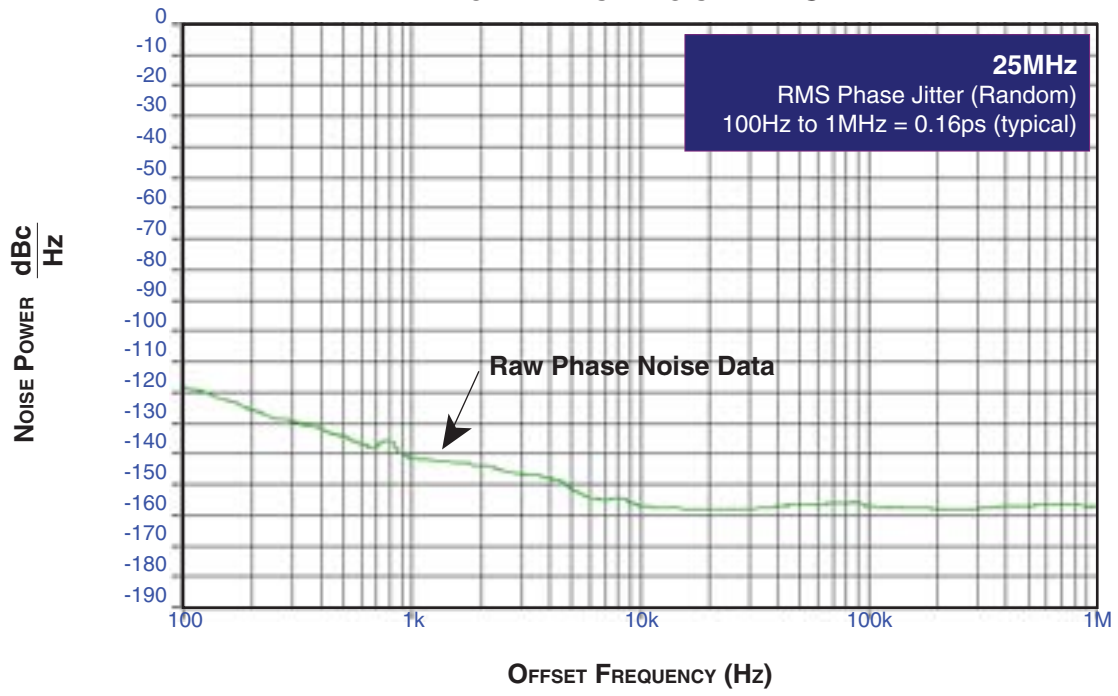
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at  $V_{DDO}/2$ .

NOTE 4: Phase jitter is dependent on the input source used.

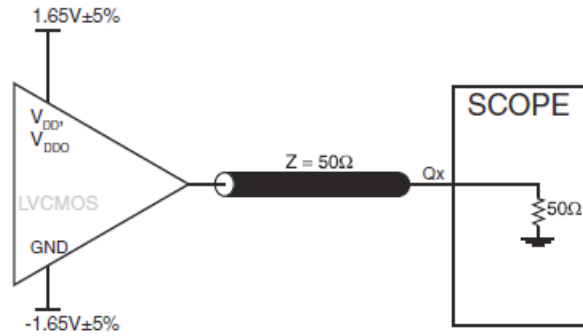
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

TYPICAL PHASE NOISE AT 25MHz

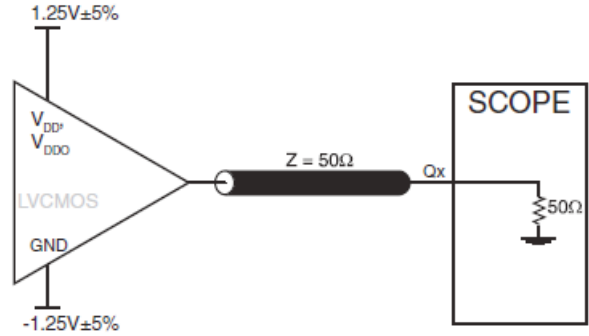




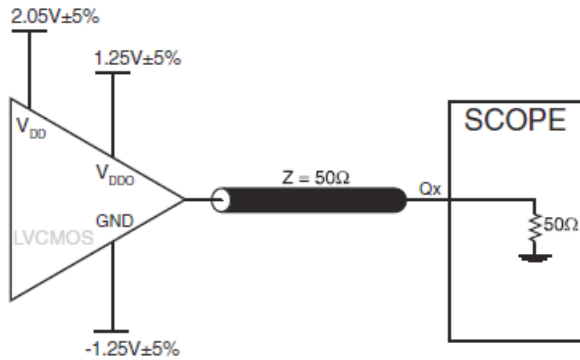
## PARAMETER MEASUREMENT INFORMATION



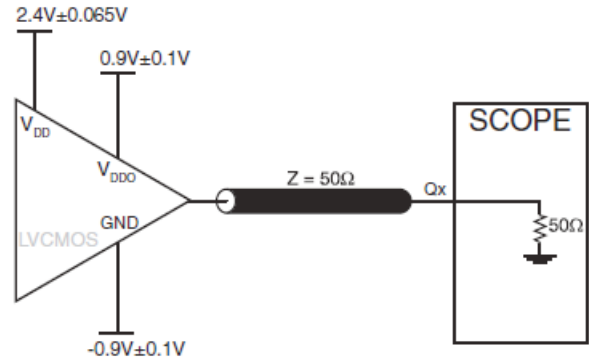
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



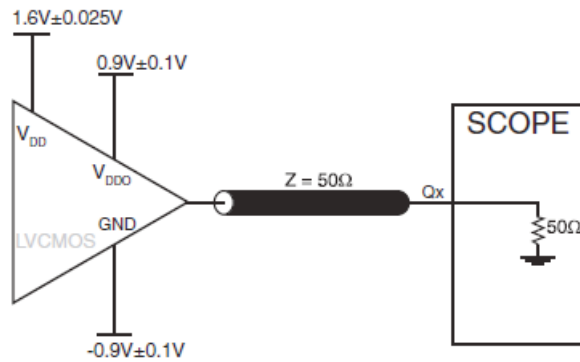
2.5V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



3.3V CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT

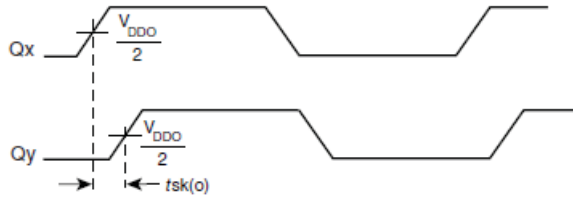


2.5V CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT

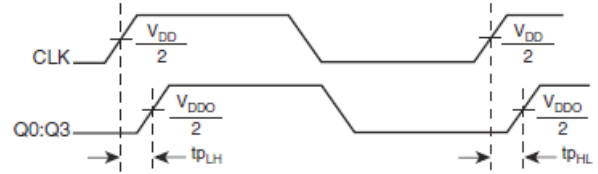


PART-TO-PART SKEW

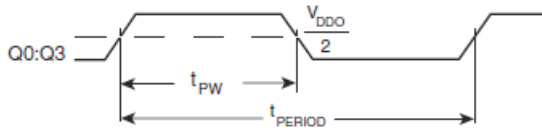
## PARAMETER MEASUREMENT INFORMATION, CONTINUED



OUTPUT SKEW

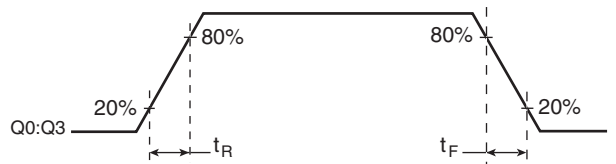


PROPAGATION DELAY



$$\text{odc} = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME

## APPLICATION INFORMATION

### RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

#### INPUTS:

##### CRYSTAL INPUTS

For applications not requiring the use of the crystal oscillator input, both XTAL\_IN and XTAL\_OUT can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from XTAL\_IN to ground.

##### CLK INPUT

For applications not requiring the use of the clock input, it can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from the CLK input to ground.

##### SELECT PINS

All select pins have internal pull-ups and pull-downs; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.

#### OUTPUTS:

##### LVC MOS OUTPUTS

All unused LVC MOS output can be left floating. There should be no trace attached.

## CRYSTAL INPUT INTERFACE

Figure 1 shows an example of 83904-02 crystal interface with a parallel resonant crystal. The frequency accuracy can be fine tuned by adjusting the C1 and C2 values. For a parallel crystal with loading capacitance  $C_L = 18\text{pF}$ , we suggest  $C_1 = 15\text{pF}$  and  $C_2 = 15\text{pF}$  to start with. These values may be slightly fine tuned further to optimize the frequency accuracy for different board layouts. Slightly increasing the C1 and C2 values will slightly reduce the frequency. Slightly decreasing the C1 and C2 values will slightly increase the frequency. For the oscillator circuit below, R1 can be used, but is not required. For new designs, it is recommended that R1 not be used.

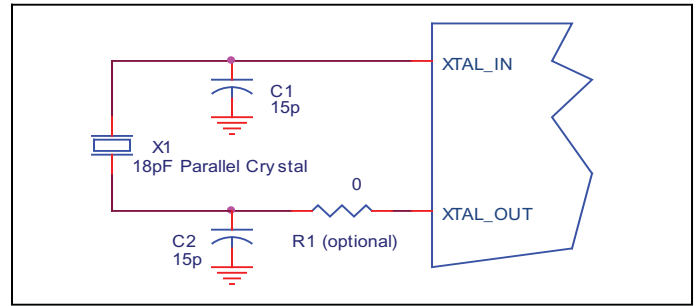


FIGURE 1. CRYSTAL INPUT INTERFACE

## OVERDRIVING THE CRYSTAL INTERFACE

The XTAL\_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in Figure 2A. The XTAL\_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver ( $R_o$ ) plus the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched

termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most  $50\Omega$  applications, R1 and R2 can be  $100\Omega$ . This can also be accomplished by removing R1 and making R2  $50\Omega$ . By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

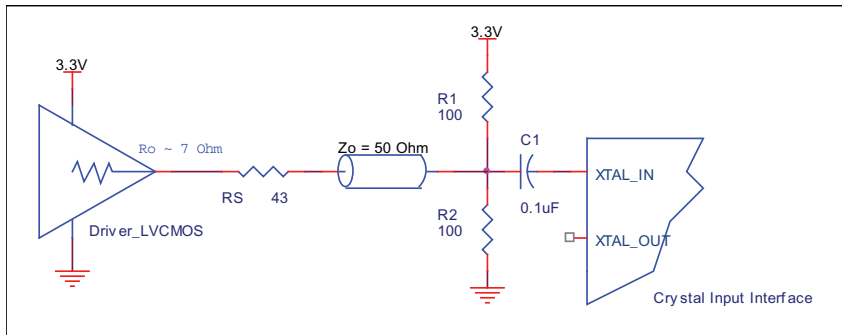


FIGURE 2A. GENERAL DIAGRAM FOR LVCMOS DRIVER TO XTAL INPUT INTERFACE

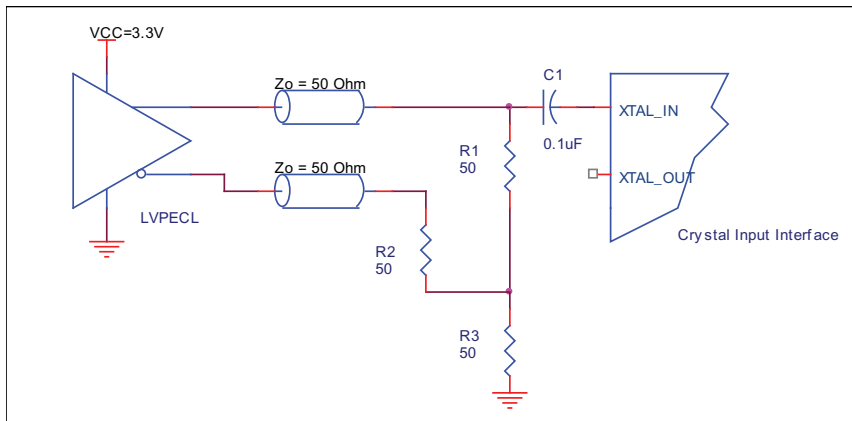


FIGURE 2A. GENERAL DIAGRAM FOR LVPECL DRIVER TO XTAL INPUT INTERFACE

## RELIABILITY INFORMATION

TABLE 7.  $\theta_{JA}$  VS. AIR FLOW TABLE FOR 16 LEAD TSSOP

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	100.3°C/W	96.0°C/W	93.9°C/W

### TRANSISTOR COUNT

The transistor count for 83904-02 is: 205

PACKAGE OUTLINE - G SUFFIX FOR 16 LEAD TSSOP

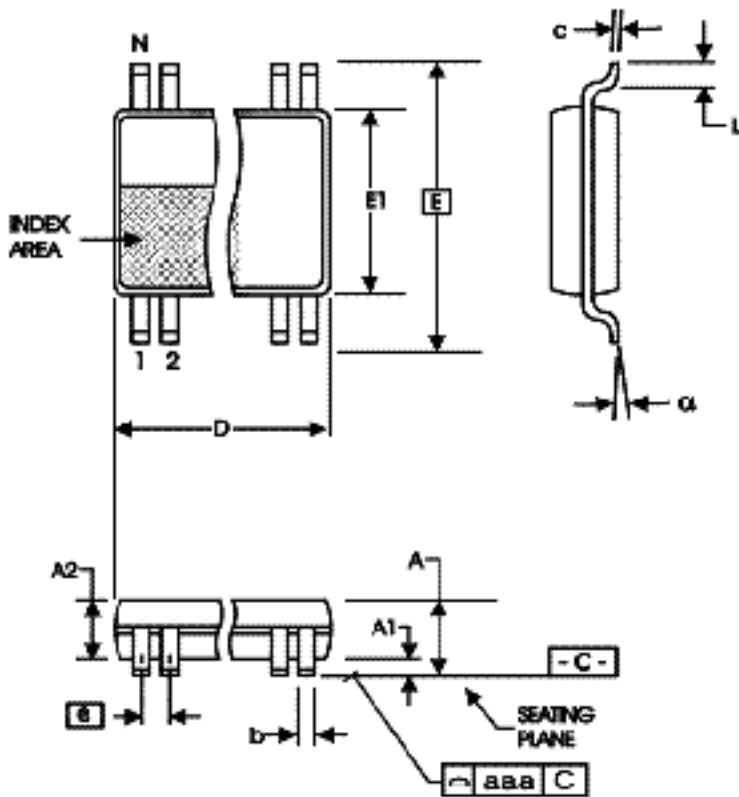


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	16	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
alpha	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

**TABLE 9. ORDERING INFORMATION**

<b>Part/Order Number</b>	<b>Marking</b>	<b>Package</b>	<b>Shipping Packaging</b>	<b>Temperature</b>
83904AG-02LF	3904A02L	16 Lead "Lead-Free" TSSOP	tube	0°C to 70°C
83904AG-02LFT	3904A02L	16 Lead "Lead-Free" TSSOP	tape & reel	0°C to 70°C

REVISION HISTORY SHEET				
Rev	Table	Page	Description of Change	Date
A	T9	12 14	Updated Overdriving the Crystal Interface section. Ordering Information Table - deleted the "ICS" prefix in the Part/Order Number column and corrected the Temperature column. Updated header/footer.	9/3/10
A	T9	14	Ordering Information - Removed leaded devices. Updated data sheet format.	3/25/15
A	T9	14	Ordering Information - Deleted LF note below table. Updated header and footer.	3/17/16





## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit [www.renesas.com/contact-us/](http://www.renesas.com/contact-us/).