FemtoClocks™ Crystal-to-3.3V LVPECL Frequency Synthesizer

843001-21

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DATA SHEET

Description

The 843001-21 is a a highly versatile, low phase noise LVPECL Synthesizer which can generate low jitter reference clocks for a variety of communications applications. The dual crystal interface allows the synthesizer to support up to two communications standards in a given application (i.e. 1GB Ethernet with a 25MHz crystal and 1Gb Fibre Channel using a 26.5625MHz crystal). The rms phase jitter performance is typically less than 1ps, thus making the device acceptable for use in demanding applications such as OC48 SONET and 10Gb Ethernet. The 843001-21 is packaged in a small 24-pin TSSOP package.

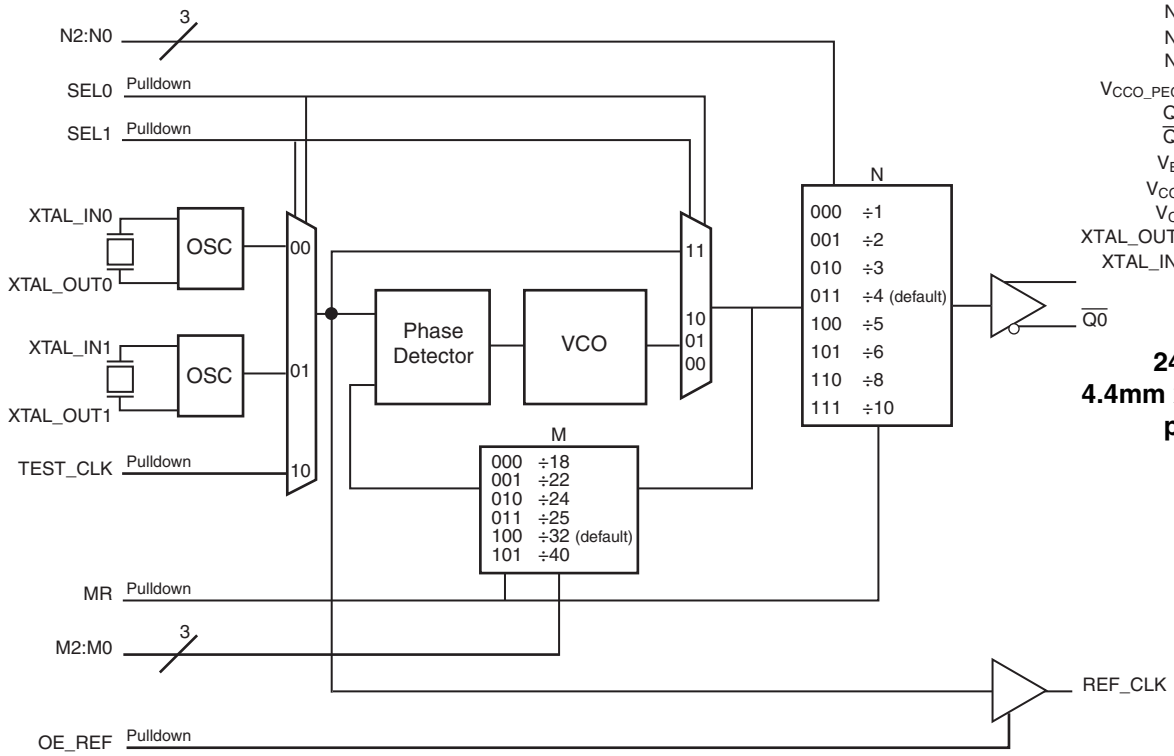
Features

- One 3.3Vdifferential LVPECL output pair and one LVCMOS/LVTTL single-ended reference clock output
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input
- VCO range: 560MHz – 700MHz
- Supports the following applications: SONET, Ethernet, Fibre Channel, Serial ATA, and HDTV
- Selectable ÷1 or ÷2 operation
- RMS phase jitter @ 622.08MHz (12kHz - 20MHz): 0.80ps (typical)

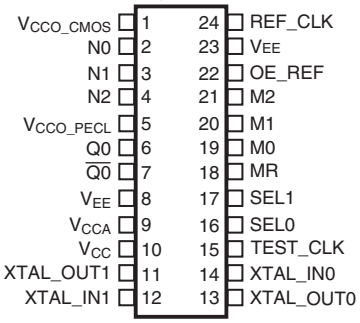
Offset	Noise Power
100Hz	-60.3 dBc/Hz
1kHz	-88.5 dBc/Hz
10kHz	-111.9 dBc/Hz
100kHz	-113.0 dBc/Hz

- Full 3.3V supply mode
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package
- For drop in replacement use 843001i-22

Block Diagram



Pin Assignment



843001-21

24-Lead TSSOP
4.4mm x 7.8mm x 0.925mm package body
G Package
Top View

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Table 1. Pin Descriptions

Number	Name	Type		Description
1	V_{CCO_CMOS}	Power		Output supply pin for REF_CLK output.
2, 3	N0, N1	Input	Pullup	Output divider select pins. Default ÷4. LVCMOS/LVTTL interface levels. See Table 3C.
4	N2	Input	Pulldown	
5	V_{CCO_PECL}	Power		Output supply pin for LVPECL output.
6, 7	Q0, $\overline{Q0}$	Output		Differential output pair. LVPECL interface levels.
8, 23	V_{EE}	Power		Negative supply pins.
9	V_{CCA}	Power		Analog supply pin.
10	V_{CC}	Power		Core supply pin.
11, 12	XTAL_OUT1, XTAL_IN1	Input		Parallel resonant crystal interface. XTAL_OUT1 is the output, XTAL_IN1 is the input.
13, 14	XTAL_OUT0, XTAL_IN0	Input		Parallel resonant crystal interface. XTAL_OUT0 is the output, XTAL_IN0 is the input.
15	TEST_CLK	Input	Pulldown	LVCMOS/LVTTL clock input.
16, 17	SEL0, SEL1	Input	Pulldownp	Input MUX select pins. LVCMOS/LVTTL interface levels. See Table 3D.
18	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true output Q0 to go low and the inverted output $\overline{Q0}$ to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
19, 20	M0, M1	Input	Pulldown	Feedback divider select pins. Default ÷32. See Table 3B LVCMOS/LVTTL interface levels.
21	M2	Input	Pullup	
22	OE_REF	Input	Pulldown	Reference clock output enable. Default Low. LVCMOS/LVTTL interface levels.
24	REF_CLK	Output		Reference clock output. LVCMOS/LVTTL interface levels.

NOTE: *Pullup and Pulldown* refer to intenal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{OUT}	Output Impedance			7		Ω

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Function Tables

Table 3A. Common Configuration Table

Input Reference Clock (MHz)	M Divider Value	N Divider Value	VCO (MHz)	Output Frequency (MHz)	Application
27	22	8	594	74.25	HDTV
24.75	24	8	594	74.25	HDTV
14.8351649	40	8	593.4066	74.1758245	HDTV
19.44	32	4	622.08	155.52	SONET
19.44	32	8	622.08	77.76	SONET
19.44	32	1	622.08	622.08	SONET
19.44	32	2	622.08	311.04	SONET
19.53125	32	4	625	156.25	10 GigE
25	25	5	625	125	1 GigE
25	25	10	625	62.5	1 GigE
25	24	6	600	100	PCI Express
25	24	4	600	150	SATA
25	24	8	600	75	SATA
26.5625	24	6	637.5	106.25	Fibre Channel 1
26.5625	24	3	637.5	212.5	4 Gig Fibre Channel
26.5625	24	4	637.5	159.375	10 Gig Fibre Channel
31.25	18	5	562.5	187.5	12 GigE

Table 3B. Programmable M Output Divider Function Table

Inputs			M Divider Value	Input Frequency (MHz)	
M2	M1	M0		Minimum	Maximum
0	0	0	18	31.1	38.9
0	0	1	22	25.5	31.8
0	1	0	24	23.3	29.2
0	1	1	25	22.4	28.0
1	0	0	32	17.5	21.9
1	0	1	40	14.0	17.5

Table 3C. Programmable N Output Divider Function Table

Inputs			M Divider Value
N2	N1	N0	
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5

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Inputs			M Divider Value
N2	N1	N0	
1	0	1	6
1	1	0	8
1	1	1	10

Table 3D. Bypass Mode Function Table

Inputs		Reference	PLL Mode
SEL1	SEL0		
0	0	XTAL0	1
0	1	XTAL1	2
1	0	TEST_CLK	8
1	1	TEST_CLK1	10

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Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characterisitcs* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O (LVPECL) Continuous Current Surge Current Outputs, V_O (LVCMOS)	 50mA 100mA -0.5V to V_{CCO_CMOS} + 0.5V
Package Thermal Impedance, θ_{JA}	70°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO_CMOS} = V_{CCO_PECL} = 3.3V \pm 5\%$, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{CCO_PECL}, V_{CCO_CMOS}	Output Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				170	mA
I_{CCA}	Analog Supply Current				11	mA
I_{CCO_PECL}, I_{CCO_CMOS}	Output Supply Current				8	mA

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Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO_CMOS} = 3.3V \pm 5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage	SEL0, SEL1, OE_REF, N0:N2, MR, M0:M2		-0.3		0.8	V
		TEST_CLK		-0.3		1.3	V
I_{IH}	Input High Current	TEST_CLK, M0, M1, N2, MR, OE_REF, SEL0, SEL1	$V_{CC} = V_{IN} = 3.465V$			150	µA
		M2, N0, N1	$V_{CC} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	TEST_CLK, M0, M1, N2, MR, OE_REF, SEL0, SEL1	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-5			µA
		M2, N0, N1	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-150			µA
V_{OH}	Output High Voltage: NOTE 1	REF_CLK		2.6			V
V_{OL}	Output Low Voltage: NOTE 1	REF_CLK				0.5	V

NOTE 1: Output terminated with 50Ω to $V_{CCO_CMOS}/2$. See Parameter Measurement Information Section, ""3.3V LVCMOS Output Load Test Circuit Diagram"".

Table 4C. LVPECL DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO_PECL} = 3.3V \pm 5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Current; NOTE 1		$V_{CCO} – 1.4$		$V_{CCO} – 0.9$	µA
V_{OL}	Output Low Current; NOTE 1		$V_{CCO} – 2.0$		$V_{CCO} – 1.7$	µA
V_{SWING}	Peak-toPeak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs termination with 50Ω to $V_{CCO_PECL} – 2V$.

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		12		40	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

NOTE: Characterized using an 18pF parallel resonant crystal.

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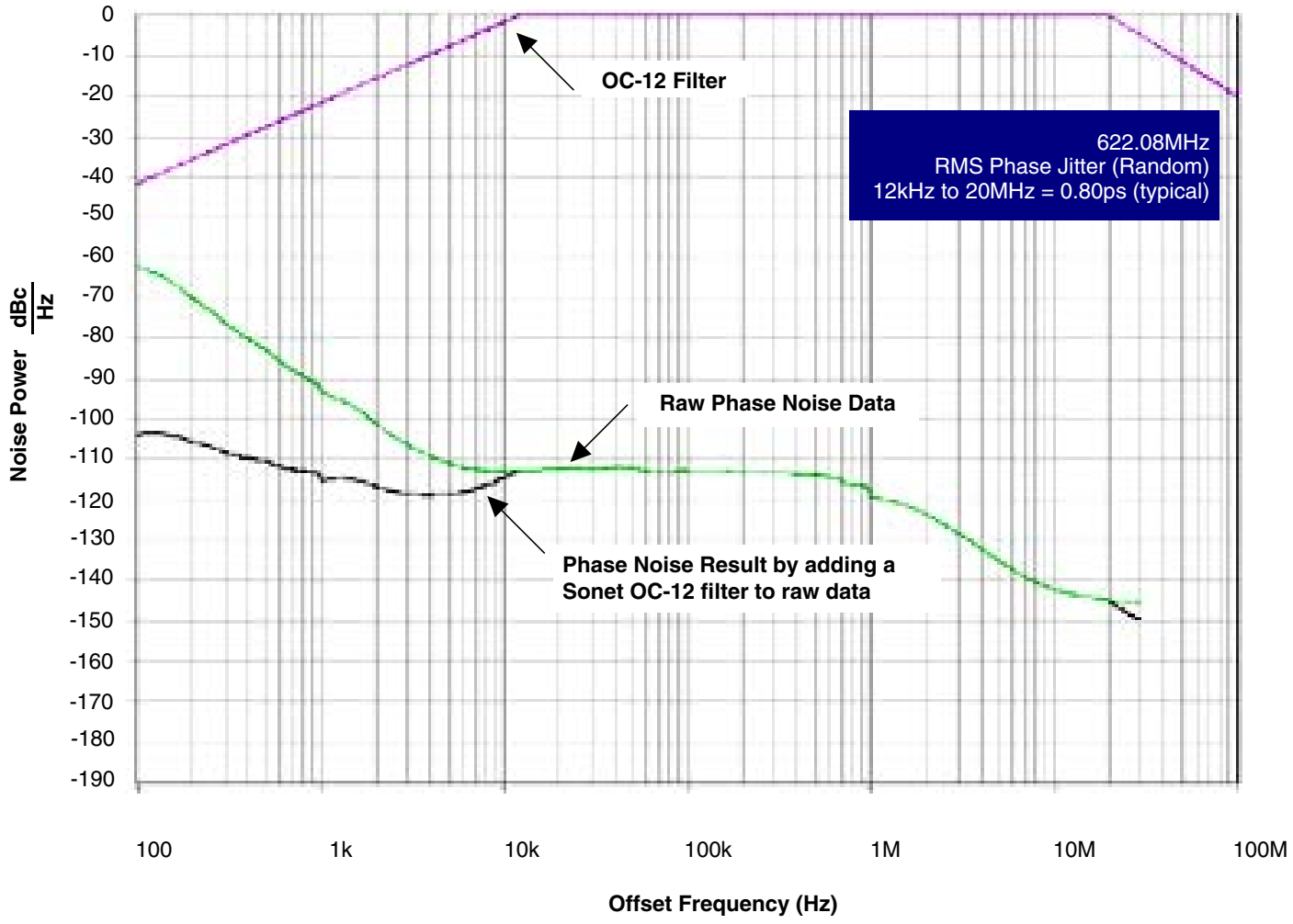
AC Electrical Characteristics

Table 6. AC Characteristics, $V_{CC} = V_{CCA} = V_{CCO_CMOS} = V_{CCO_PECL} = 3.3V \pm 5\%$, $T_A = 0°C$ to $70°C$

Parameter	Symbol		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			56		700	MHz
t_{PD}	Propagation Delay; NOTE 1	TEST_CLK to REF_CLK		2.3		2.8	ns
ϕjit(Ø)	RMS Phase Jitter, (Random); NOTE 2, 3		622.08MHz, (12kHz – 20MHz)		0.80		ps
t_{VCO}	PLL VCO Lock Range			560		700	MHz
t_R / t_F	Output Rise/Fall Time	Q0, $\overline{Q0}$	20% to 80%	200		500	ps
		REF_CLK	20% to 80%	300		800	ps
odc	Output Duty Cycle	Q0, $\overline{Q0}$		45		55	%
		REF_CLK		44		56	%

NOTE 1: Measured from the $V_{CC}/2$ of the input to $V_{CCO_CMOS}/2$ of the output.
NOTE 2: Phase jitter measured using a 19.44MHz quartz crystal.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

Typical Phase Noise at 622.08MHz



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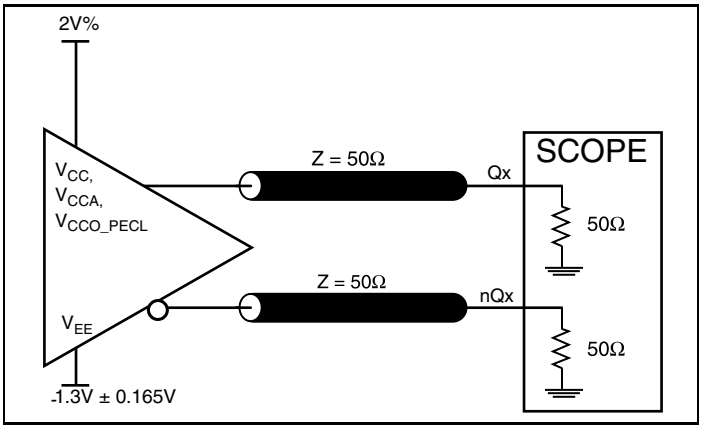
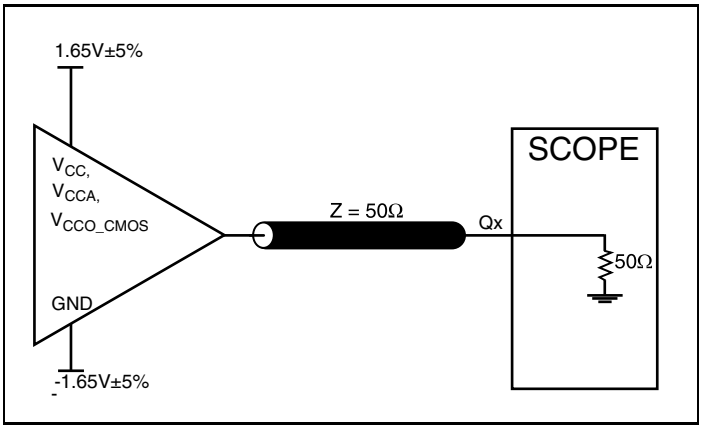
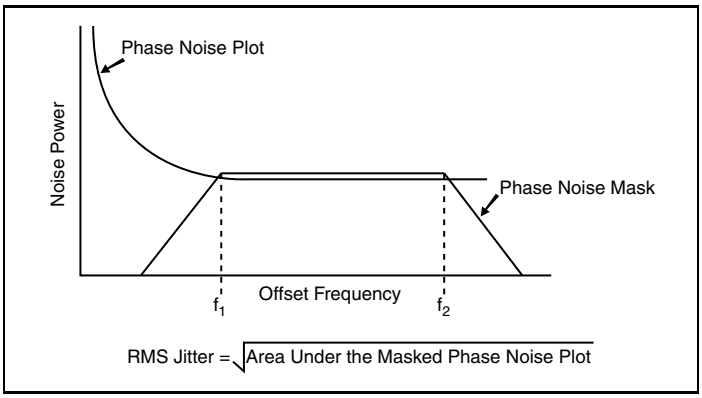
Parameter Measurement Information



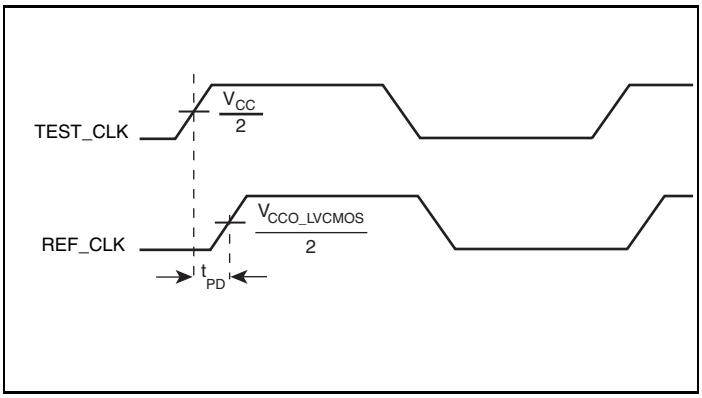
3.3V LVPECL Output Load AC Test Circuit



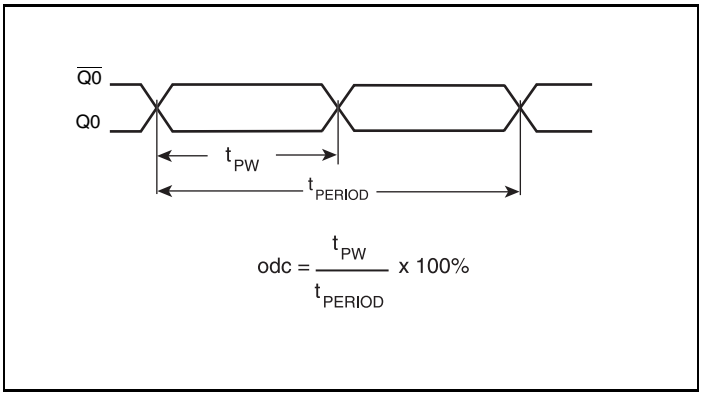
3.3V LVCMOS Output Load AC Test Circuit



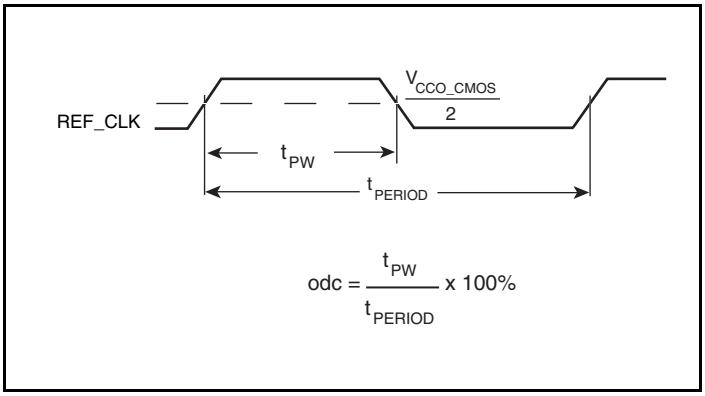
RMS Phase Jitter



Propagation Delay



LVPECL Output Duty Cycle/Pulse Width/Period



LVCMOS Output Duty Cycle/Pulse Width/Period

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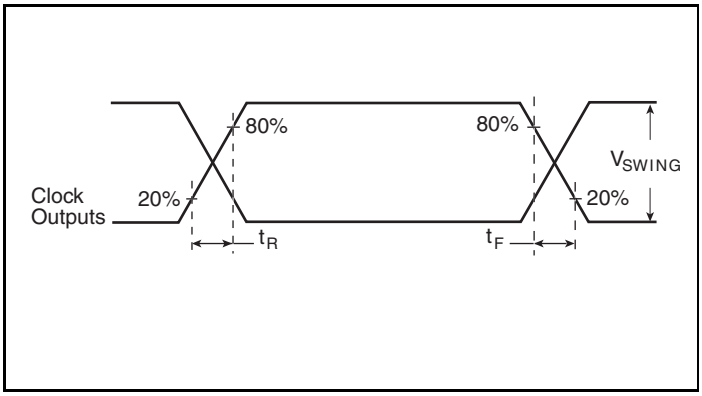
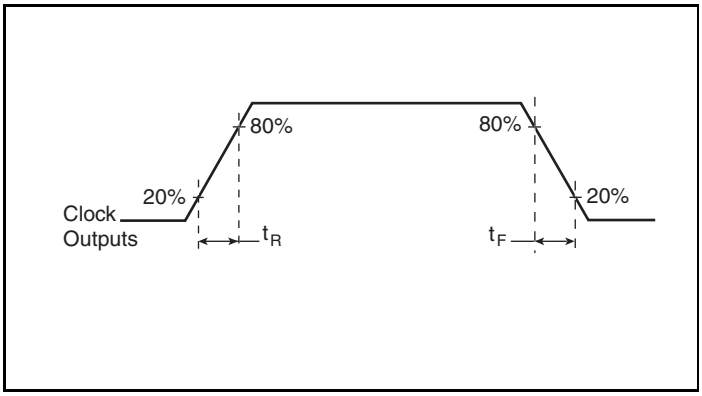
Parameter Measurement Information, continued



LVPECL Output Rise/Fall Time



LVCMOS Output Rise/Fall Time

Application Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The 843001-21 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA} and V_{CCO_x} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10μF and a .01μF bypass capacitor should be connected to each V_{CCA} pin.

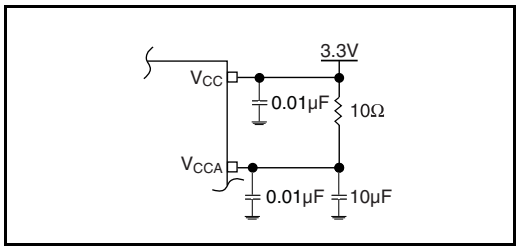


Figure 1. Power Supply Filtering

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Crystal Input Interface

The 843001-21 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 19.44MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

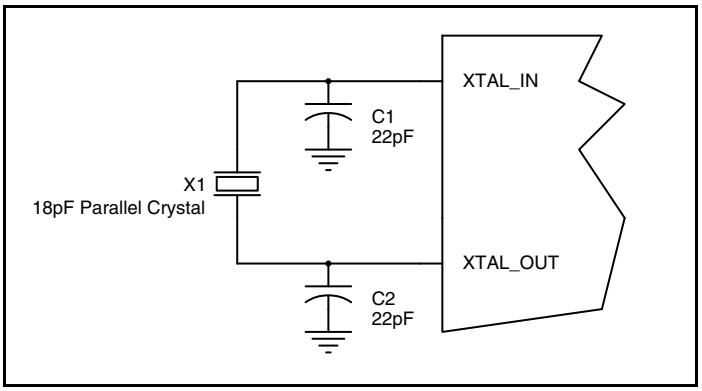

Figure 2. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

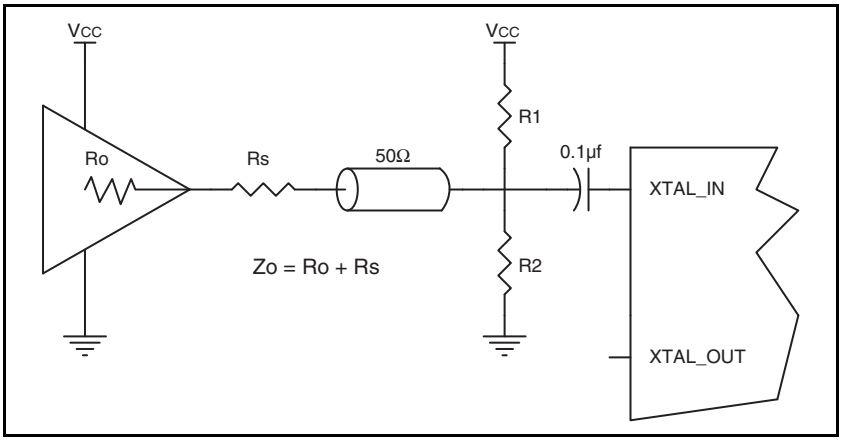

Figure 3. General Disgram for LVCMOS Driver to XTAL Input Interface

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Recommendations for Unused Input and Output Pins

Inputs:

Crystal Inputs:

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

TEST_CLK Input:

For applications not requiring the use of the test clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the TEST_CLK to ground.

LVCMOS Control Pins:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Output:

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVCMOS Output:

All unused LVCMOS output can be left floating. We recommend that there is no trace attached.

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and $\overline{FOUT}$ are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

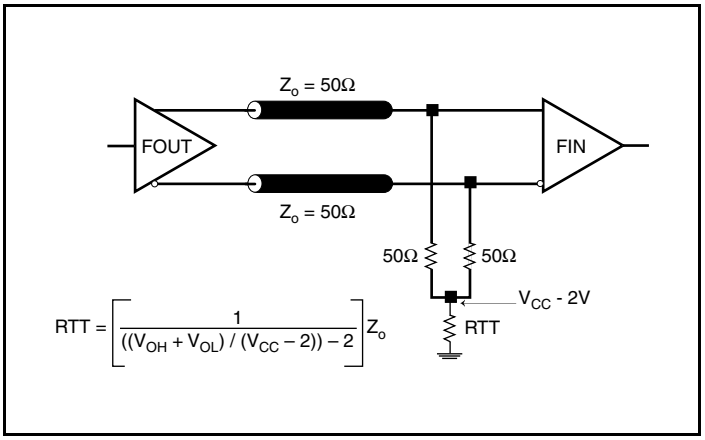

Figure 4A. 3.3V LVPECL Output Termination

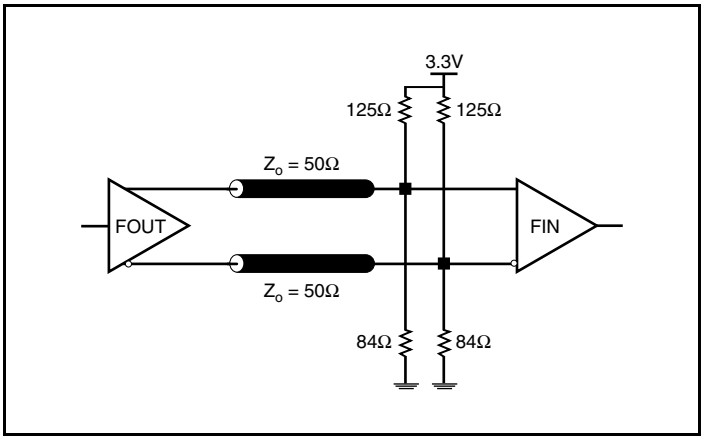

Figure 4B. 3.3V LVPECL Output Termination

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Power Considerations

This section provides information on power dissipation and junction temperature for the ICS843001.21.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 843001-21 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC}= 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 170mA = **589.05mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**

Total Power$_{_MAX}$ (3.3V, with all outputs switching) = 589.05mW + 30mW = **619.05mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 65°C/W per Table 7below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.619W * 65°C/W = 110.2°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 7. Thermal Resitance θ_{JA} for 24 Lead TSSOP, Forced Convection

θ_{JA} **vs. Air Flow**			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65	62

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3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 5.*

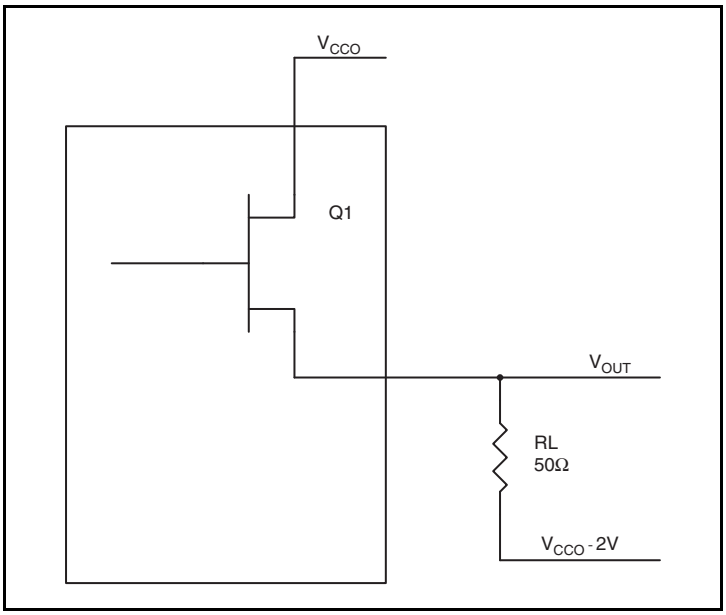

Figure 5. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} - 2V.

- For logic high, $V_{OUT} = V_{OH_MAX} = \mathbf{V_{CCO_MAX} - 0.9V}$
  $(V_{CCO_MAX} - V_{OH_MAX}) = \mathbf{0.9V}$
- For logic low, $V_{OUT} = V_{OL_MAX} = \mathbf{V_{COO_MAX} - 1.7V}$
  $(V_{CCO_MAX} - V_{OL_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd_H = [(V_{OH_MAX} - (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) = [(2V - (V_{CCO_MAX} - V_{OH_MAX}))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd_L = [(V_{OL_MAX} - (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) = [(2V - (V_{CCO_MAX} - V_{OL_MAX}))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

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Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 24 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65	62

Transistor Count

The transistor count for 843001-21 is: 4057

Package Outline and Package Dimension

Package Outline - G Suffix for 24 Lead TSSOP

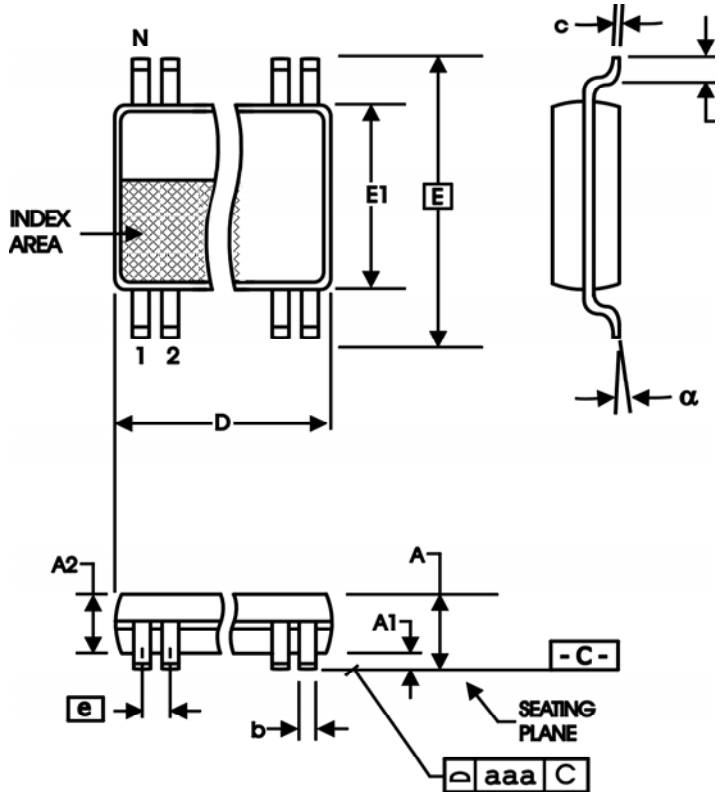

Table 9. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	24	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

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Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
843001AG-21LF	ICS843001A21L	“Lead-Free” 24 Lead TSSOP	Tube	0°C to 70°C
843001AG-21LFT	ICS843001A21L	“Lead-Free” 24 Lead TSSOP	Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T10	1 14	Features Section - added Lead-Free bullet. Ordering Information table - added Lead-Free marking.	2/8/05
A	T3C T10	3 9 10	Programmable N Output Divider Function Table - corrected heading from M Divide Value to N Divide value. Added *Recommendations for Unused Input and Output Pins.* Ordering Information Table - added lead-free note.	10/26/05
A		1 9 10	General Description - corrected crystal frequency from 25.5625MHz crystal to 26.5625MHz crystal. Added *LVCMOS Output RiseFall Time* Diagram. Added *LVCMOS to XTAL Interface* section. Updated format throughout the datasheet.	3/15/07
A	T10	15	Ordering Information - removed leaded devices. Updated data sheet information.	4/6/15
A			Product Discontinuation Notice - Last time buy expires May 6, 2017. PDN CQ-16-01	5/20/16

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