General Description

The 843003 is a 3 differential output LVPECL Synthesizer designed to generate Ethernet refer- ence clock frequencies. Using a 31.25MHz or 26.041666MHz, 18pF parallel resonant crystal, the following frequencies can be generated based on the settings of 4 fre- quency select pins (DIV_SEL[A1:A0], DIV_SEL[B1:B0]): 625MHz, 312.5MHz, 156.25MHz, and 125MHz. The 843003 has 2 output banks, Bank A with 1 differential LVPECL output pair and Bank B with 2 differential LVPECL output pairs.

The two banks have their own dedicated frequency select pins and can be independently set for the frequencies mentioned above. The 843003 uses IDT's 3rd generation low phase noise VCO technology and can achieve 1ps or lower typical rms phase jitter, easily meeting Ethernet jitter requirements. The 843003 is packaged in a small 24-pin TSSOP package.

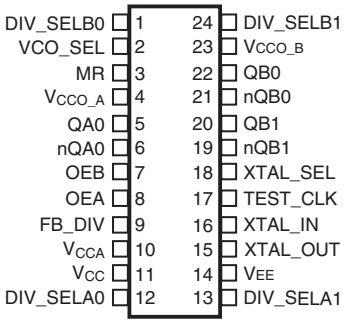
Features

- Three 3.3V LVPECL outputs on two banks, A Bank with one LVPECL pair and B Bank with 2 LVPECL output pairs
- Using a 31.25MHz or 26.041666 crystal, the two output banks can be independently set for 625MHz, 312.5MHz, 156.25MHz or 125MHz
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input
- VCO range: 560MHz – 700MHz
- RMS phase jitter @ 156.25MHz (1.875MHz - 20MHz): 0.51ps (typical)

Offset	Noise Power
100Hz	-96.8 dBc/Hz
1kHz	-119.1 dBc/Hz
10kHz	-126.4 dBc/Hz
100kHz	-127.0 dBc/Hz

- Full 3.3V supply mode
- 0°C to 70°C ambient operating temperature
- Industrial temperature available upon request
- Available in ead-free (RoHS 6) package

Pin Assignment



843003

24-Lead TSSOP
4.4mm x 7.8mm x 0.925mm
package body
G Package

Block Diagram

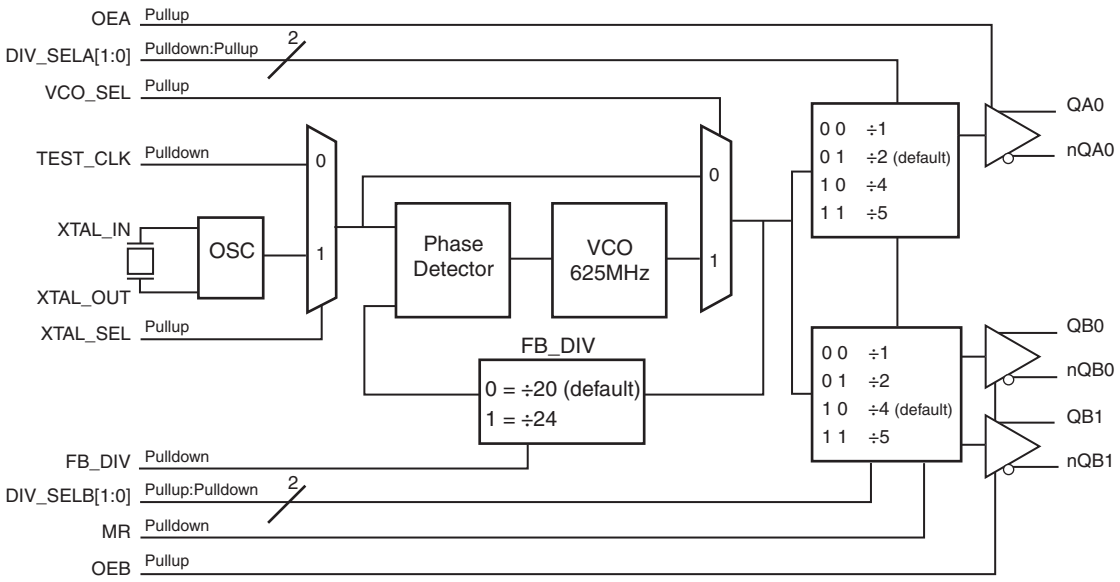


Table 1. Pin Descriptions

Number	Name	Type		Description
1	DIV_SELB0	Input	Pulldown	Division select pin for Bank B. Default = Low. LVCMOS/LVTTL interface levels.
2	VCO_SEL	Input	Pullup	VCO select pin. When Low, the PLL is bypassed and the crystal reference or TEST_CLK (depending on XTAL_SEL setting) are passed directly to the output dividers. Has an internal pullup resistor so the PLL is not bypassed by default. LVCMOS/LVTTL interface levels.
3	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. Has an internal pulldown resistor so the power-up default state of outputs and dividers are enabled. LVCMOS/LVTTL interface levels.
4	V_{CCO_A}	Power		Output supply pin for Bank A outputs.
5, 6	QA0, nQA0	Output		Differential output pair. LVPECL interface levels.
7	OEB	Input	Pullup	Output enable Bank B. Active High output enable. When logic HIGH, the output pair on Bank B is enabled. When logic LOW, the output pair drives differential Low (QB0 = Low, nQB0 = High). Has an internal pullup resistor so the default power-up state of outputs are enabled. LVCMOS/LVTTL interface levels.
8	OEA	Input	Pullup	Output enable Bank A. Active High output enable. When logic HIGH, the 2 output pairs on Bank A are enabled. When logic LOW, the output pair drives differential Low (QA0 = Low, nQA0 = High). Has an internal pullup resistor so the default power-up state of outputs are enabled. LVCMOS/LVTTL interface levels.
9	FB_DIV	Input	Pulldown	Feedback divide select. When Low (default), the feedback divider is set for ÷20. When HIGH, the feedback divider is set for ÷24. LVCMOS/LVTTL interface levels.
10	V_{CCA}	Power		Analog supply pin.
11	V_{CC}	Power		Core supply pin.
12	DIV_SELA0	Input	Pullup	Division select pin for Bank A. Default = HIGH. LVCMOS/LVTTL interface levels.
13	DIV_SELA1	Input	Pulldown	Division select pin for Bank A. Default = Low. LVCMOS/LVTTL interface levels.
14	V_{EE}	Power		Negative supply pin.
15, 16	XTAL_OUT, XTAL_IN	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input. XTAL_IN is also the overdrive pin if you want to overdrive the crystal circuit with a single-ended reference clock.
17	TEST_CLK	Input	Pulldown	Single-ended reference clock input. Has an internal pulldown resistor to pull to low state by default. Can leave floating if using the crystal interface. LVCMOS/LVTTL interface levels.
18	XTAL_SEL	Input	Pullup	Crystal select pin. Selects between the single-ended TEST_CLK or crystal interface. Has an internal pullup resistor so the crystal interface is selected by default. LVCMOS/LVTTL interface levels.
19, 20	nQB1, QB1	Output		Differential output pair. LVPECL interface levels.
21, 22	nQB01, QB0	Output		Differential output pair. LVPECL interface levels.
23	V_{CCO_B}	Power		Output supply pin for Bank B outputs.
24	DIV_SELB1	Input	Pullup	Division select pin for Bank B. Default = High. LVCMOS/LVTTL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3A. Bank A Frequency Table

Inputs				Feedback Divider	Bank A Output Divider	M/N Multiplication Factor	QA0/nQA0 Output Frequency (MHz)
Crystal Frequency (MHz)	DIV_SELA1	DIV_SELA0	FB_DIV				
31.25	0	0	0	20	1	20	625
31.25	0	1	0	20	2	10	312.5
31.25	1	0	0	20	4	5	156.25
31.25	1	1	0	20	5	4	125
26.041666	0	0	1	24	1	24	625
26.041666	0	1	1	24	2	12	312.5
26.041666	1	0	1	24	4	6	156.25
26.041666	1	1	1	24	5	4.8	125

Table 3B. Bank B Frequency Table

Inputs				Feedback Divider	Bank B Output Divider	M/N Multiplication Factor	QBx/nQBx Output Frequency (MHz)
Crystal Frequency (MHz)	DIV_SELB1	DIV_SELB0	FB_DIV				
31.25	0	0	0	20	1	20	625
31.25	0	1	0	20	2	10	312.5
31.25	1	0	0	20	4	5	156.25
31.25	1	1	0	20	5	4	125
26.041666	0	0	1	24	1	24	625
26.041666	0	1	1	24	2	12	312.5
26.041666	1	0	1	24	4	6	156.25
26.041666	1	1	1	24	5	4.8	125

Table 3C. Output Bank Configuration Select Function Table

Inputs		Bank A Output Divider	Inputs		Bank B Output Divider
DIV_SELA1	DIV_SELA0		DIV_SELB1	DIV_SELB0	
0	0	1	0	0	1
0	1	2	0	1	2
1	0	4	1	0	4
1	1	5	1	1	5

Table 3D. Feedback Divider Configuration Select Function Table

Inputs	
FB_DIV	Feedback Divide
0	20
1	24

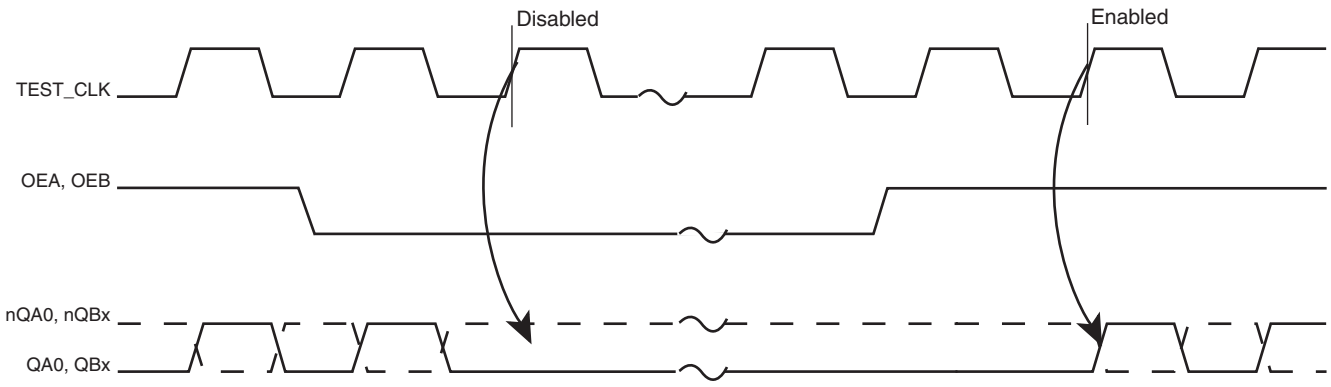


Figure 1. OE Timing Diagram

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O (LVPECL) Continuous Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA}	70°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO\_A} = V_{CCO\_B} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{CCO_A}, V_{CCO_B}	Output Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				158	mA
I_{CCA}	Analog Supply Current				15	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO\_A} = V_{CCO\_B} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	DIV_SEL[A0:A1], FB_DIV, DIV_SEL[B0:B1], OEA, OEB, VCO_SEL, XTAL_SEL, MR		-0.3		0.8	V
		TEST_CLK		-0.3		1.3	V
I_{IH}	Input High Current	TEST_CLK, FB_DIV, MR, DIV_SELA1, DIV_SELB0	$V_{CC} = V_{IN} = 3.465V$			150	µA
		OEA, OEB, VCO_SEL, XTAL_SEL, DIV_SELB1, DIV_SELA0	$V_{CC} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	TEST_CLK, FB_DIV, MR, DIV_SELA1, DIV_SELB0	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-5			µA
		OEA, OEB, VCO_SEL, XTAL_SEL, DIV_SELB1, DIV_SELA0	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-150			µA

Table 4C. LVPECL DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO\_A} = V_{CCO\_B} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ to $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Current; NOTE 1		$V_{CCO} - 1.4$		$V_{CCO} - 0.9$	µA
V_{OL}	Output Low Current; NOTE 1		$V_{CCO} - 2.0$		$V_{CCO} - 1.7$	µA
V_{SWING}	Peak-to-peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs termination with 50Ω to $V_{CCO\_A, \_B} - 2V$.

Table 5. Crystal Characteristics

Parameter		Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental			
Frequency	FB_DIV = ÷20		28	31.25	35	MHz
	FB_DIV = ÷24		23.33	26.04166	29.167	MHz
Equivalent Series Resistance (ESR)					50	Ω
Shunt Capacitance					7	pF

NOTE: Characterized using an 18pF parallel resonant crystal.

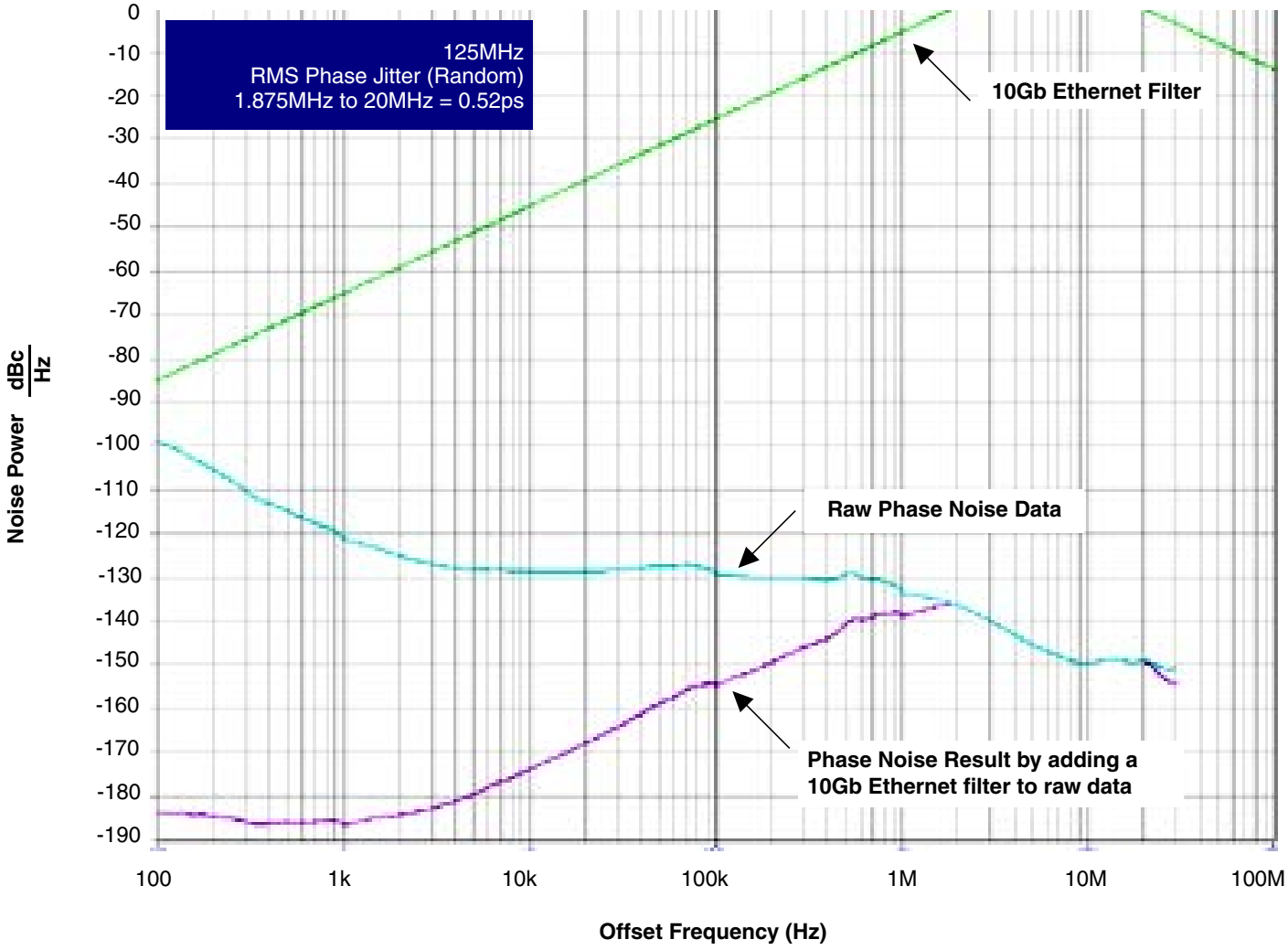
AC Electrical Characteristics

Table 6. AC Characteristics, $V_{CC} = V_{CCA} = V_{CCO\_A} = V_{CCO\_B} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ to $70°C$

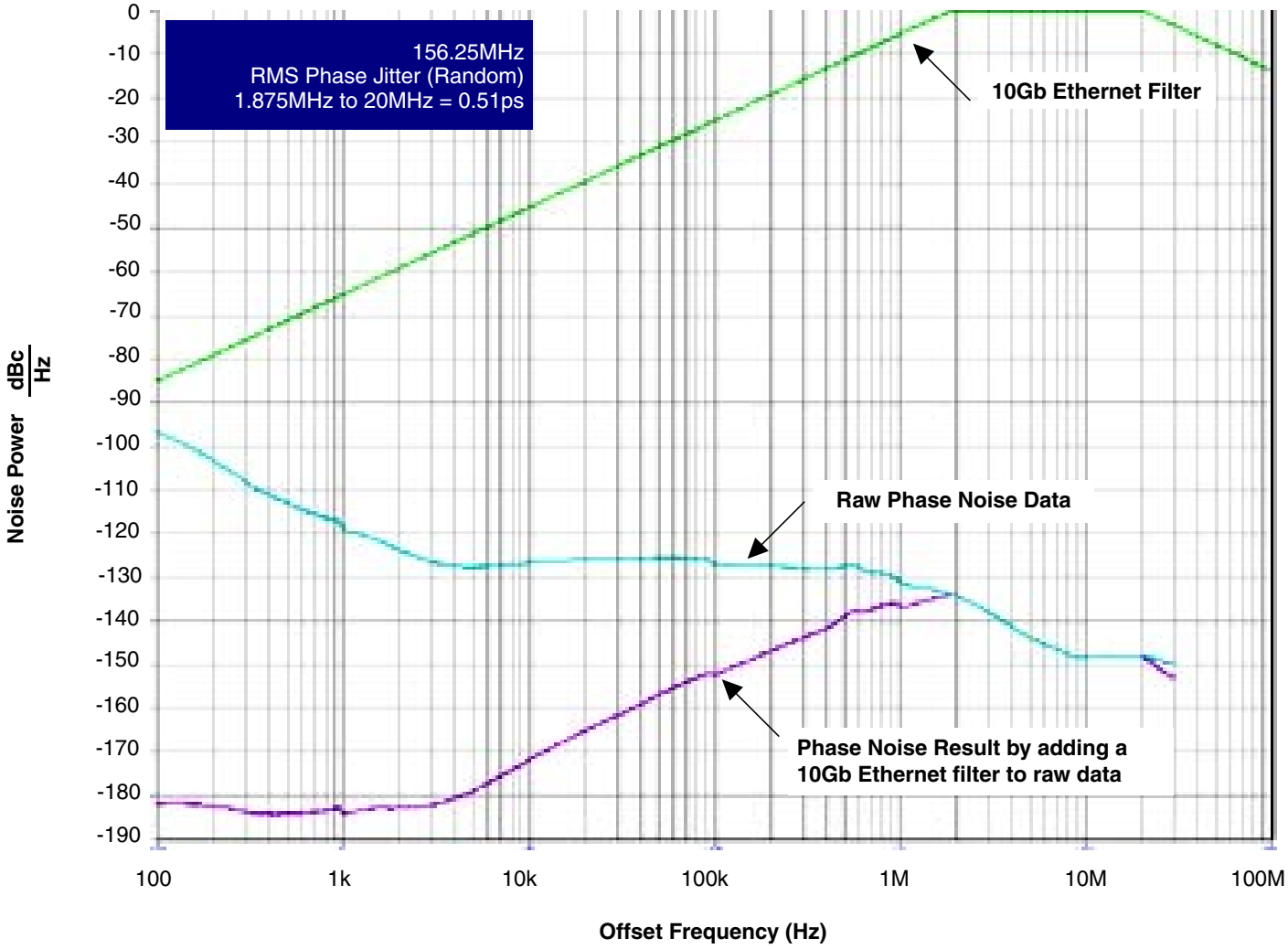
Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	DIV_SELx[1:0] = 00	560		700	MHz
		DIV_SELx[1:0] = 01	280		350	MHz
		DIV_SELx[1:0] = 10	140		175	MHz
		DIV_SELx[1:0] = 11	112		140	MHz
*t*sk(b)	Bank Skew, NOTE 1				20	ps
*t*sk(o)	Output Skew; NOTE 2, 4	Outputs @ Same Frequency			35	ps
		Outputs @ Different Frequencies			100	ps
*t*jit(Ø)	RMS Phase Jitter, (Random); NOTE 3	625MHz, (1.875MHz – 20MHz)		0.42		ps
		312.5MHz, (1.875MHz – 20MHz)		0.50		ps
		156.25MHz, (1.875MHz – 20MHz)		0.51		ps
		125MHz, (1.875MHz – 20MHz)		0.52		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		600	ps
odc	Output Duty Cycle	DIV_SELx[1:0] = 00	40		60	%
		DIV_SELx[1:0] ≠ 00	47		53	%

NOTE 1: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.
NOTE 2: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Please refer to the Phase Noise Plots.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

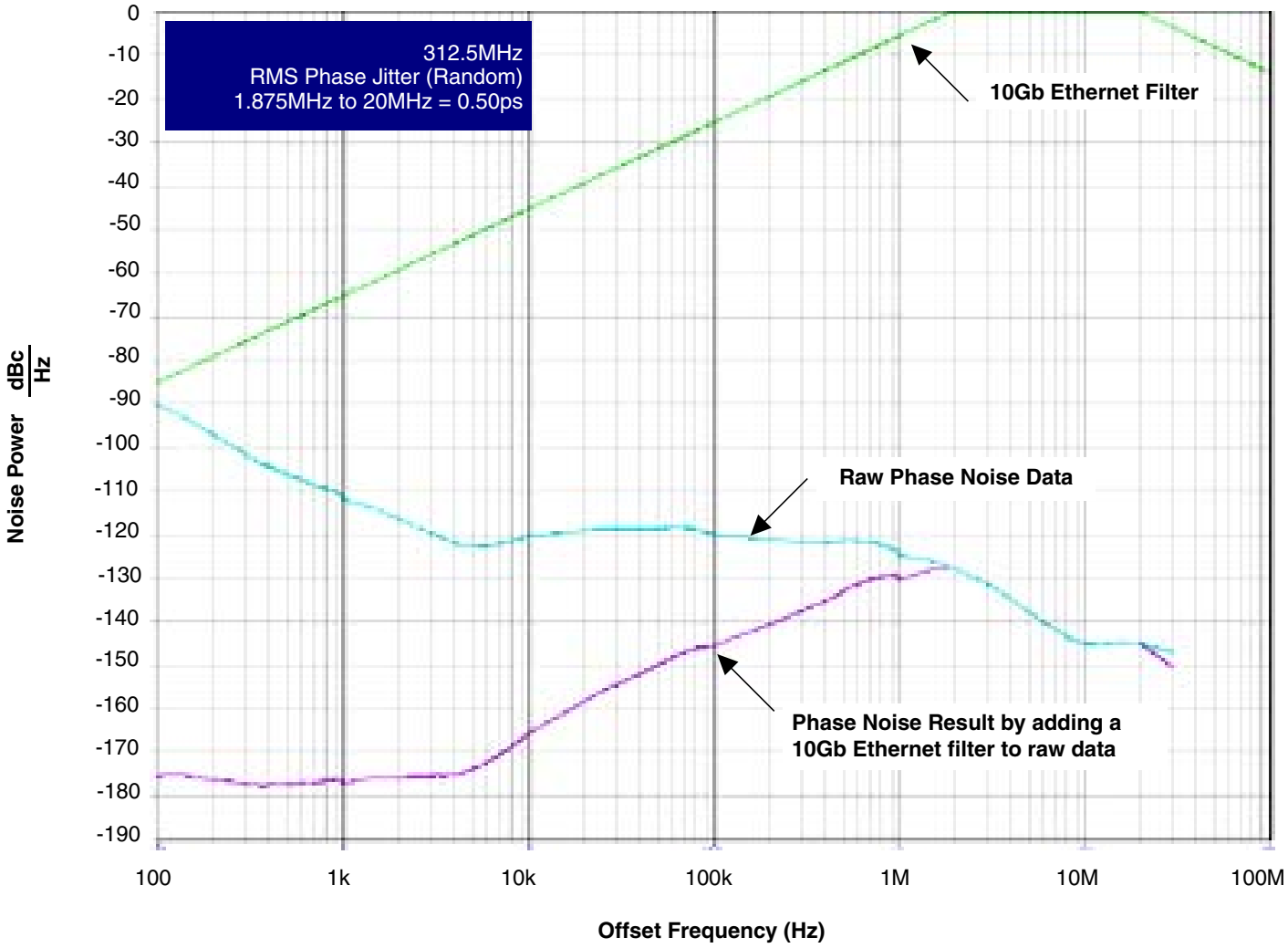
Typical Phase Noise at 125MHz



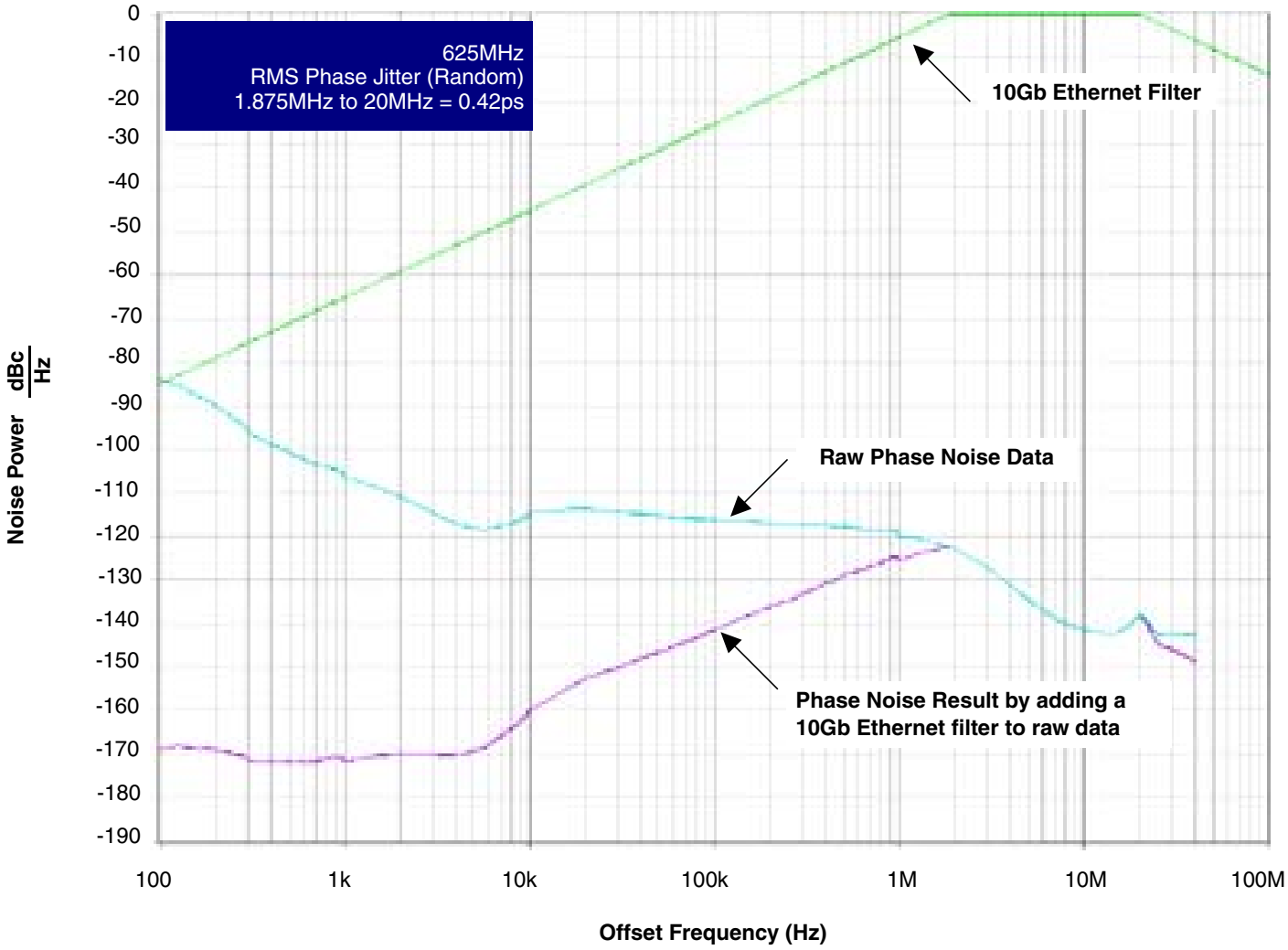
Typical Phase Noise at 156.25MHz



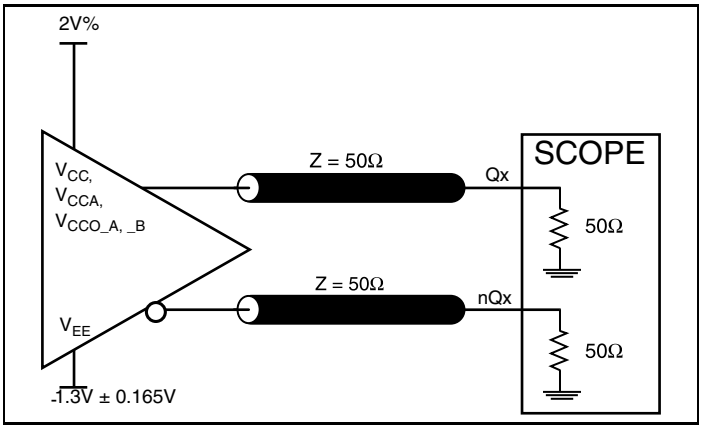
Typical Phase Noise at 312.5MHz



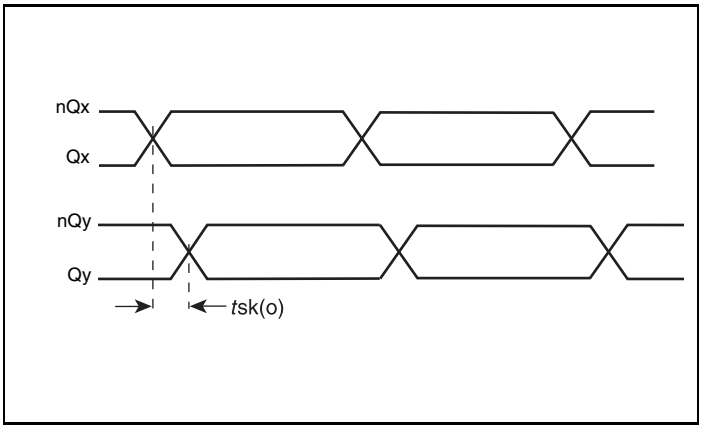
Typical Phase Noise at 625MHz



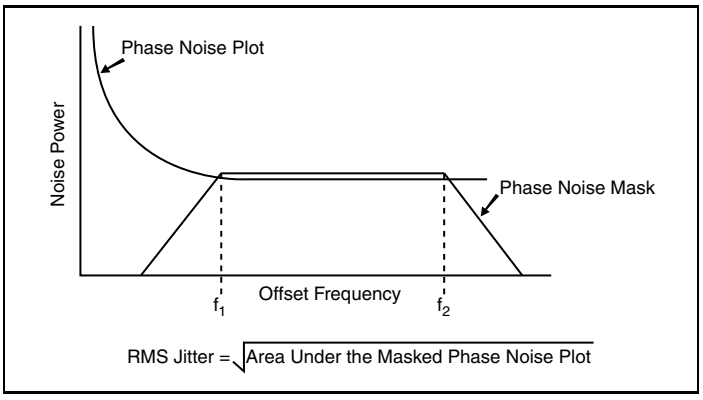
Parameter Measurement Information



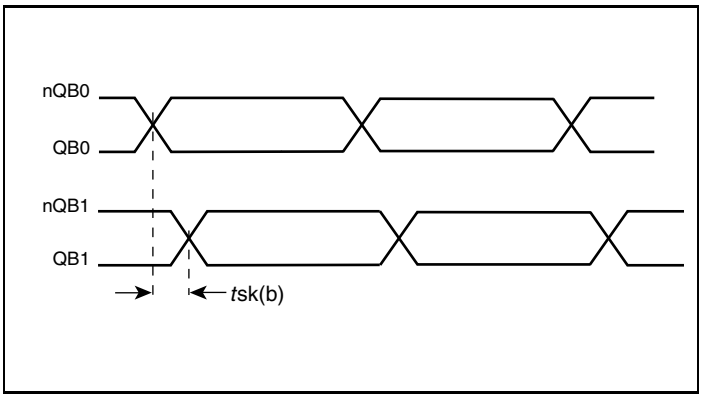
LVPECL Output Load AC Test Circuit



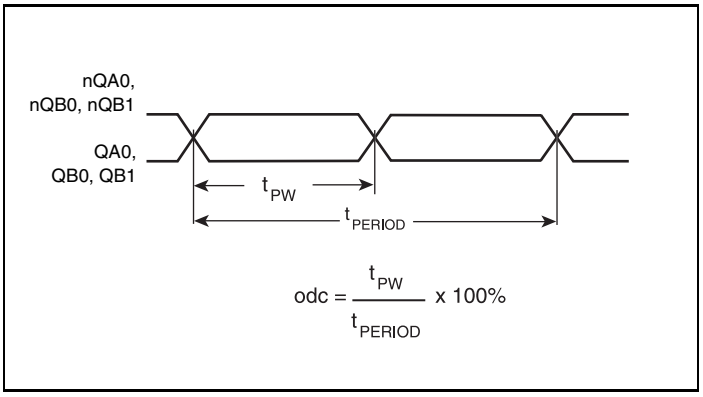
Output Skew



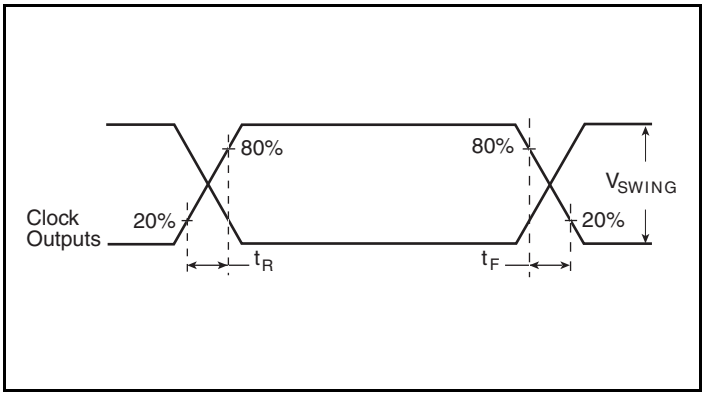
RMS Phase Jitter



Bank Skew



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

Application Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 843003 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA} and V_{CCO_x} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 2* illustrates this for a generic V_{CC} pin and also shows that V_{CCA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{CCA} pin.

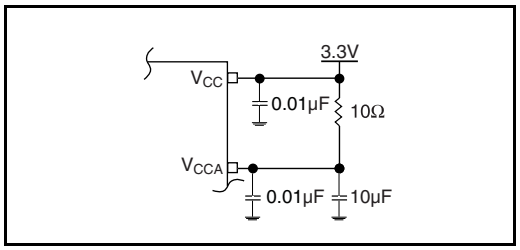


Figure 2. Power Supply Filtering

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

TEST_CLK Input

For applications not requiring the use of the test clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the TEST_CLK to ground.

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Crystal Input Interface

The 843003 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 3* below were determined using a 31.25MHz or 26.041666MHz 18pF parallel resonant crystal and were chosen to minimize the ppm error.

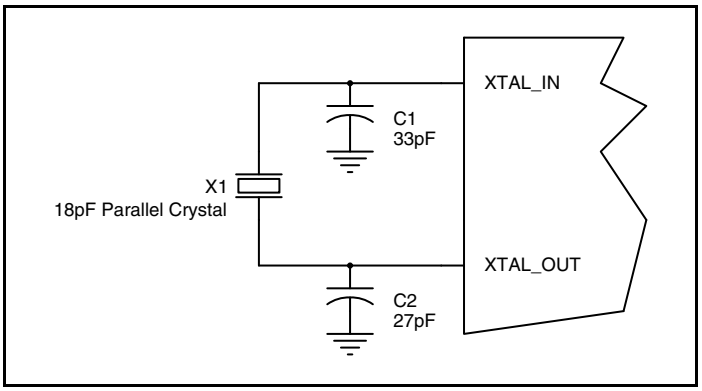


Figure 3. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 4.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

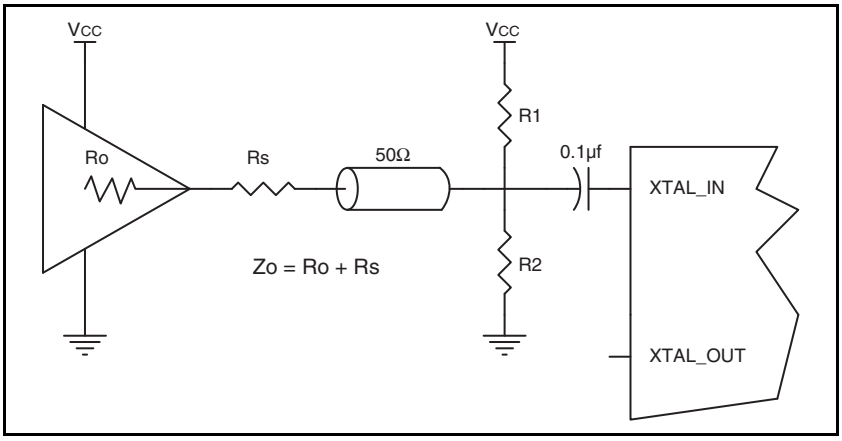


Figure 4. General Diagram for LVCMOS Driver to XTAL Input Interface

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 5A and 5B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

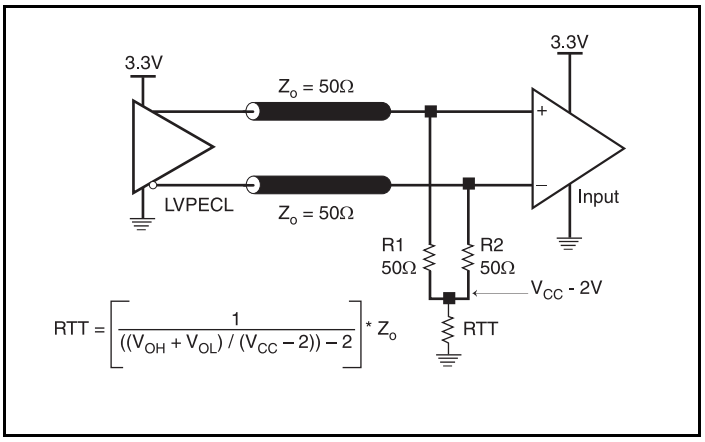


Figure 5A. 3.3V LVPECL Output Termination

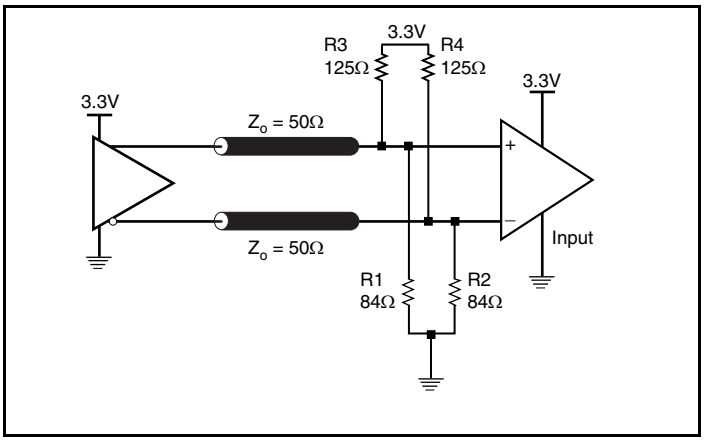


Figure 5B. 3.3V LVPECL Output Termination

Layout Guideline

Figure 6A shows a schematic example of the 843003. An example of LVEPCL termination is shown in this schematic. Additional LVPECL termination approaches are shown in the LVPECL Termination Application Note. In this example, an 18 pF parallel resonant 31.25MHz crystal is used. The C1= 27pF and C2 = 33pF are recommended for frequency accuracy. The C1 and C2 may be slightly adjusted for optimizing frequency accuracy.

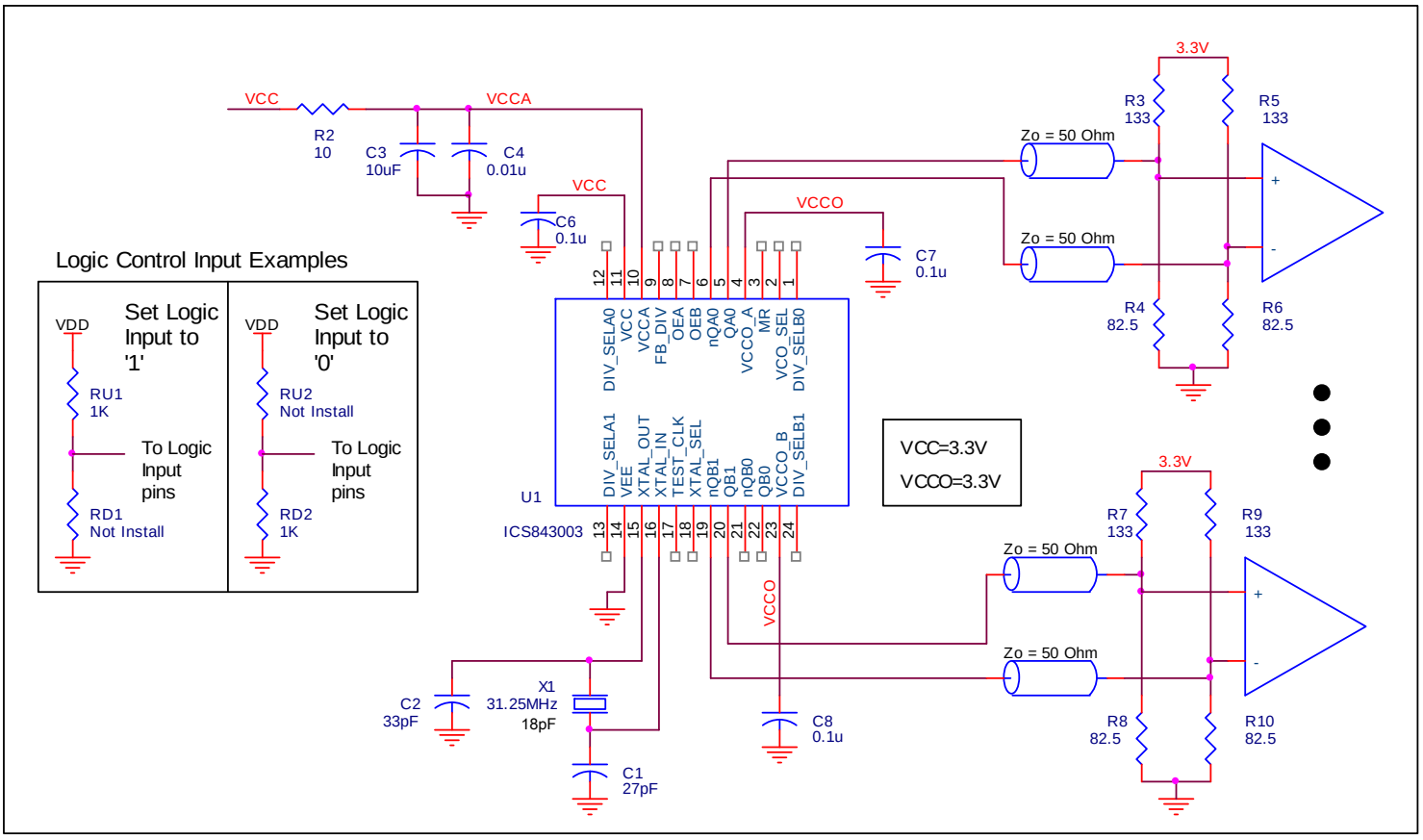


Figure 6A. 843003 Schematic Example

PC Board Layout Example

Figure 5B shows an example of 843003 P.C. board layout. The crystal X1 footprint shown in this example allows installation of either surface mount HC49S or through-hole HC49 package. The footprints of other components in this example are listed in the *Table 7.* There should be at least one decoupling capacitor per power pin. The decoupling capacitors should be located as close as possible to the power pins. The layout assumes that the board has clean analog power ground plane.

Figure 6B. 843003 PC Board Layout Example

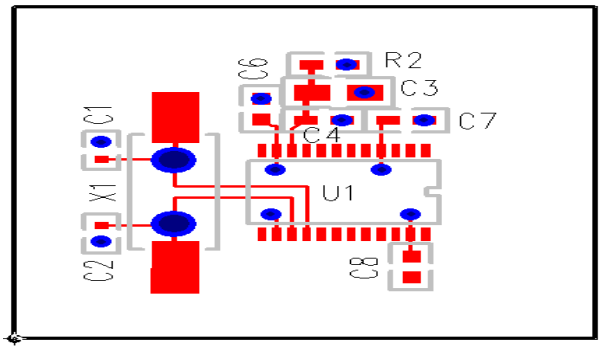


Table 7. Footprint Table

Reference	Size
C1, C2	0402
C3	0805
C4, C5, C6, C7, C8	0603
R2	0603

NOTE: Table 7, lists component sizes shown in this layout example.

Power Considerations

This section provides information on power dissipation and junction temperature for the 843003.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 843003 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 158mA = **547.5mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 3 * 30mW = **90mW**

Total Power$_{\_MAX}$ (3.3V, with all outputs switching) = 547.5mW + 90mW = **637.5mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 65°C/W per Table 8below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.638W * 65°C/W = 111.5°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 8. Thermal Resitance θ_{JA} for 24 Lead TSSOP, Forced Convection

θ_{JA} **vs. Air Flow**			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65	62

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 7.*

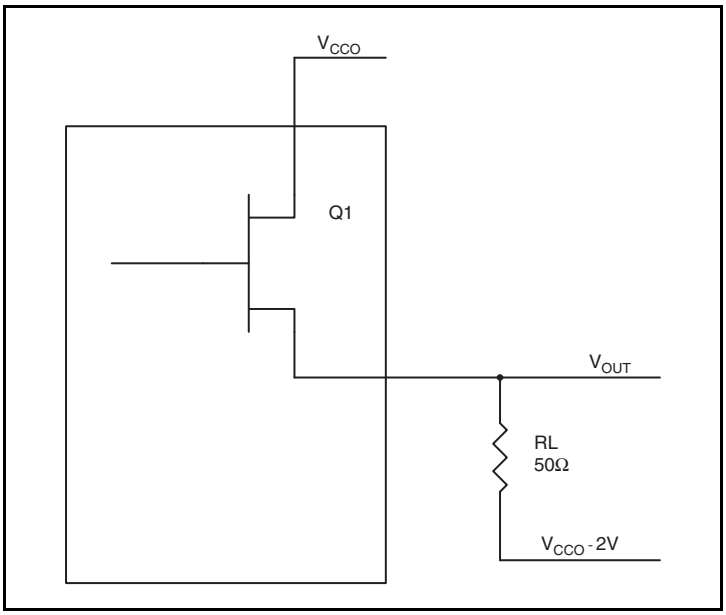


Figure 7. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 0.9V}$
  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{COO\_MAX} - 1.7V}$
  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) = [(2V – 0.9V)/50Ω] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) = [(2V – 1.7V)/50Ω] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 9. θ_{JA} vs. Air Flow Table for a 24 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65	62

Transistor Count

The transistor count for 843003 is: 3767

Package Outline and Package Dimension

Package Outline - G Suffix for 24 Lead TSSOP

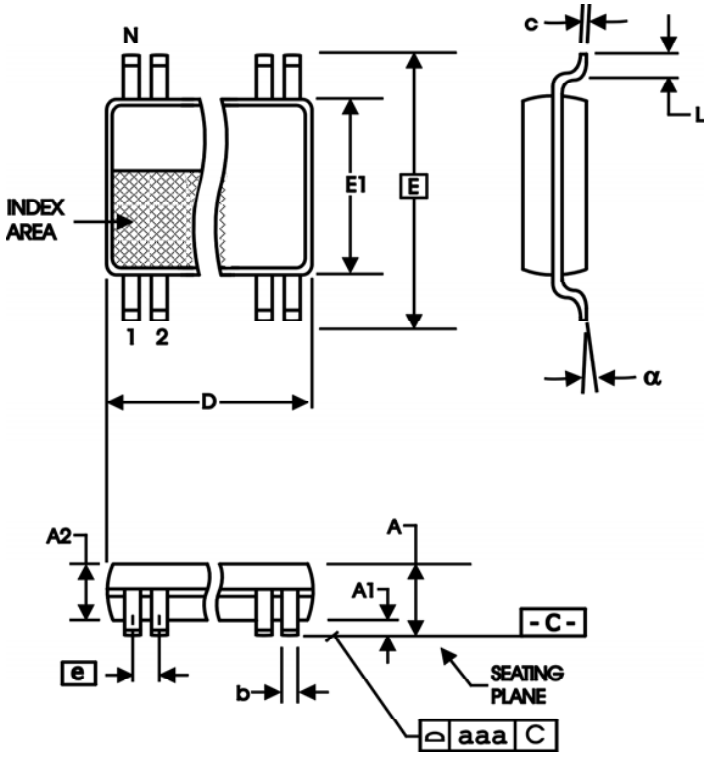


Table 10. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	24	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 11. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS843003AGLF	ICS843003AGLF	“Lead-Free” 24 Lead TSSOP	Tube	0°C to 70°C
ICS843003AGLFT	ICS843003AGLF	“Lead-Free” 24 Lead TSSOP	Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	 T10	1 11 17	Features Section - added Lead-Free bullet. Added *Recommendations for Unused Input and Output Pins.* Ordering Information table - added Lead-Free part number, marking and note.	1/25/06
A	T3B	3 14	Bank B Frequency Table - corrected table labeling. Added *LVCMOS to XTAL Interface* section. Updated datasheet format.	2/19/08
A	T11	19	Ordering Information - removed leaded devices. Updated data sheet format.	4/7/15

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