FemtoClock® Crystal-to-3.3V LVPECL Frequency Synthesizer

843003I-01

DATASHEET

General Description

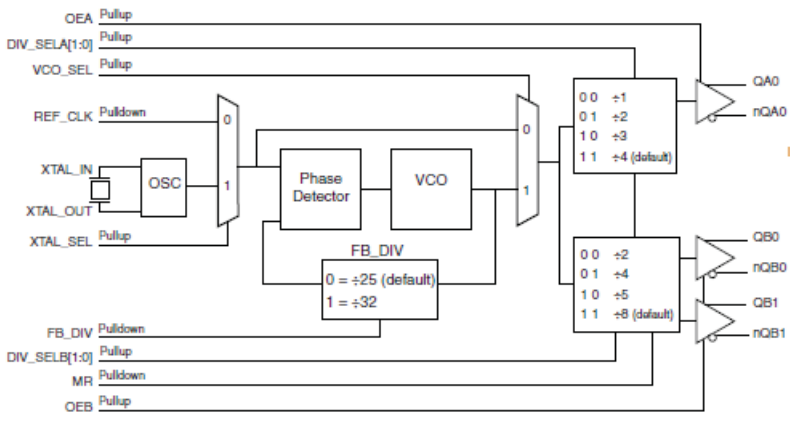
The 843003i-01 is a 3 differential output LVPECL Synthesizer designed to generate Ethernet reference clock frequencies. Using a 19.53125MHz or 25MHz, 18pF parallel resonant crystal, the following frequencies can be generated based on the settings of 4 frequency select pins (DIV_SEL[A1:A0], DIV_SEL[B1:B0]): 625MHz, 312.5MHz, 156.25MHz, and 125MHz. The 843003I-01 has 2 output banks, Bank A with 1 differential LVPECL output pair and Bank B with 2 differential LVPECL output pairs.

The two banks have their own dedicated frequency select pins and can be independently set for the frequencies mentioned above. The 843003i-01 uses ICS' 3rd generation low phase noise VCO technology and can achieve 1ps or lower typical rms phase jitter, easily meeting Ethernet jitter requirements. The 843003i-01 is packaged in a small 24-pin TSSOP package.

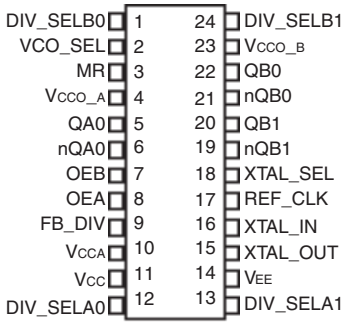
Features

- Three 3.3V LVPECL outputs on two banks, A Bank with one LVPECL pair and B Bank with two LVPECL output pairs
- Using a 19.53125MHz or 25MHz crystal, the two output banks can be independently set for 625MHz, 312.5MHz, 156.25MHz or 125MHz
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input
- VCO range: 490MHz to 680MHz
- RMS phase jitter @ 156.25MHz (1.875MHz - 20MHz): 0.53ps (typical)
- 3.3V output supply mode
- -40°C to 85°C ambient operating temperature
- Available in lead-free RoHS compliant package

Block Diagram



Pin Assignment



843003I-01
24-Lead TSSOP
4.40mm x 7.8mm x 0.92mm
package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1 24	DIV_SELB0 DIV_SELB1	Input	Pullup	Division select pin for Bank B. Default = HIGH. LVCMOS/LVTTL interface levels.
2	VCO_SEL	Input	Pullup	VCO select pin. When Low, the PLL is bypassed and the crystal reference or REF_CLK (depending on XTAL_SEL setting) are passed directly to the output dividers. Has an internal pullup resistor so the PLL is not bypassed by default. LVCMOS/LVTTL interface levels.
3	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. Has an internal pulldown resistor so the power-up default state of outputs and dividers are enabled. LVCMOS/LVTTL interface levels.
4	V_{CCO_A}	Power		Output supply pin for Bank A outputs.
5, 6	QA0, nQA0	Ouput		Differential output pair. LVPECL interface levels.
7	OEB	Input	Pullup	Output enable Bank B. Active High output enable. When logic HIGH, the 2 output pairs on Bank B are enabled. When logic LOW, the output pairs drive differential Low (QB0=Low, nQB0=High). Has an internal pullup resistor so the default power-up state of outputs are enabled. LVCMOS/LVTTL interface levels.
8	OEA	Input	Pullup	Output enable Bank A. Active High output enable. When logic HIGH, the output pair on Bank A is enabled. When logic LOW, the output pair drives differential Low (QA0=Low, nQA0=High). Has an internal pullup resistor so the default power-up state of outputs are enabled. LVCMOS/LVTTL interface levels.
9	FB_DIV	Input	Pulldown	Feedback divide select. When Low (default), the feedback divider is set for ÷25. When HIGH, the feedback divider is set for ÷32. LVCMOS/LVTTL interface levels.
10	V_{CCA}	Power		Analog supply pin.
11	V_{CC}	Power		Core supply pin.
12 13	DIV_SELA0 DIV_SELA1	Input	Pullup	Division select pin for Bank A. Default = HIGH. LVCMOS/LVTTL interface levels.
14	V_{EE}	Power		Negative supply pin.
15, 16	XTAL_OUT, XTAL_IN	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input. XTAL_IN is also the overdrive pin if you want to overdrive the crystal circuit with a single-ended reference clock.
17	REF_CLK	Input	Pulldown	Single-ended reference clock input. Has an internal pulldown resistor to pull to low state by default. Can leave floating if using the crystal interface. LVCMOS/LVTTL interface levels.
18	XTAL_SEL	Input	Pullup	Crystal select pin. Selects between the single-ended REF_CLK or crystal interface. Has an internal pullup resistor so the crystal interface is selected by default. LVCMOS/LVTTL interface levels.
19, 20	nQB1, QB1	Output		Differential output pair. LVPECL interface levels.
21, 22	nQB0, QB0	Output		Differential output pair. LVPECL interface levels.
23	V_{CCO_B}	Power		Output supply pin for Bank B outputs.

NOTE: refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Table 3A. Bank A Frequency Table

Inputs				Feedback Divider	Bank A Output Divider	M/N Multiplication Factor	QA0/nQA0 Output Frequency (MHz)
Crystal Frequency (MHz)	FB_DIV	DIV_SELA1	DIV_SELA0				
25	0	0	0	25	1	25	625
25	0	0	1	25	2	12.5	312.5
20	0	0	1	25	2	12.500	250
22.5	0	1	0	25	3	8.333	187.5
25	0	1	1	25	4	6.25	156.25
24	0	1	1	25	4	6.25	150
20	0	1	1	25	4	6.25	125
19.44	1	0	0	32	1	32	622.08
19.44	1	0	1	32	2	16	311.04
15.625	1	0	1	32	2	16	250
18.75	1	1	0	32	3	10.667	200
19.44	1	1	1	32	4	8	155.52
18.75	1	1	1	32	4	8	150
15.625	1	1	1	32	4	8	125

Table 3B. Bank B Frequency Table

Inputs				Feedback Divider	Bank B Output Divider	M/N Multiplication Factor	QBx/nQBx Output Frequency (MHz)
Crystal Frequency (MHz)	FB_DIV	DIV_SELB1	DIV_SELB0				
25	0	0	0	25	2	12.5	312.5
20	0	0	0	25	2	12.5	250
25	0	0	1	25	4	6.25	156.25
24	0	0	1	25	4	6.25	150
20	0	0	1	25	4	6.25	125
25	0	1	0	25	5	5	125
25	0	1	1	25	8	3.125	78.125
24	0	1	1	25	8	3.125	75
20	0	1	1	25	8	3.125	62.5
19.44	1	0	0	32	2	16	311.04
15.625	1	0	0	32	2	16	250
19.44	1	0	1	32	4	8	155.52
18.75	1	0	1	32	4	8	150
15.625	1	0	1	32	4	8	125
15.625	1	1	0	32	5	6.4	100
19.44	1	1	1	32	8	4	77.76
18.75	1	1	1	32	8	4	75
15.625	1	1	1	32	8	4	62.5

Table 3C. Output Bank A Configuration Select Function Table

Inputs		Outputs
DIV_SELA1	DIV_SELA0	QA
0	0	÷1
0	1	÷2
1	0	÷3
1	1	÷4

Table 3D. Output Bank B Configuration Select Function Table

Inputs		Outputs
DIV_SELB1	DIV_SELB0	QBx
0	0	÷2
0	1	÷4
1	0	÷5
1	1	÷8

Table 3E. Feedback Divider Configuration Select Function Table

Inputs	
FB_DIV	Feedback Divide
0	÷25
1	÷32

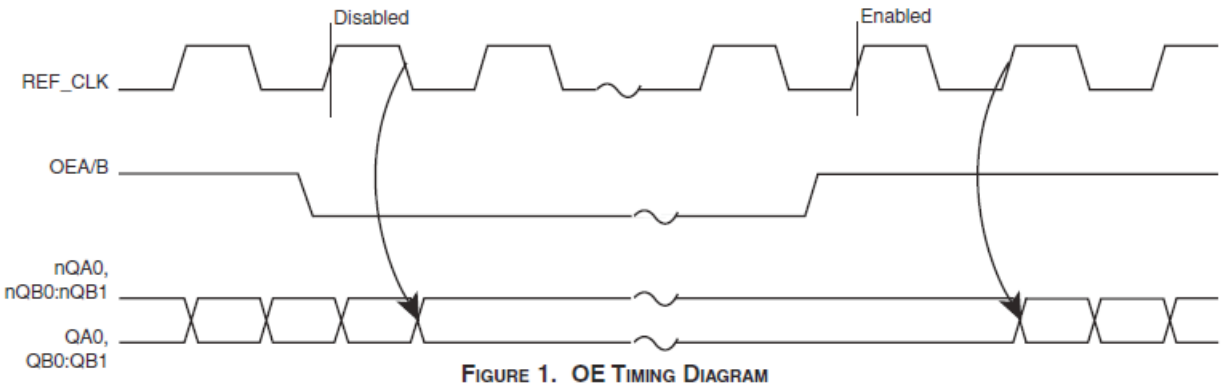


Figure 1. OE Timing Diagram

Table 3F. OEA Select Function Table

Inputs	Outputs	
OEA	QA0	nQA0
0	LOW	HIGH
1	Active	Active

Table 3G. OEB Select Function Table

Inputs	Outputs	
OEB	QB0:QB1	nQB0:nQB1
0	LOW	HIGH
1	Active	Active

Absolute Maximum Ratings

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	70°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO\_A} = V_{CCO\_B}$ = 3.3V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.20	3.3	V_{CC}	V
$V_{CCO\_A, B}$	Output Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				150	mA
I_{CCA}	Analog Supply Current				20	mA

Table 4B. LVCMOS / LVTTL DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO\_A} = V_{CCO\_B}$ = 3.3V±5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	REF_CLK, MR, FB_DIV	$V_{CC} = V_{IN}$ = 3.465V			150	µA
		DIV_SELA0, DIV_SELA1, DIV_SELB0, DIV_SELB1, VCO_SEL, XTAL_SEL, OEA, OEB	$V_{CC} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	REF_CLK, MR, FB_DIV	V_{CC} = 3.465V, V_{IN} = 0V	-5			µA
		DIV_SELA0, DIV_SELA1, DIV_SELB0, DIV_SELB1, VCO_SEL, XTAL_SEL, OEA, OEB	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA

Table 4C. LVPECL DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO\_A} = V_{CCO\_B}$ = 3.3V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V - 1.4		V- 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V - 2.0		V - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50 to V - 2V.

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter		Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental			
Frequency	FB_DIV = ÷25		19.6		27.2	MHz
	FB_DIV = ÷32		15.313		21.25	MHz
Equivalent Series Resistance (ESR)					50	Ω
Shunt Capacitance					7	pF
Drive Level					1	mW

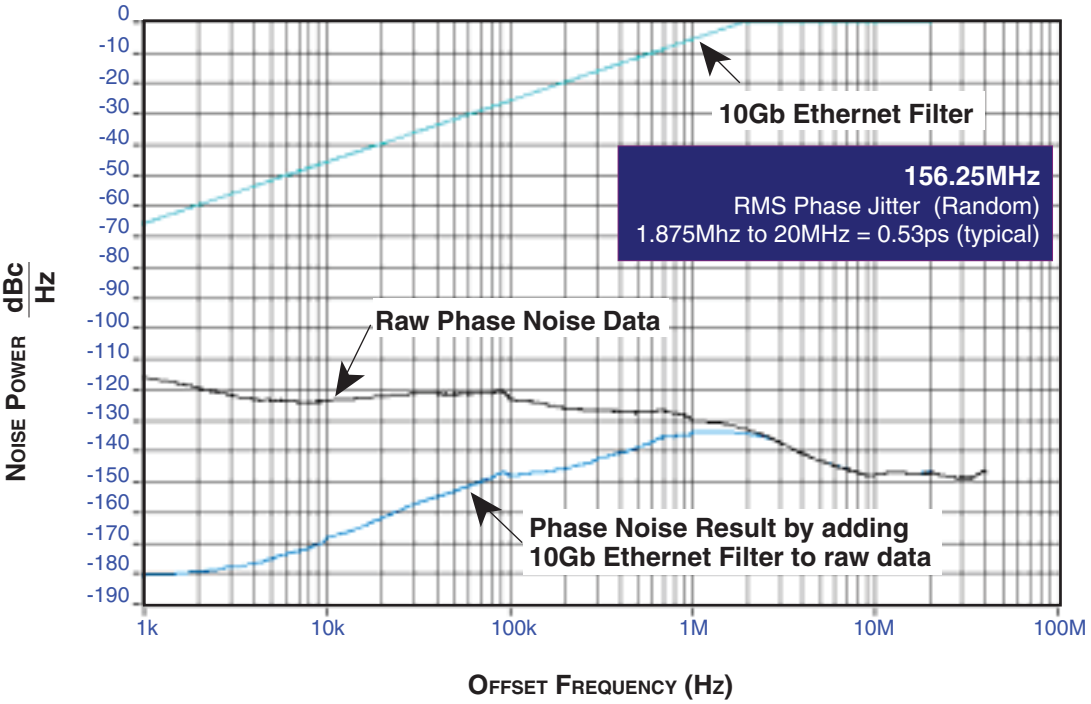
NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 6. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO\_A} = V_{CCO\_B}$ = 3.3V±5%, T_A = -40°C TO 85°C

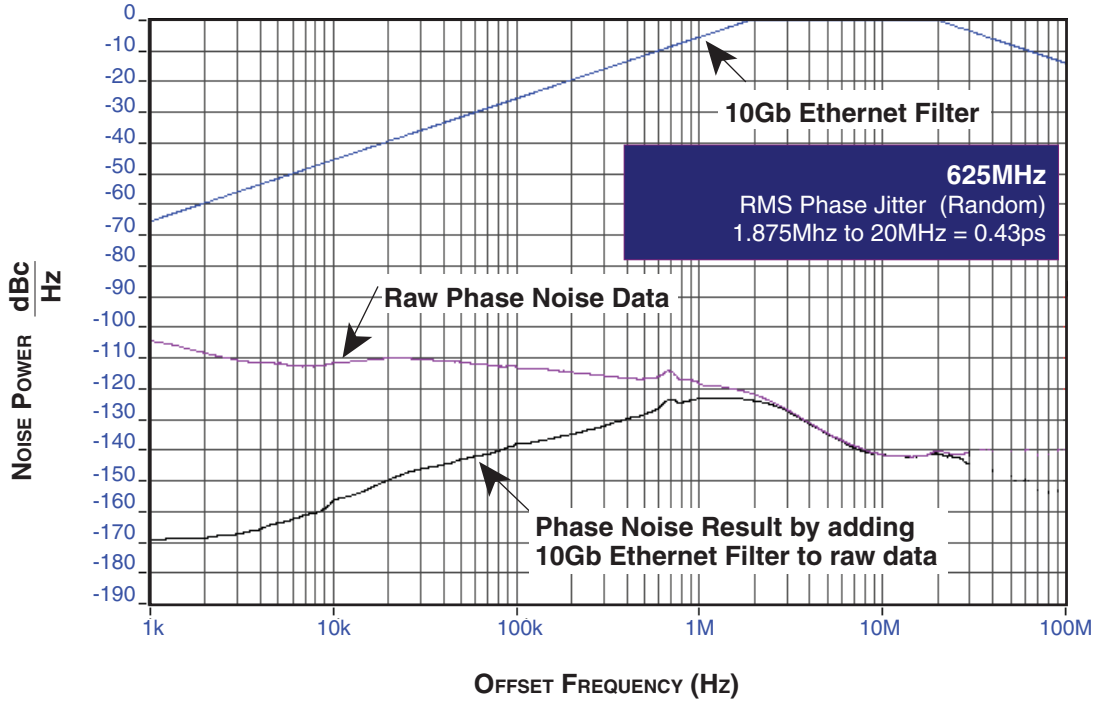
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency Range	Output Divider = ÷1	490		680	MHz
		Output Divider = ÷2	245		340	MHz
		Output Divider = ÷3	163.33		226.67	MHz
		Output Divider = ÷4	122.5		170	MHz
		Output Divider = ÷5	98		136	MHz
		Output Divider = ÷8	61.25		85	MHz
tsk(b)	Bank Skew, NOTE 1				50	ps
tsk(o)	Output Skew; NOTE 2, 4	Outputs @ Same Frequency			125	ps
		Outputs @ Different Frequencies			225	ps
tjit(Ø)	RMS Phase Jitter (Random); NOTE 3	625MHz (1.875MHz - 20MHz)		0.43		ps
		312.5MHz (1.875MHz - 20MHz)		0.51		ps
		156.25MHz (1.875MHz - 20MHz)		0.53		ps
		125MHz (1.875MHz - 20MHz)		0.48		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		600	ps
odc	Output Duty Cycle	Output Divider = ÷1	40		60	%
		Output Divider [1] ÷1	45		55	%

NOTE 1: Defined as skew winthin a bank of outputs at the same voltages and with equal load conditions.
NOTE 2: Defined as skew between outputs at the same supply voltages and with equal load conditions.
Measured at the output differential cross points.
NOTE 3: Please refer to the Phase Noise Plots.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

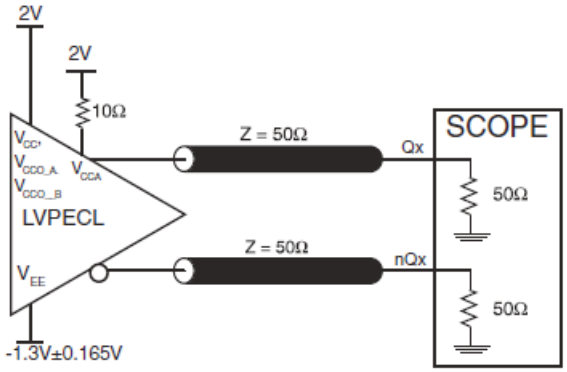
Typical Phase Noise at 156.25MHz



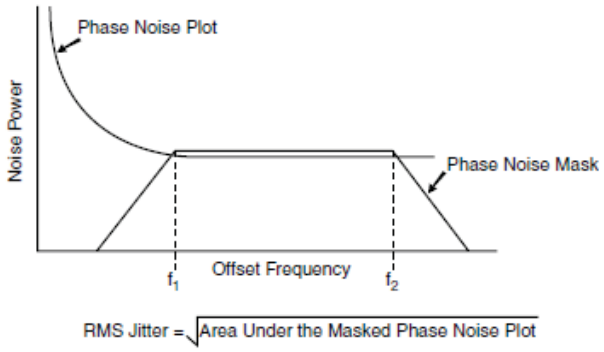
Typical Phase Noise at 625MHz



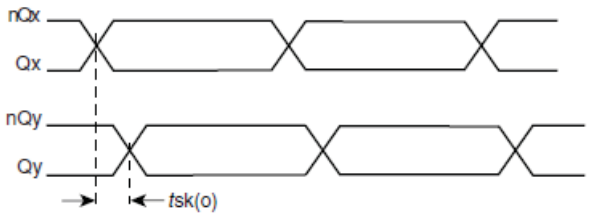
PARAMETER MEASUREMENT INFORMATION



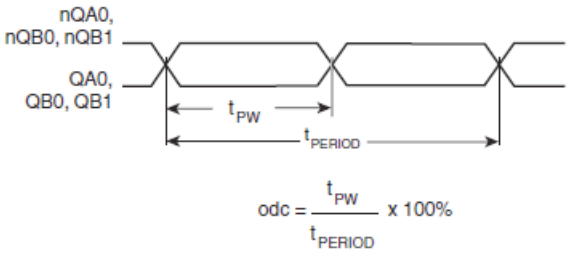
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



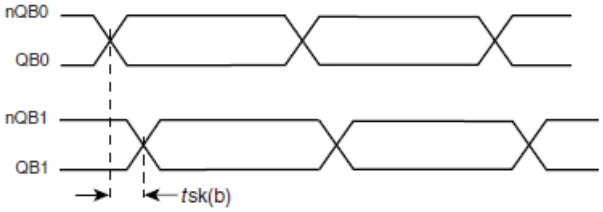
RMS PHASE JITTER



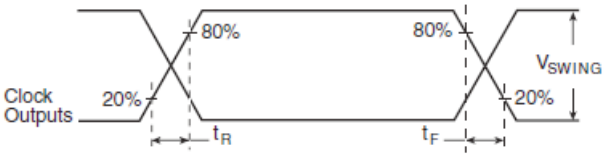
OUTPUT SKEW



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



BANK SKEW



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS843003I-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA}, and V_{CCOx} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 2* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{CCA} pin.

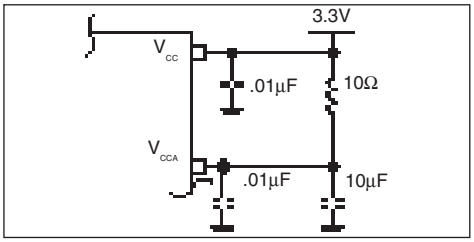


FIGURE 2. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS843003I-01 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 3* below were determined using a 19.53125MHz or 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

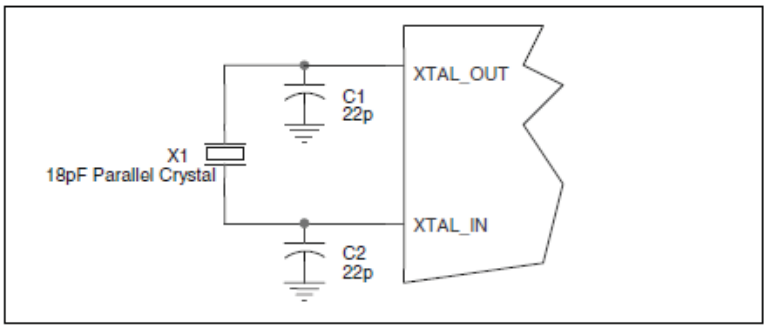


Figure 3. CRYSTAL INPUT INTERFACE

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Input:

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

REF_CLK Input:

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK to ground.

LVCMOS Control Pins:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Output

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Termination for 3.3V LVPECL Output

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

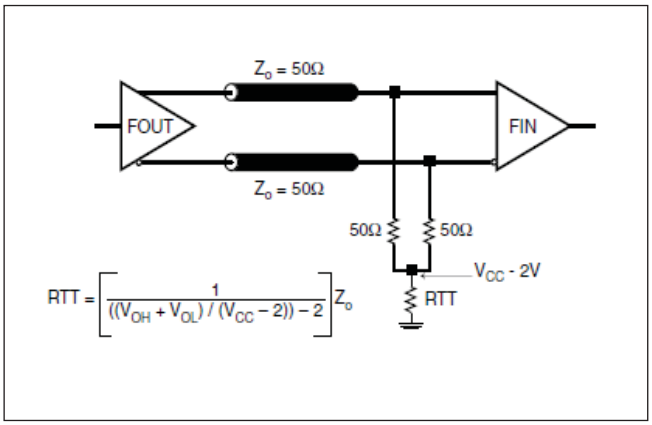


Figure 4A. LVPECL Output Termination

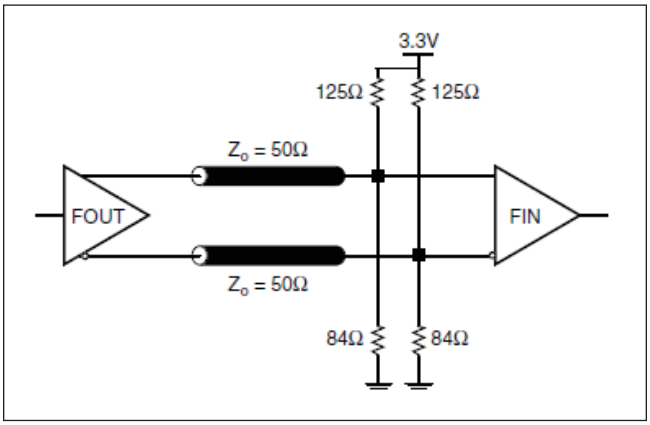


Figure 4B. LVPECL Output Termination

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS843003I-01. Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS843003I-01 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 150mA = **519.75mW**
- Power (outputs)$_{MAX}$ = **30.2mW/Loaded Output pair**
  If all outputs are loaded, the total power is 3 * 30.2mW = **90.6mW**

Total Power$_{_MAX}$ (3.465V, with all outputs switching) = 519.75mW + 90.6mW = **610.35mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 65°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.610W * 65°C/W = 124.6°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 7. THERMAL RESISTANCE θ_{JA} FOR 24-PIN TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 5.*

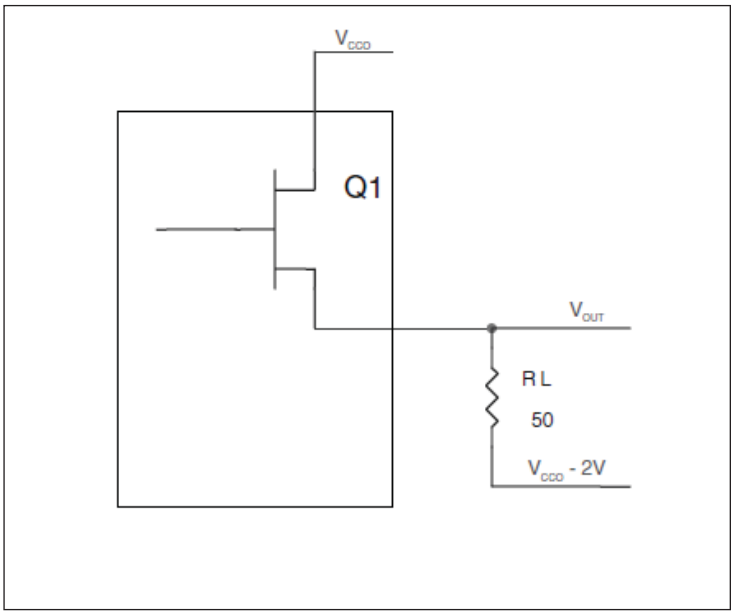


FIGURE 5. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} – 1.0V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{1.0V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} – 1.7V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) =$
$[(2V - 1V)/50\Omega] * 1V =$ **20.0mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30.2mW**

RELIABILITY INFORMATION

TABLE 8. θ_{JA} VS. AIR FLOW TABLE FOR 24 LEAD TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

TRANSISTOR COUNT

The transistor count for 843003I-01 is: 3822

Package Outline - G Suffix for 24 Lead TSSOP

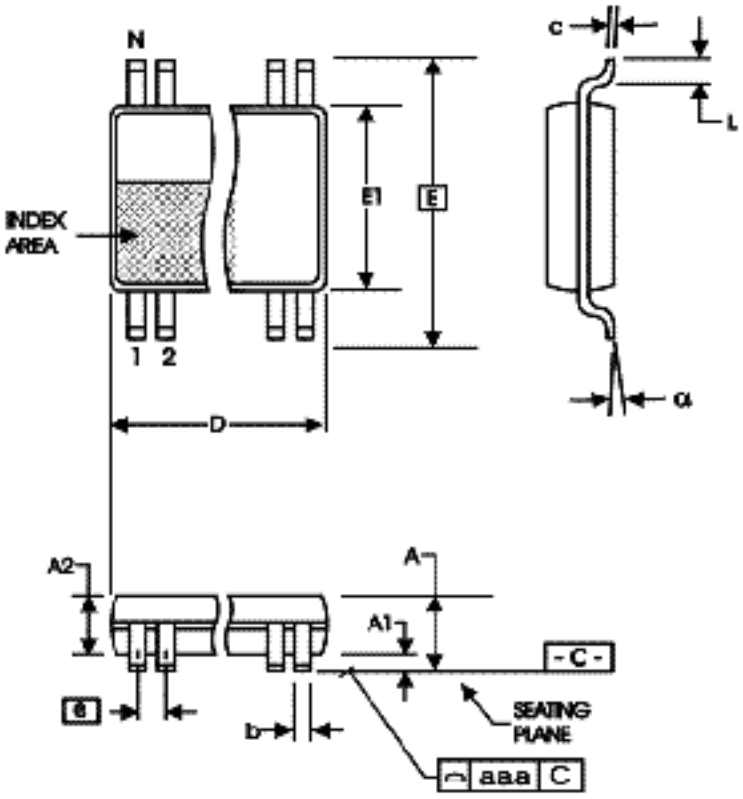


Table 9. Package Dimensions

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS843003AGI-01LF	ICS43003AI01L	24 Lead “Lead-Free” TSSOP	tube	-40°C to 85°C
ICS843003AGI-01LFT	ICS43003AI01L	24 Lead “Lead-Free” TSSOP	tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T10	15	Removed leaded devices - last time buy expired October 28, 2014. PDN CQ-13-02 Updated datasheet format.	12/8/14

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