

## General Description

The 843004I is a 4 output LVPECL synthesizer optimized to generate Fibre Channel reference clock frequencies. Using a 26.5625MHz 18pF parallel resonant crystal, the following frequencies can be generated based on the two frequency select pins (F\_SEL[1:0]): 212.5MHz, 187.5MHz, 159.375MHz, 156.25MHz, 106.25MHz, and 53.125MHz. The 843004I uses IDT's 3<sup>rd</sup> generation low phase noise VCO technology and can achieve 1ps or lower typical rms phase jitter, easily meeting Fibre Channel jitter requirements. The 843004I is packaged in a small 24-pin TSSOP package.

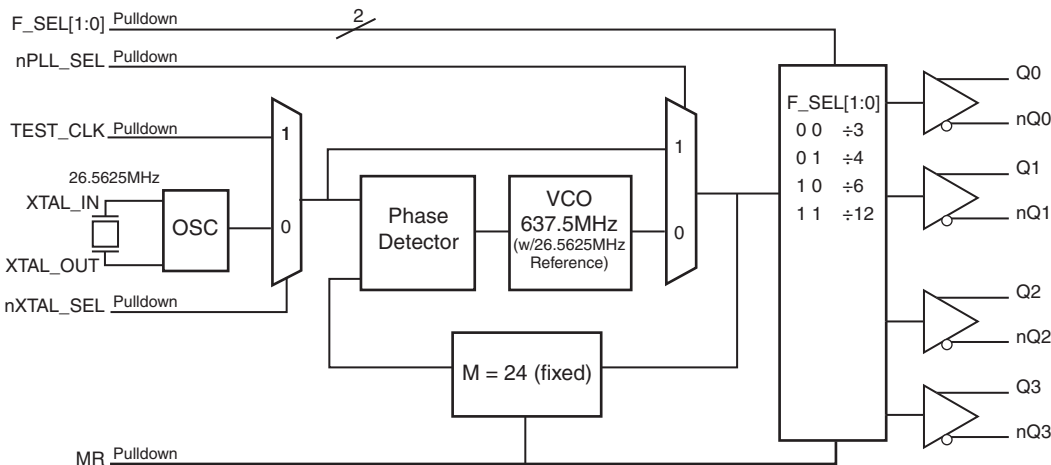
## Features

- Four 3.3V differential LVPECL output pairs
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended clock input
- Supports the following output frequencies: 212.5MHz, 187.5MHz, 159.375MHz, 156.25MHz, 106.25MHz, 53.125MHz
- VCO range: 560MHz – 680MHz
- Output skew: 50ps (maximum)
- RMS phase jitter @ 212.5MHz, using a 26.5625MHz crystal (2.55MHz – 20MHz): 0.47ps (typical)
- Full 3.3V or 2.5V supply modes
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

## Bank A Frequency Table

Inputs				N Div. Value	M/N Div. Value	Output Frequency (MHz)
Input Frequency (MHz)	F_SEL1	F_SEL0	M Div. Value			
26.5625	0	0	24	3	8	212.5
26.5625	0	1	24	4	6	159.375
26.5625	1	0	24	6	4	106.25
26.5625	1	1	24	12	2	53.125
26.04166	0	1	24	4	6	156.25
23.4375	0	0	24	3	8	187.5

## Block Diagram



## Pin Assignment

nQ1	1	24	nQ2
Q1	2	23	Q2
V <sub>CC0</sub>	3	22	V <sub>CC0</sub>
Q0	4	21	Q3
nQ0	5	20	nQ3
MR	6	19	VEE
nPLL_SEL	7	18	nc
nc	8	17	nXTAL_SEL
V <sub>CCA</sub>	9	16	TEST_CLK
F_SEL0	10	15	VEE
V <sub>CC</sub>	11	14	XTAL_IN
F_SEL1	12	13	XTAL_OUT

**843004I**

**24-Lead TSSOP**  
4.4mm x 7.8mm x 0.925mm  
package body  
G Package  
Top View

**Table 1. Pin Descriptions**

Number	Name	Type		Description
1, 2	nQ1, Q1	Output		Differential output pair. LVPECL interface levels.
3, 22	V <sub>CC0</sub>	Power		Output supply pins.
4, 5	Q0, nQ0	Output		Differential output pair. LVPECL interface levels.
6	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
7	nPLL_SEL	Input	Pulldown	Selects between the PLL and TEST_CLK as input to the dividers. When LOW, selects PLL (PLL Enable). When HIGH, deselects the reference clock (PLL Bypass). LVCMOS/LVTTL interface levels.
8, 18	nc	Unused		No connect.
9	V <sub>CCA</sub>	Power		Analog supply pin.
10, 12	F_SEL0, F_SEL1	Input	Pulldown	Frequency select pins. LVCMOS/LVTTL interface levels.
11	V <sub>CC</sub>	Power		Core supply pin.
13, 14	XTAL_OUT, XTAL_IN	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.
15, 19	V <sub>EE</sub>	Power		Negative supply pins.
16	TEST_CLK	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
17	nXTAL_SEL	Input	Pulldown	Selects between the single-ended TEST_CLK or crystal interface as the PLL reference source. When HIGH, selects TEST_CLK. When LOW, selects XTAL. LVCMOS/LVTTL interface levels.
20, 21	nQ3, Q3	Output		Differential output pair. LVPECL interface levels.
23, 24	Q2, nQ2	Output		Differential output pair. LVPECL interface levels.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{CC}$	4.6V
Inputs, $V_I$ XTAL_IN Other Inputs	0V to $V_{CC}$ -0.5V to $V_{CC} + 0.5V$
Outputs, $I_O$ (LVPECL) Continuous Current Surge Current	50mA 100mA
Package Thermal Impedance, $\theta_{JA}$	70°C/W (0 mps)
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

**Table 3A. Power Supply DC Characteristics,  $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{CCA}$	Analog Supply Voltage		3.135	3.3	3.465	V
$V_{CCO}$	Output Supply Voltage		3.135	3.3	3.465	V
$I_{EE}$	Power Supply Current				130	mA
$I_{CCA}$	Analog Supply Current	Included in $I_{EE}$			15	mA

**Table 3B. Power Supply DC Characteristics,  $V_{CC} = V_{CCA} = V_{CCO} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Core Supply Voltage		2.375	2.5	2.625	V
$V_{CCA}$	Analog Supply Voltage		2.375	2.5	2.625	V
$V_{CCO}$	Output Supply Voltage		2.375	2.5	2.625	V
$I_{EE}$	Power Supply Current				120	mA
$I_{CCA}$	Analog Supply Current	Included in $I_{EE}$			12	mA

**Table 3C. LVCMOS/LVTTL DC Characteristics,  $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	$V_{CC} = 3.3V$	2		$V_{CC} + 0.3$	V
		$V_{CC} = 2.5V$	1.7		$V_{CC} + 0.3$	V
$V_{IL}$	Input Low Voltage	$V_{CC} = 3.3V$	-0.3		0.8	V
		$V_{CC} = 2.5V$	-0.3		0.7	V
$I_{IH}$	Input High Current	TEST_CLK, MR, F_SEL[0:1], nPLL_SEL, nXTAL_SEL $V_{CC} = V_{IN} = 3.465V$ or $2.625V$			150	$\mu A$
$I_{IL}$	Input Low Current	TEST_CLK, MR, F_SEL[0:1], nPLL_SEL, nXTAL_SEL $V_{CC} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	-5			$\mu A$

**Table 3D. LVPECL DC Characteristics,  $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Current; NOTE 1		$V_{CCO} - 1.4$		$V_{CCO} - 0.9$	$\mu A$
$V_{OL}$	Output Low Current; NOTE 1		$V_{CCO} - 2.0$		$V_{CCO} - 1.7$	$\mu A$
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs termination with  $50\Omega$  to  $V_{CCO} - 2V$ .

**Table 4. Crystal Characteristics**

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		23.33	26.5625	28.33	MHz
Equivalent Series Resistance (ESR)				50	$\Omega$
Shunt Capacitance				7	pF

NOTE: Characterized using an 18pF parallel resonant crystal.

## AC Electrical Characteristics

**Table 5A. AC Characteristics,  $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency Range	$F\_SEL[1:0] = 00$	186.67		226.66	MHz
		$F\_SEL[1:0] = 01$	140		170	MHz
		$F\_SEL[1:0] = 10$	93.33		113.33	MHz
		$F\_SEL[1:0] = 11$	46.67		56.66	MHz
$t_{sk(o)}$	Output Skew; NOTE 1, 2				50	ps
$f_{jit}(\emptyset)$	RMS Phase Jitter, (Random); NOTE 3	212.5MHz, (2.55MHz – 20MHz)		0.47		ps
		159.375MHz, (1.875MHz – 20MHz)		0.52		ps
		156.25MHz, (1.875MHz – 20MHz)		0.52		ps
		106.25MHz, (637kHz – 5MHz)		0.62		ps
		53.125MHz, (637kHz – 50MHz)		0.67		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	300		600	ps
odc	Output Duty Cycle	$F\_SEL[1:0] \neq 00$	49		51	%
		$F\_SEL[1:0] = 00$	42		58	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Please refer to the Phase Noise Plots.

**Table 5B. AC Characteristics,  $V_{CC} = V_{CCA} = V_{CCO} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

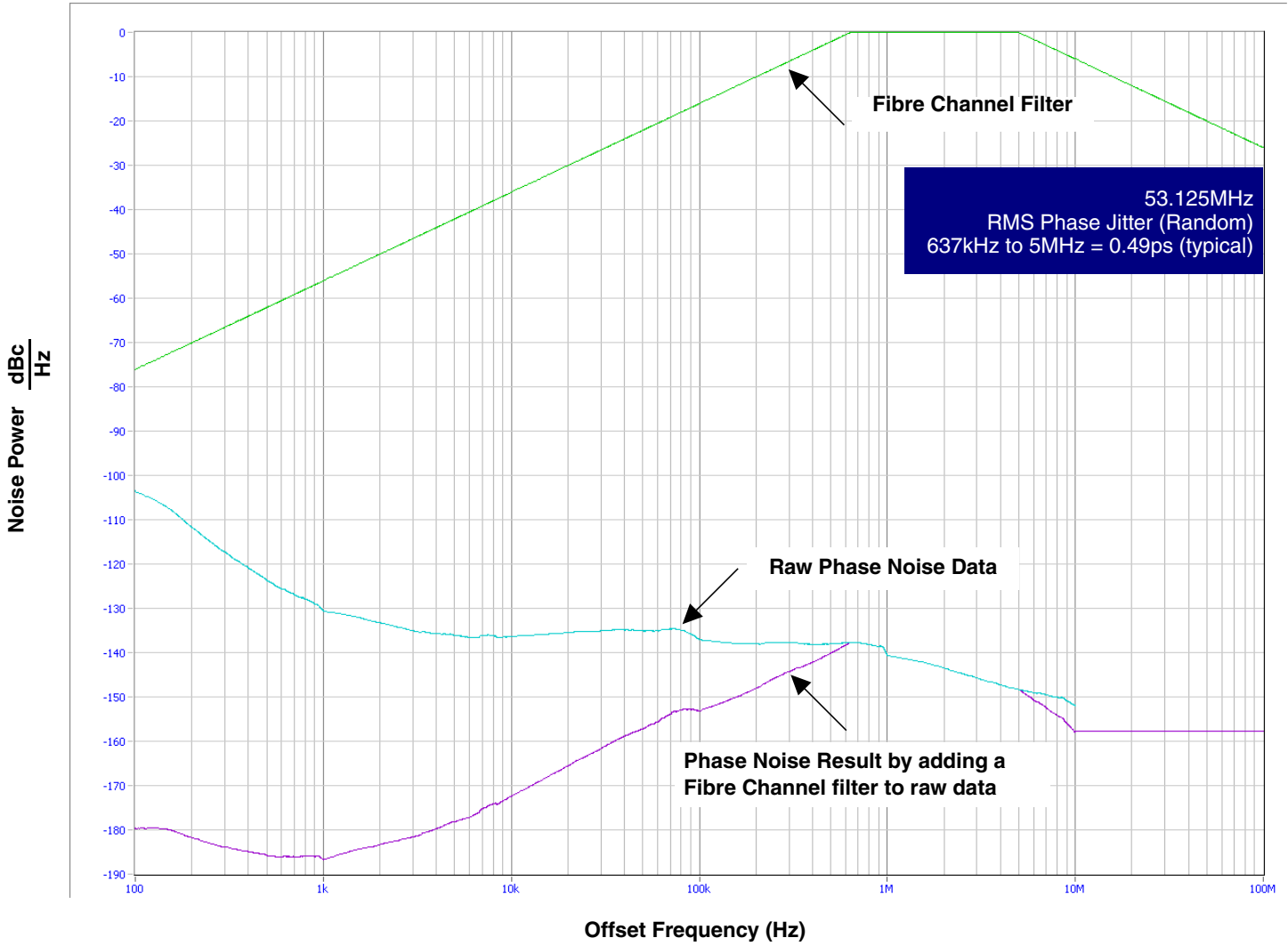
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency Range	$F\_SEL[1:0] = 00$	186.67		226.66	MHz
		$F\_SEL[1:0] = 01$	140		170	MHz
		$F\_SEL[1:0] = 10$	93.33		113.33	MHz
		$F\_SEL[1:0] = 11$	46.67		56.66	MHz
$t_{sk(o)}$	Output Skew; NOTE 1, 2				50	ps
$f_{jit}(\emptyset)$	RMS Phase Jitter, (Random)	212.5MHz, (2.55MHz – 20MHz)		0.49		ps
		159.375MHz, (1.875MHz – 20MHz)		0.52		ps
		156.25MHz, (1.875MHz – 20MHz)		0.52		ps
		106.25MHz, (637kHz – 5MHz)		0.65		ps
		53.125MHz, (637kHz – 50MHz)		0.71		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	300		600	ps
odc	Output Duty Cycle	$F\_SEL[1:0] \neq 00$	48		52	%
		$F\_SEL[1:0] = 00$	42		58	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

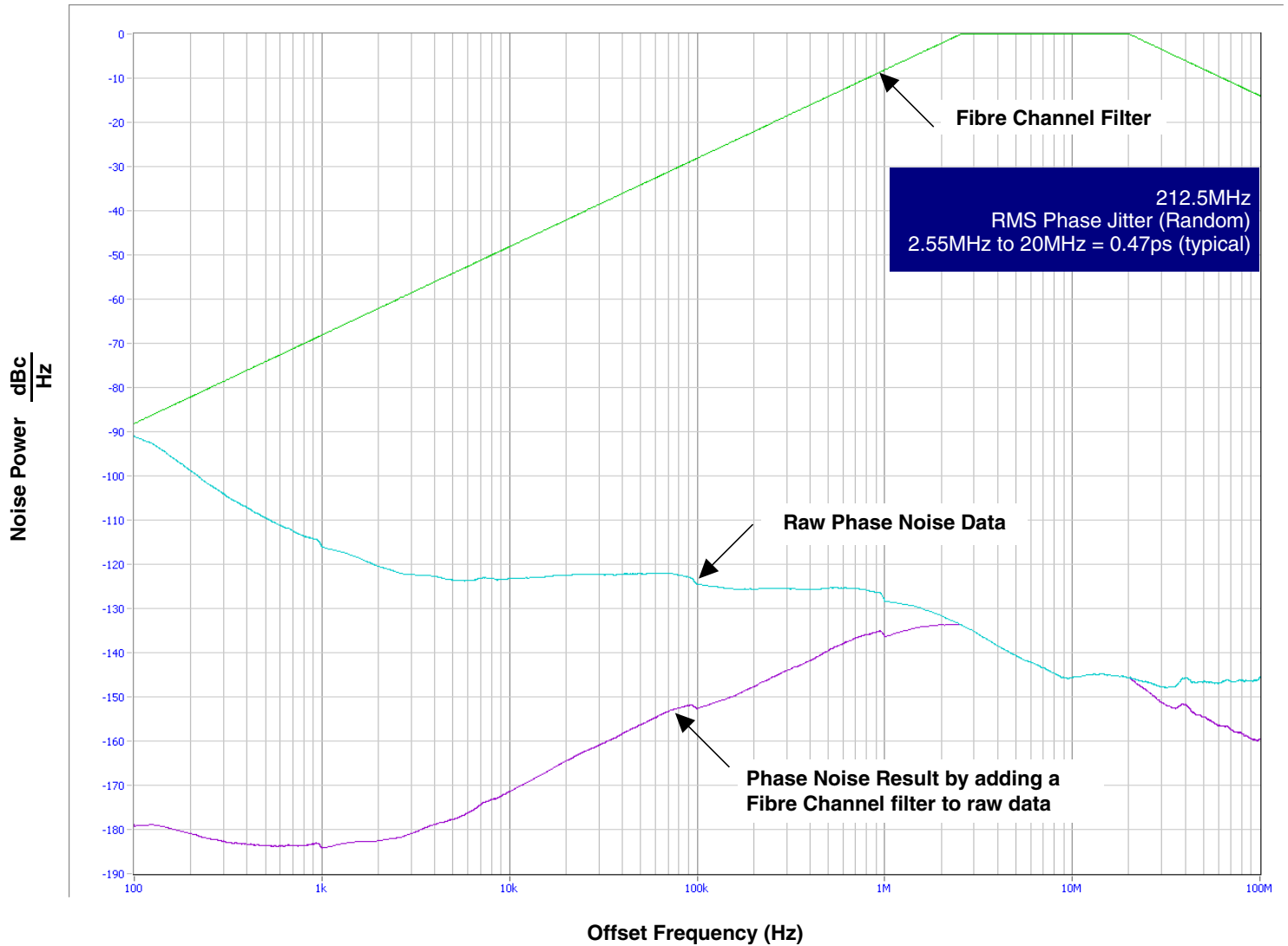
NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

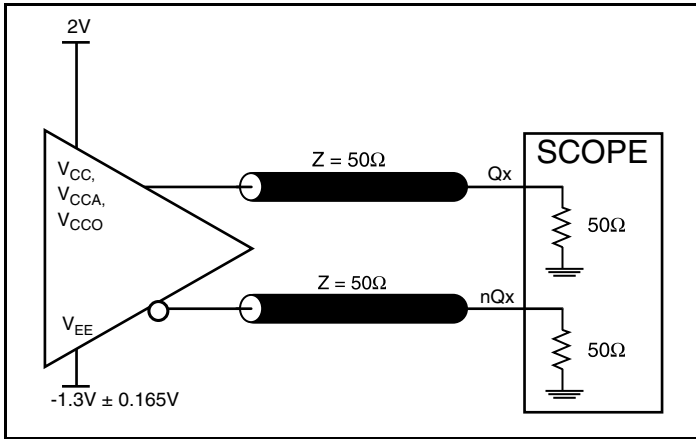
Typical Phase Noise at 53.125MHz at 3.3V



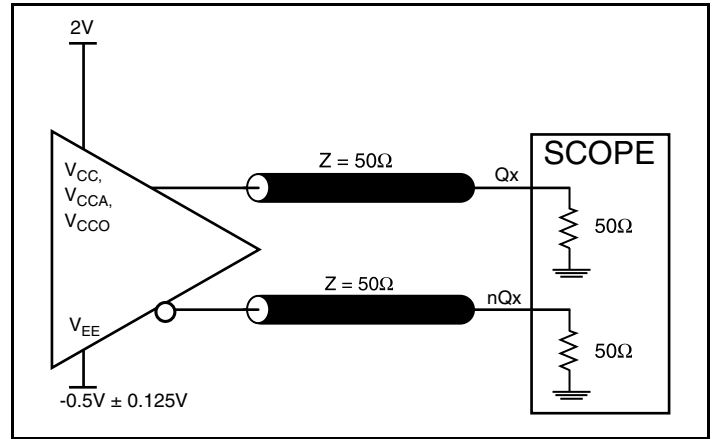
Typical Phase Noise at 212.5MHz at 3.3V



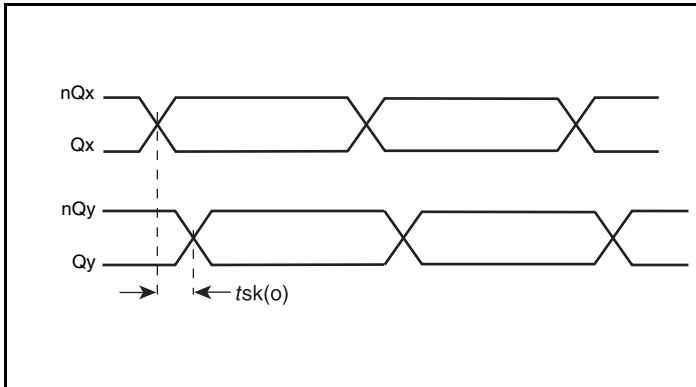
## Parameter Measurement Information



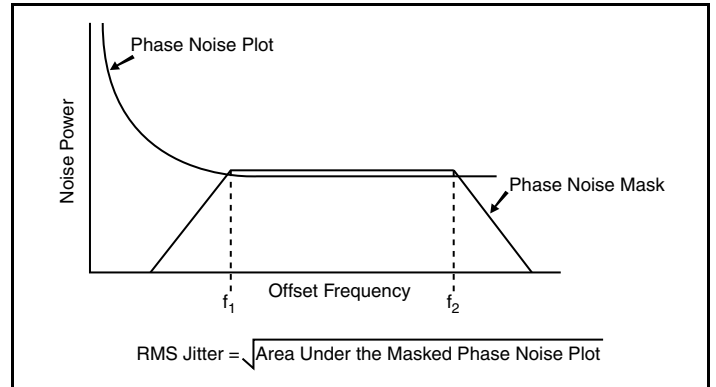
3.3V Core/ 3.3V Output Load AC Test Circuit



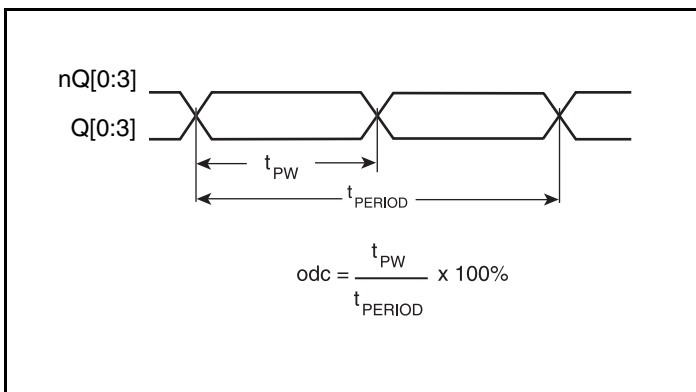
2.5V Core/ 2.5V Output Load AC Test Circuit



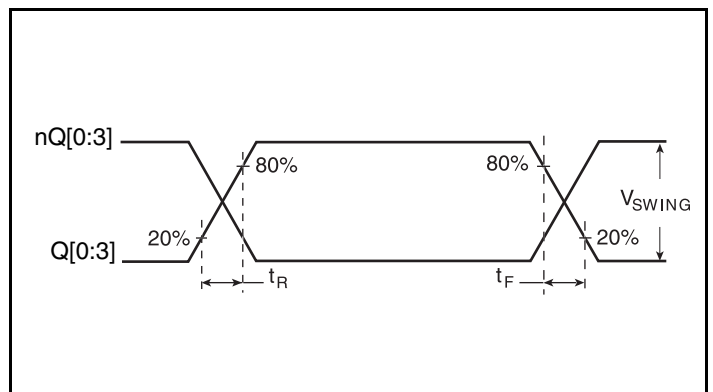
Output Skew



RMS Phase Jitter



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time



## Application Information

### Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 843004I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{CC}$ ,  $V_{CCA}$  and  $V_{CCO}$  should be individually connected to the power supply plane through vias, and  $0.01\mu\text{F}$  bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic  $V_{CC}$  pin and also shows that  $V_{CCA}$  requires that an additional  $10\Omega$  resistor along with a  $10\mu\text{F}$  bypass capacitor be connected to the  $V_{CCA}$  pin.

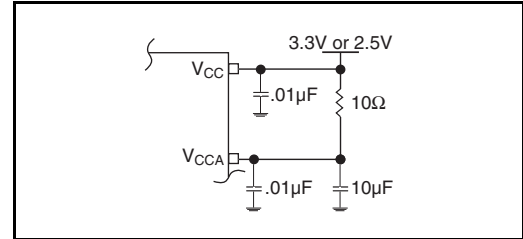


Figure 1. Power Supply Filtering

### Recommendations for Unused Input and Output Pins

#### Inputs:

##### Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL\_IN and XTAL\_OUT can be left floating. Though not required, but for additional protection, a  $1\text{k}\Omega$  resistor can be tied from XTAL\_IN to ground.

##### TEST\_CLK Input

For applications not requiring the use of the clock, it can be left floating. Though not required, but for additional protection, a  $1\text{k}\Omega$  resistor can be tied from the TEST\_CLK to ground.

##### LVC MOS Control Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A  $1\text{k}\Omega$  resistor can be used.

#### Outputs:

##### LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

## Crystal Input Interface

The 843004I has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 26.5625MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

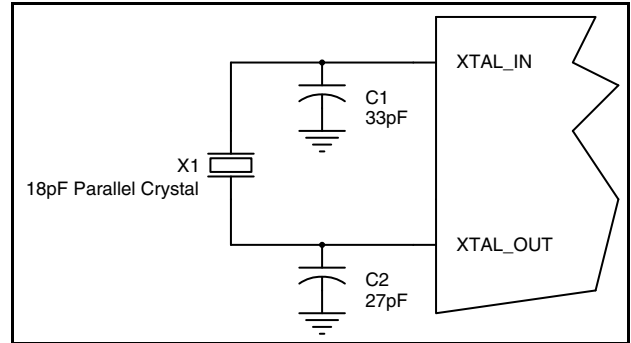


Figure 2. Crystal Input Interface

## Overdriving the XTAL Interface

The XTAL\_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3A*. The XTAL\_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver ( $R_o$ ) plus the series resistance ( $R_s$ ) equals the transmission line impedance. In addition,

matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First,  $R_1$  and  $R_2$  in parallel should equal the transmission line impedance. For most 50Ω applications,  $R_1$  and  $R_2$  can be 100Ω. This can also be accomplished by removing  $R_1$  and making  $R_2$  50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

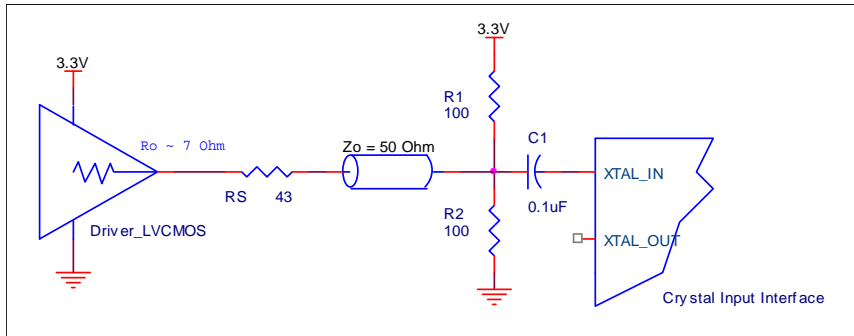


Figure 3A. General Diagram for LVCMOS Driver to XTAL Input Interface

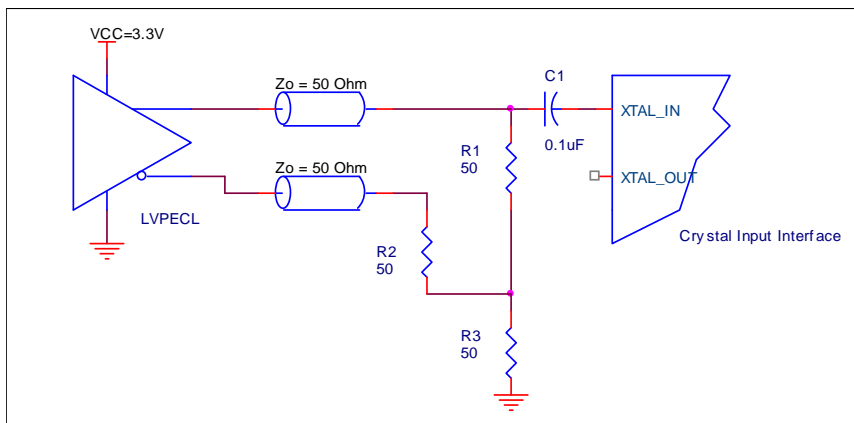


Figure 3B. General Diagram for LVPECL Driver to XTAL Input Interface

### Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion.

Figures 4A and 4B show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

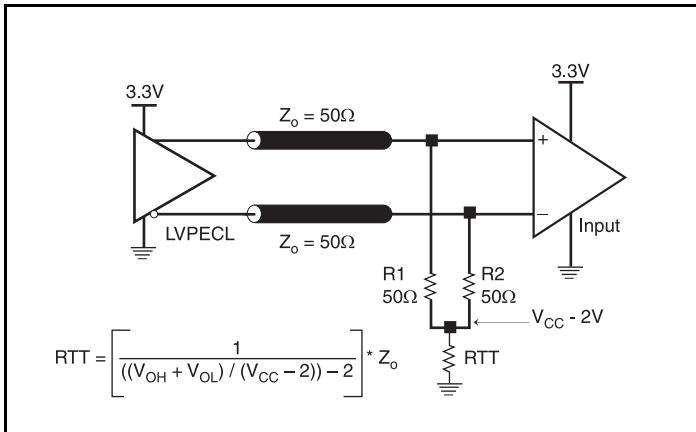


Figure 4A. 3.3V LVPECL Output Termination

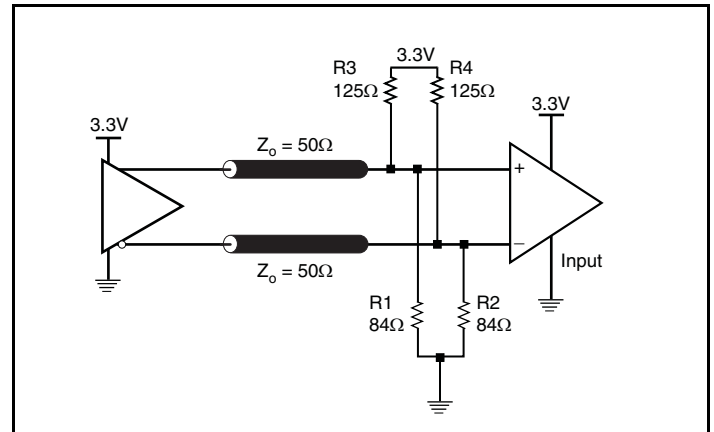


Figure 4B. 3.3V LVPECL Output Termination

## Termination for 2.5V LVPECL Outputs

Figure 5A and Figure 5B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating  $50\Omega$  to  $V_{CC} - 2V$ . For  $V_{CC0} = 2.5V$ , the  $V_{CC0} - 2V$  is very close to ground

level. The R3 in Figure 5B can be eliminated and the termination is shown in Figure 5C.

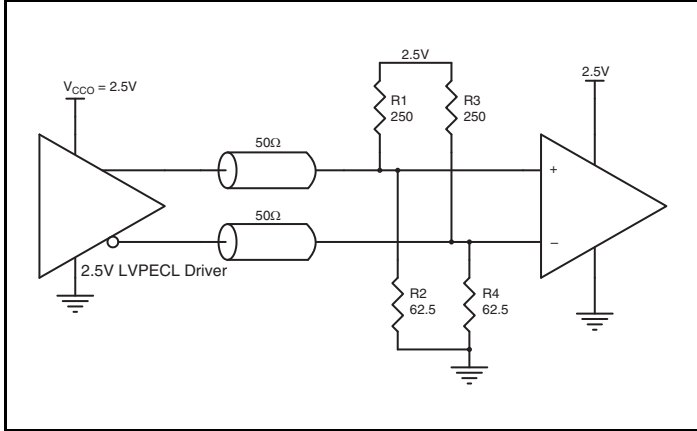


Figure 5A. 2.5V LVPECL Driver Termination Example

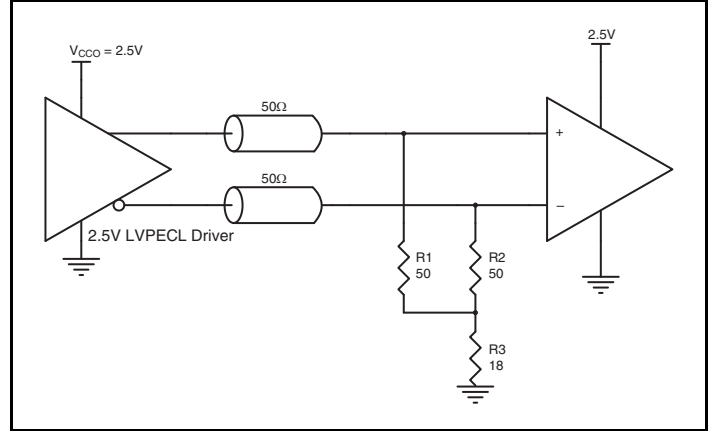


Figure 5B. 2.5V LVPECL Driver Termination Example

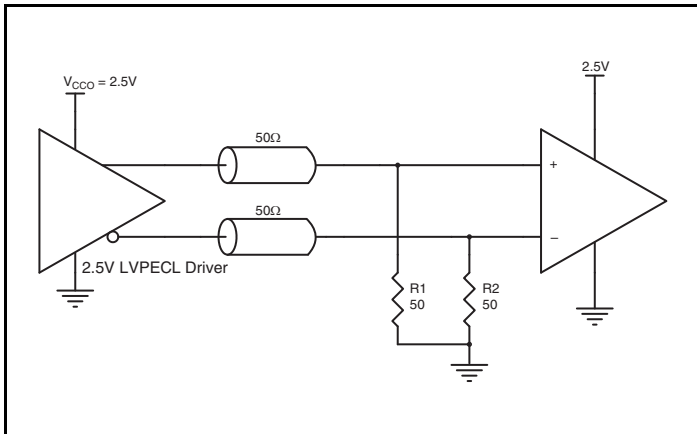


Figure 5C. 2.5V LVPECL Driver Termination Example

## Layout Guideline

Figure 6 shows a schematic example of the 843004I. An example of LVEPCL termination is shown in this schematic. Additional LVPECL termination approaches are shown in the LVPECL Termination Application Note. In this example, an 18pF parallel resonant

26.5625MHz crystal is used. The C1 = 27pF and C2 = 33pF are recommended for frequency accuracy. For different board layout, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy.

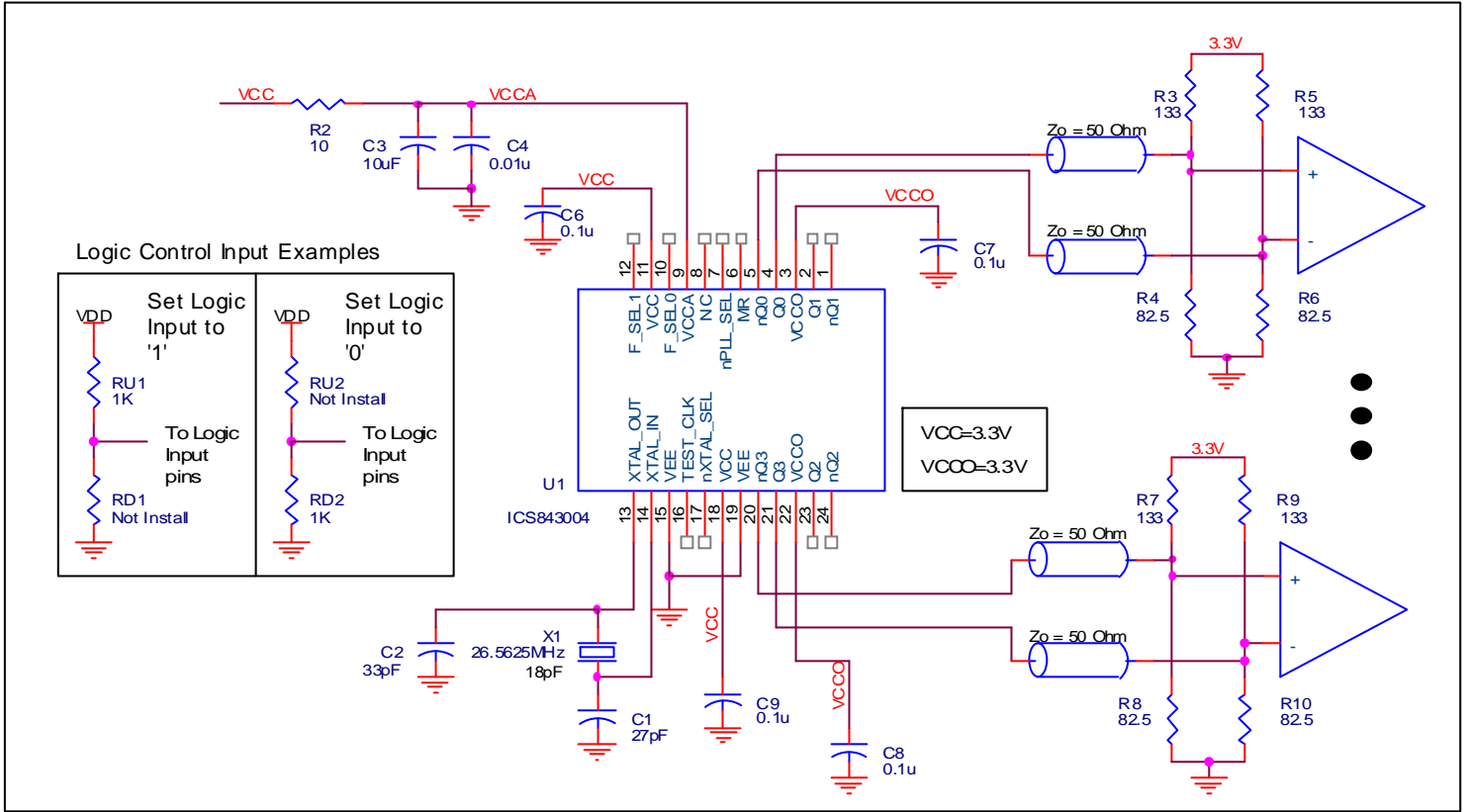


Figure 6. 843004I Schematic Example

## Power Considerations

This section provides information on power dissipation and junction temperature for the 843004I. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 843004I is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.465V * 130mA = 450.45mW$
- Power (outputs)<sub>MAX</sub> = **30mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $4 * 30mW = 120mW$

**Total Power<sub>MAX</sub>** (3.465V, with all outputs switching) =  $450.45mW + 120mW = 570.45mW$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 65°C/W per Table 6 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ C + 0.571W * 65^\circ C/W = 122.1^\circ C. \text{ This is below the limit of } 125^\circ C.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

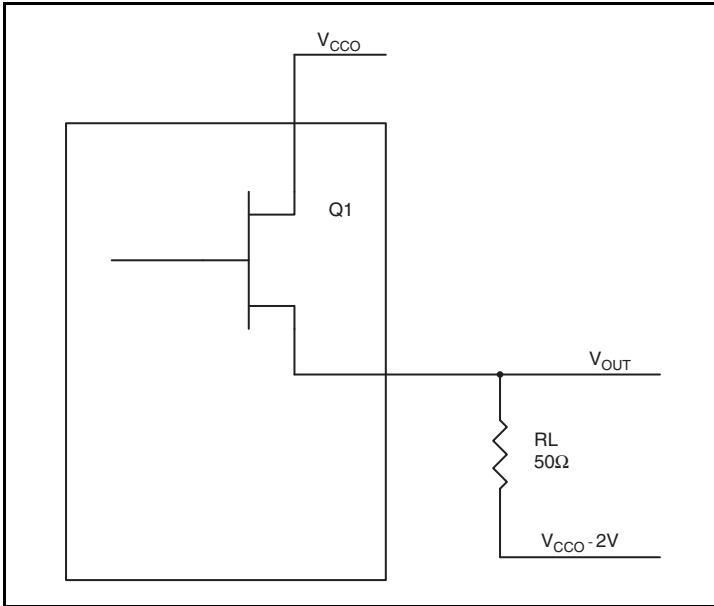
**Table 6. Thermal Resistance  $\theta_{JA}$  for 24 Lead TSSOP, Forced Convection**

$\theta_{JA}$ vs. Air Flow			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

### 3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

LVPECL output driver circuit and termination are shown in *Figure 7*.



**Figure 7. LVPECL Driver Circuit and Termination**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V<sub>CCO</sub> - 2V.

- For logic high, V<sub>OUT</sub> = V<sub>OH\_MAX</sub> = V<sub>CCO\_MAX</sub> - 0.9V  
(V<sub>CCO\_MAX</sub> - V<sub>OH\_MAX</sub>) = 0.9V
- For logic low, V<sub>OUT</sub> = V<sub>OL\_MAX</sub> = V<sub>CCO\_MAX</sub> - 1.7V  
(V<sub>CCO\_MAX</sub> - V<sub>OL\_MAX</sub>) = 1.7V

Pd<sub>H</sub> is power dissipation when the output drives high.

Pd<sub>L</sub> is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = \mathbf{19.8mW}$$

$$Pd_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$$

$$\text{Total Power Dissipation per output pair} = Pd_H + Pd_L = \mathbf{30mW}$$

## Reliability Information

Table 7.  $\theta_{JA}$  vs. Air Flow Table for a 24 Lead TSSOP

$\theta_{JA}$ vs. Air Flow			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65	62

## Transistor Count

The transistor count for 843004I is: 2578

## Package Outline and Package Dimensions

Package Outline - G Suffix for 24 Lead TSSOP

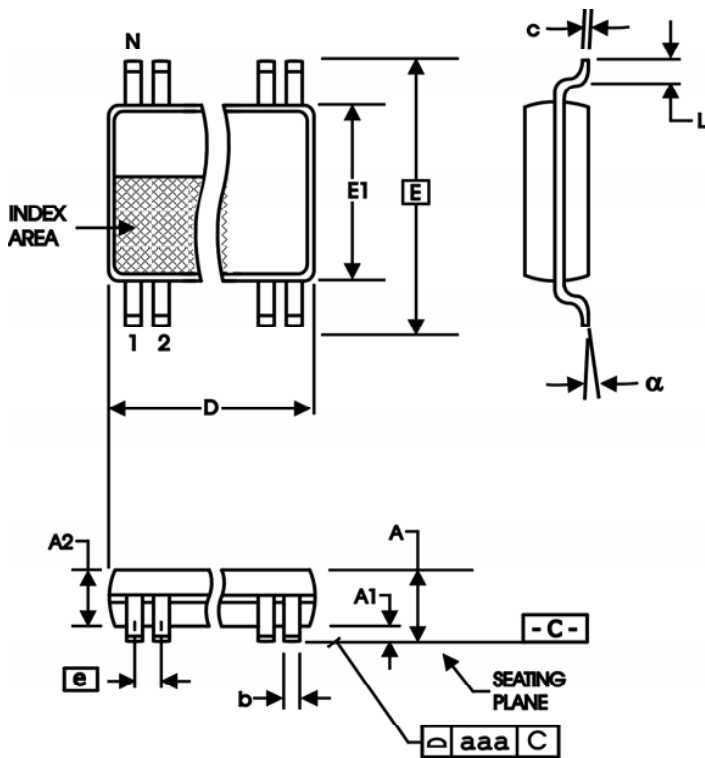


Table 8. Package Dimensions

All Dimensions in Millimeters		
Symbol	Minimum	Maximum
N	24	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
$\alpha$	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153



## Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
843004AGILF	ICS843004AGIL	"Lead-Free" 24 Lead TSSOP	Tube	-40°C to 85°C
843004AGILFT	ICS843004AGIL	"Lead-Free" 24 Lead TSSOP	Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

## Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T5A, T5B	5	AC Characteristics Table - added Thermal Note.	2/19/10
		9	Added <i>Recommendations for Unused Input and Output Pins</i> section.	
		9	Reworded text in <i>Power Supply Filtering Techniques</i> .	
		10	Added <i>Overdriving the XTAL Interface</i> section.	
	11	Updated Figures 4A and 4B.		
	T9	17	Ordering Information Table - added lead-free marking. Deleted "ICS" prefix from part/order number. Datasheet conversion.	
B	T9	17	Ordering Information - removed leaded devices	12/9/14



## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit [www.renesas.com/contact-us/](http://www.renesas.com/contact-us/).