General Description

The ICS8430S07I is a PLL-based clock generator specifically designed for Cavium Networks SoC processors. This high performance device is optimized to generate the processor core reference clock, the DDR reference clocks, the PCI/PCI-X bus clocks, and the clocks for both the Gigabit Ethernet MAC and PHY. The clock generator offers ultra low-jitter, low-skew clock outputs, and edge rates that easily meet the input requirements for the CN3005/CN3010/CN3020 processors. The output frequencies are generated from a 25MHz external input source or an external 25MHz parallel resonant crystal. The extended temperature range of the ICS8430S07I supports telecommunication, networking, and storage requirements.

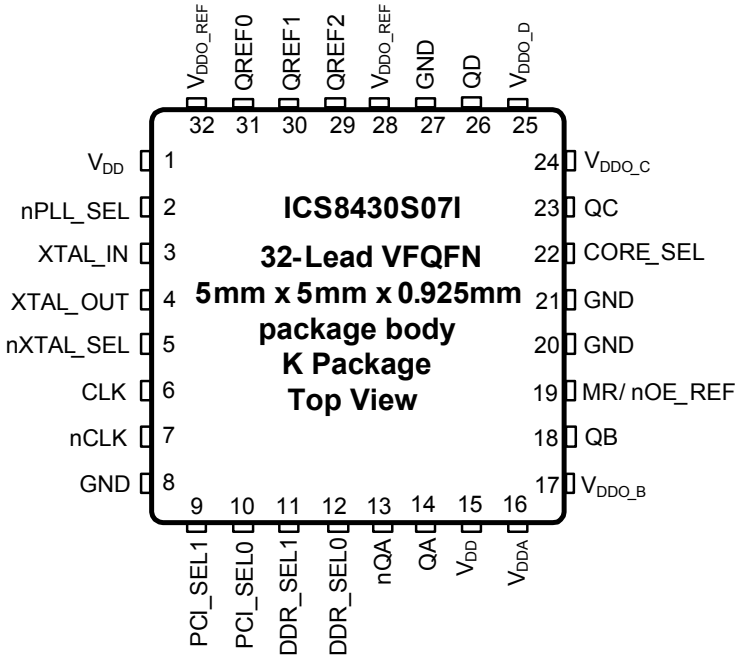
Applications

- Systems using CN30XX MIPS64 Broadband Processors
- Networking, control and storage equipment, including routers, switches, application-aware gateways, triple-play gateways, WLAN and 3G/4G access and aggregation devices, storage arrays, storage networking equipment, servers, and intelligent NICs
- 802.11 a/b/g/n wireless for home data and multi-media distribution
- QoS for high quality Voice, Video, and Data Service
- Next-generation PON, VDSL2, and Cable Networks
- High-performance NAS
- Audio/Video Storage and Distribution
- Consumer Space Media Server

Features

- One selectable differential LVPECL output pair for DDR 533/400/667
- Six LVCMOS/ LVTTL outputs, 15Ω typical output impedance
  - One selectable core clock for the processor
  - One selectable clock for the PCI/ PCI-X bus
  - One 125MHz clock reference for GbE MAC
  - Three 25MHz clock references for GbE PHY
- Selectable external crystal or differential (single-ended) input source
- Crystal oscillator interface designed for 25MHz, parallel resonant crystal
- Differential input pair (CLK, nCLK) accepts LVPECL, LVDS, LVHSTL, SSTL, HCSL input levels
- Internal resistor bias on nCLK pin allows the user to drive CLK input with external single-ended (LVCMOS/ LVTTL) input levels
- RMS phase jitter @ 125MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.78ps (typical), QD output
- Output supply:
  LVPECL – 3.3V Core
  LVCMOS – Core/Output
  3.3V/3.3V
  3.3V/2.5V
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Pin Assignment



Block Diagram

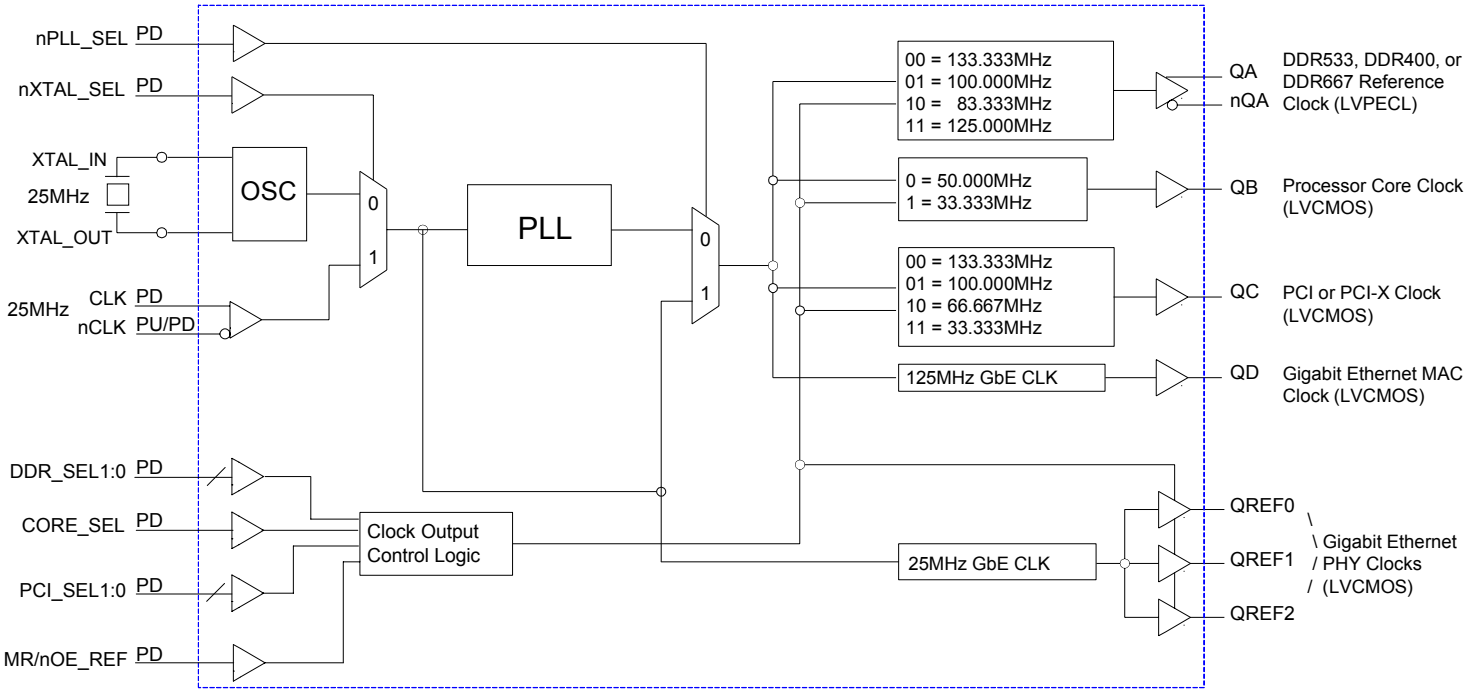


Table 1. Pin Descriptions

Number	Name	Type		Description
1, 15	V_{DD}	Power		Core supply pins.
2	nPLL_SEL	Input	Pulldown	PLL bypass. When LOW, selects PLL (PLL Enable). When HIGH, bypasses the PLL. LVCMOS/LVTTL interface levels.
3, 4	XTAL_IN, XTAL_OUT	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.
5	nXTAL_SEL	Input	Pulldown	Selects XTAL inputs when LOW. Selects differential clock (CLK, nCLK) input when HIGH. LVCMOS/LVTTL interface levels.
6	CLK	Input	Pulldown	Non-inverting differential clock input.
7	nCLK	Input	Pullup/ Pulldown	Inverting differential clock input. Internal resistor bias to $V_{DD}/2$.
8, 20, 21, 27	GND	Power		Power supply ground.
9, 10	PCI_SEL1, PCI_SEL0	Input	Pulldown	Selects the PCI/PCI-X reference clock output frequency. See Table 3C. LVCMOS/LVTTL interface levels.
11, 12	DDR_SEL1, DDR_SEL0	Input	Pulldown	Selects the DDR reference clock output frequency. See Table 3B. LVCMOS/LVTTL interface levels.
13, 14	nQA, QA	Output		Differential output pair. LVPECL interface levels.
16	V_{DDA}	Power		Analog supply pin.
17	V_{DDO_B}	Power		Bank B output supply pin. 3.3 V or 2.5V supply.
18, 23, 26, 29, 30, 31	QB, QC, QD, QREF2, QREF1, QREF0	Output		Single-ended outputs. LVCMOS/LVTTL interface levels.
19	MR/nOE_REF	Input	Pulldown	Active HIGH Master Reset. Active LOW output enable. When logic HIGH, the internal dividers are reset and the QREF[2:0] outputs are in high impedance (HI-Z). When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/ LVTTL interface levels.
22	CORE_SEL	Input	Pulldown	Selects the processor core clock output frequency. The output frequency is 50MHz when LOW, and 33.333MHz when HIGH. See Table 3A. LVCMOS/LVTTL interface levels.
24	V_{DDO_C}	Power		Bank C output supply pin. 3.3 V or 2.5V supply.
25	V_{DDO_D}	Power		Bank D output supply pin. 3.3 V or 2.5V supply.
28, 32	V_{DDO_REF}	Power		REF bank output supply pins. 3.3 V or 2.5V supply.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				2		pF
C_{PD}	Power Dissipation Capacitance (per output)		V_{DD}, V_{DDO_X} = 3.465V		4		pF
			V_{DD} = 3.465V, V_{DDO_X} = 2.625V		4		pF
R_{PULLUP}	Input Pullup Resistor				51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor				51		kΩ
R_{OUT}	Output Impedance	QB, QC, QD, QREF[0:2]	V_{DDO_X} = 3.465V		15		Ω
		QB, QC, QD, QREF[0:2]	V_{DDO_X} = 2.625V		20		Ω

NOTE: V_{DDO_X} denotes V_{DDO_B}, V_{DDO_C}, V_{DDO_D} and V_{DDO_REF}.

Function Tables

Table 3A. QB Output Control Input Function Table

Input	Output Frequency
CORE_SEL	**QB**
0 (default)	50MHz
1	33.333MHz

Table 3B. QA Output Control Input Function Table

Inputs		Output Frequency
DDR_SEL1	**DDR_SEL0**	**QA, nQA**
0 (default)	0 (default)	133.333MHz
0	1	100.000MHz
1	0	83.333MHz
1	1	125.000MHz

Table 3C. QC Output Control Input Function Table

Inputs		Output Frequency
PCI_SEL1	**PCI_SEL0**	**QC**
0 (default)	0 (default)	133.333MHz
0	1	100.000MHz
1	0	66.6667MHz
1	1	33.333MHz

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O (LVCMOS)	-0.5V to V_{DD} + 0.5V
Outputs, I_O (LVPECL) Continuos Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA}	39.5°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO\_X} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.20	3.3	V_{DD}	V
V_{DDO_X}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				170	mA
I_{DDA}	Analog Supply Current				20	mA
I_{DDO_X}	Output Supply Current				25	mA

NOTE: V_{DDO_X} denotes V_{DDO_B}, V_{DDO_C}, V_{DDO_D} and V_{DDO_REF}.
NOTE: I_{DDO_X} = I_{DDO_B}, I_{DDO_C}, I_{DDO_D} and I_{DDO_REF}.

Table 4B. Power Supply DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO\_X} = 2.5V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.20	3.3	V_{DD}	V
V_{DDO_X}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				160	mA
I_{DDA}	Analog Supply Current				20	mA
I_{DDO_X}	Output Supply Current				20	mA

NOTE: V_{DDO_X} denotes V_{DDO_B}, V_{DDO_C}, V_{DDO_D} and V_{DDO_REF}.
NOTE: I_{DDO_X} = I_{DDO_B}, I_{DDO_C}, I_{DDO_D} and I_{DDO_REF}.

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO_X} = 3.3V ± 5% or 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	nPLL_SEL, CORE_SEL, nXTAL_SEL, PCI_SEL[0:1], DDR_SEL[0:1], MR/nOE_REF	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	nPLL_SEL, CORE_SEL, nXTAL_SEL, PCI_SEL[0:1], DDR_SEL[0:1], MR/nOE_REF	V_{DD} = 3.465V, V_{IN} = 0V	-10			µA
V_{OH}	Output High Voltage; NOTE 1		V_{DDO_X} = 3.465V	2.6			V
			V_{DDO_X} = 2.625V	1.8			V
V_{OL}	Output Low Voltage: NOTE 1		V_{DDO_X} = 3.465V or 2.625V			0.6	V

NOTE 1: Outputs terminated with 50Ω to V_{DDO_X}/2. See Parameter Measurement Information, *Output Load Test Circuit diagram.*

Table 4C. Differential DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK/nCLK	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	CLK	V_{DD} = 3.465V, V_{IN} = 0V	-10			µA
		nCLK	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			0.5		V_{DD} – 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2. Common mode voltage is defined as V_{IH}.

Table 4D. LVPECL DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{DD} – 1.4		V_{DD} – 0.8	V
V_{OL}	Output Low Voltage; NOTE 1		V_{DD} – 2.0		V_{DD} – 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.55		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{DD} – 2V.

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				300	μW

NOTE: Characterized using an 18pF parallel resonant crystal.

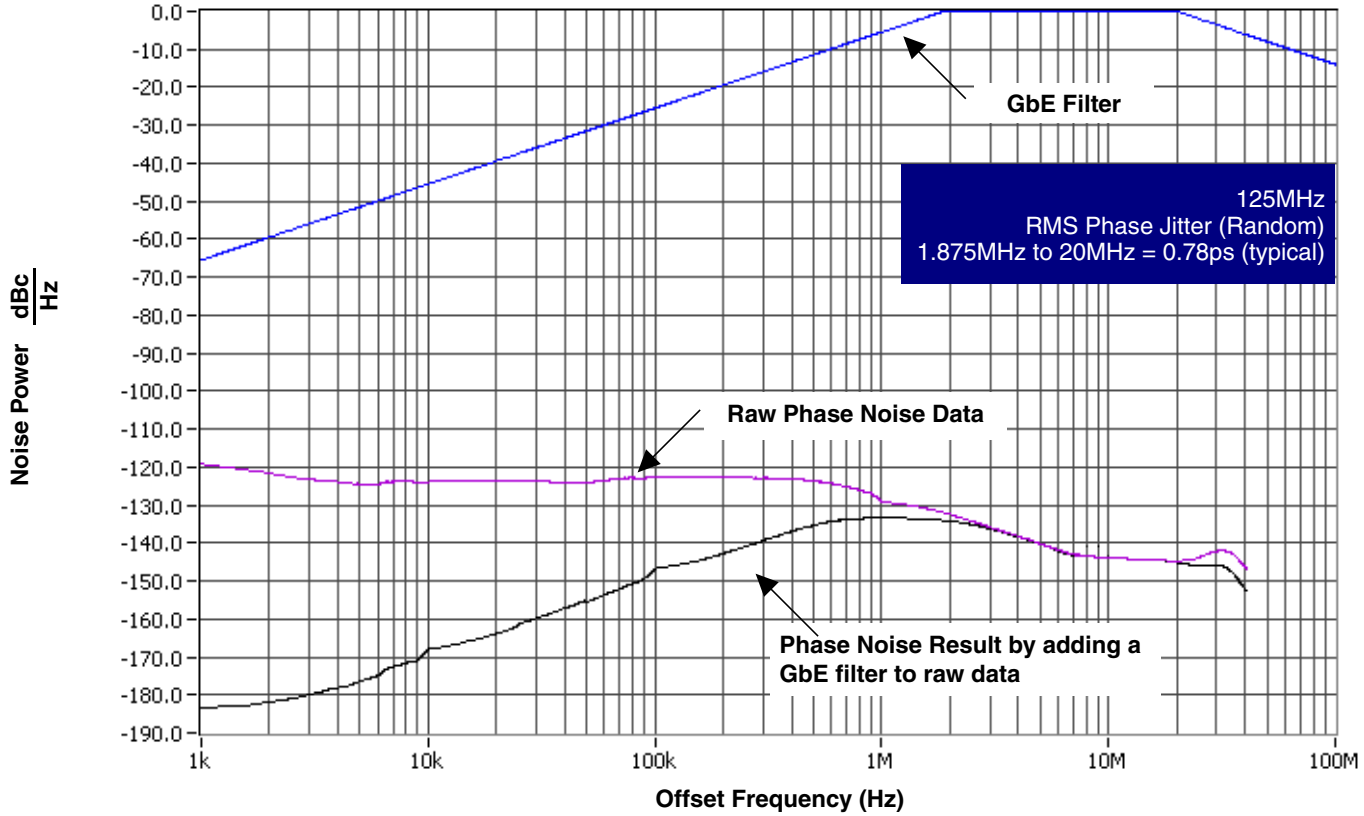
AC Electrical Characteristics

Table 6. AC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO_X} = 3.3V ± 5% or 2.5V ± 5%, T_A = -40°C to 85°C

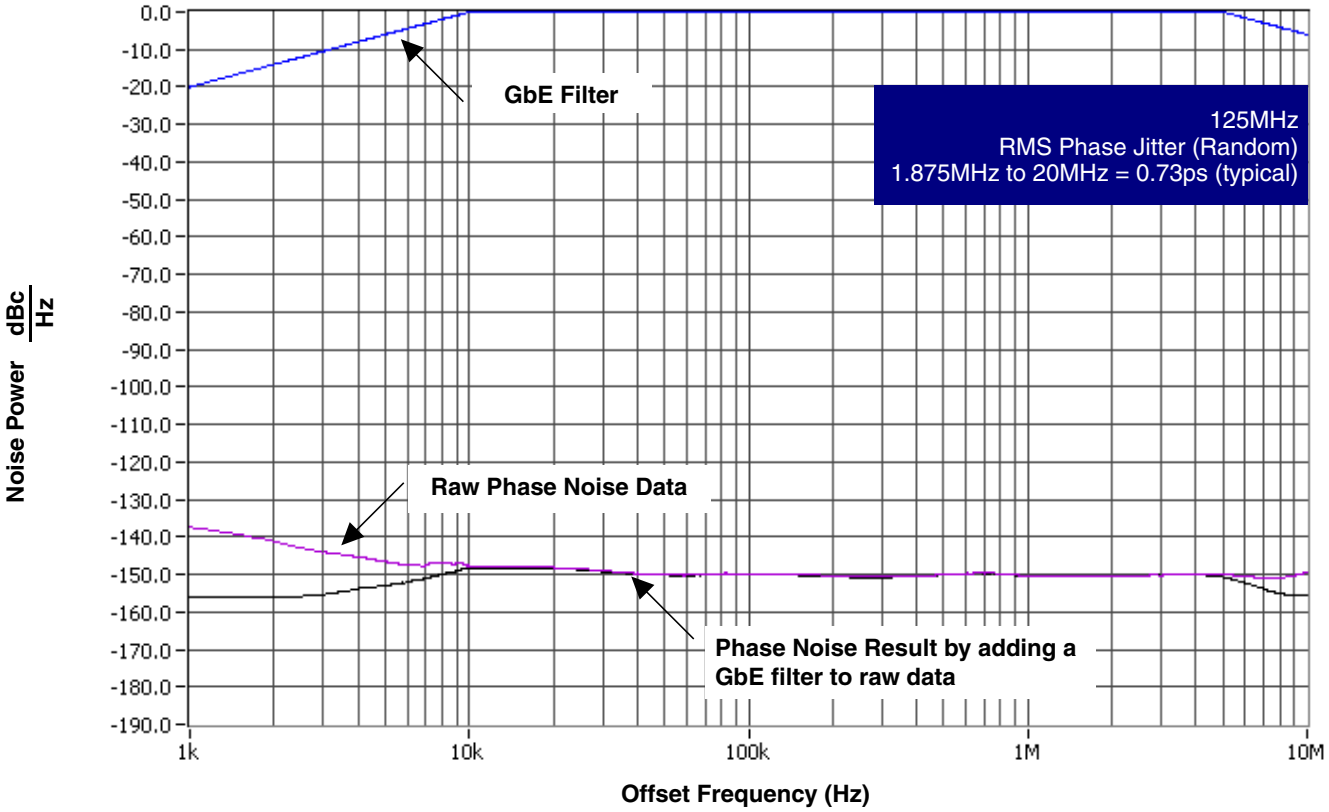
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	QA/nQA	DDR_SEL[1:0] = 00		133.333		MHz
		QA/nQA	DDR_SEL[1:0] = 01		100		MHz
		QA/nQA	DDR_SEL[1:0] = 10		83.333		MHz
		QA/nQA	DDR_SEL[1:0] = 11		125		MHz
		QB	CORE_SEL = 0		50		MHz
		QB	CORE_SEL = 1		33.333		MHz
		QC	PCI_SEL[1:0] = 00		133.333		MHz
		QC	PCI_SEL[1:0] = 01		100		MHz
		QC	PCI_SEL[1:0] = 10		66.667		MHz
		QC	PCI_SEL[1:0] = 11		33.333		MHz
		QD			125		MHz
		QREF[0:2]			25		MHz
*t*sk(b)	Bank Skew; NOTE 2, 4	QREF[0:2]				35	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4	QREF[0:2]				400	ps
tjit(cc)	Cycle-to-Cycle Jitter; NOTE 4, 5	QB, QC,				270	ps
		QA/nQA	measured at crosspoint			95	ps
		QD				200	ps
tjit(per)	Period Jitter (pk-pk); NOTE 4	QA/nQA	measured at crosspoint	-90		90	ps
tjit(hper)	Half-period Jitter (pk-pk)	QA/nQA	measured at crosspoint	-90		90	ps
tjit(Ø)	RMS Phase Jitter, (Random); NOTE 1	QREF[0:2]	25MHz (10kHz to 5MHz)		0.73		ps
		QD	125MHz (1.875MHz to 20MHz)		0.78		ps
t_R / t_F	Output Rise/Fall Time	QB	20% to 80%	100		450	ps
		QA/nQA		100		300	ps
		QC, QREF[0:2]		100		450	ps
		QD		100		450	ps
odc	Output Duty Cycle	QA/nQA		49		51	%
		QB, QC, QD, QREF[0:2]		45		55	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Refer to the phase noise plot.
NOTE 2: Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDO}/2.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 5: All outputs running at corresponding f_{MAX}.

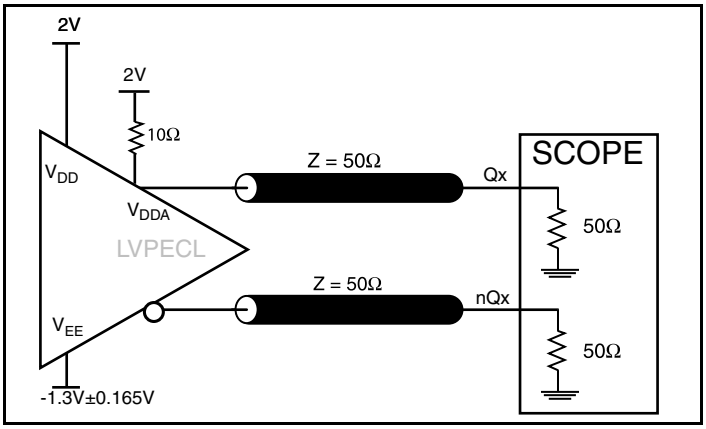
Typical Phase Noise at 125MHz (QD output @ 3.3V)



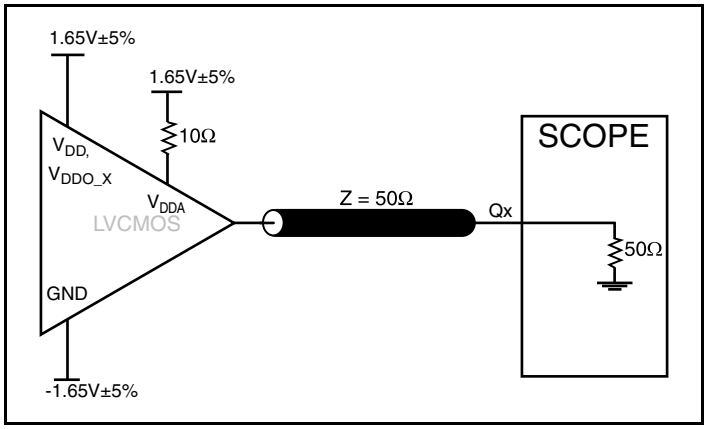
Typical Phase Noise at 25MHz (QREF output @ 3.3V)



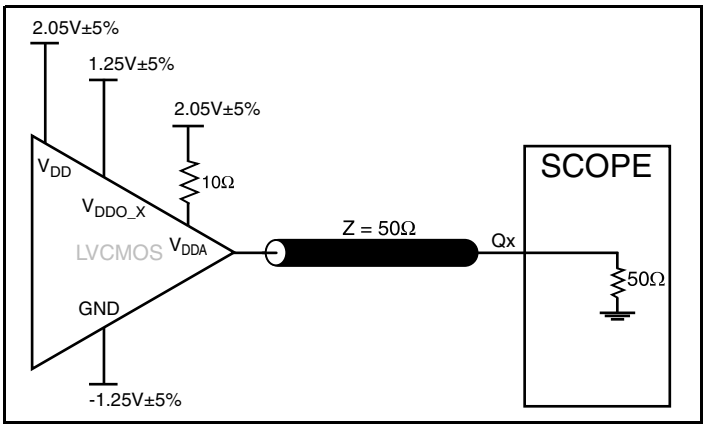
Parameter Measurement Information



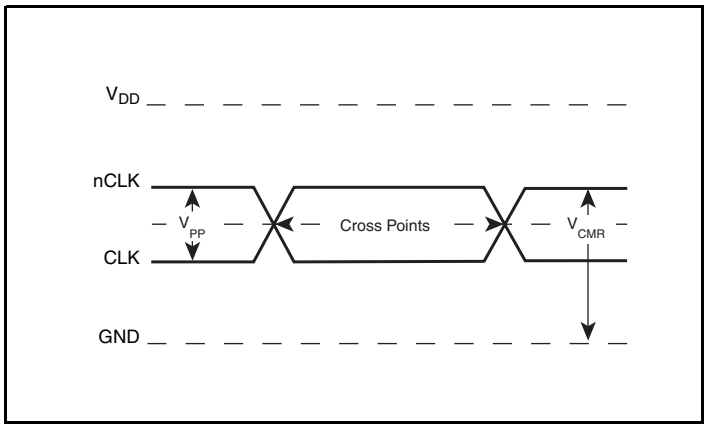
3.3V Core/3.3V LVPECL Output Load AC Test Circuit



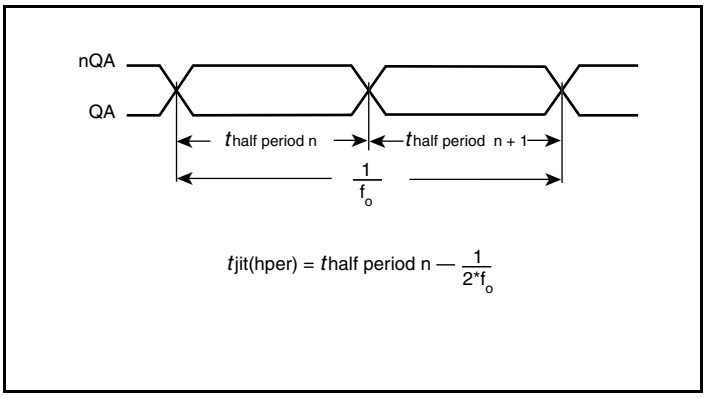
3.3V Core/3.3V LVCMOS Output Load AC Test Circuit



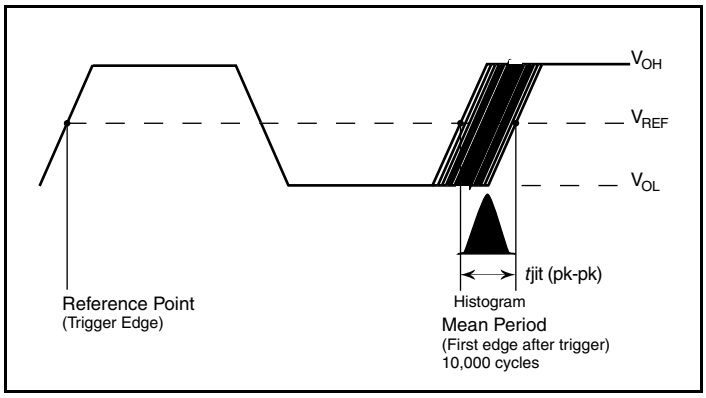
3.3V Core/2.5V LVCMOS Output Load AC Test Circuit



Differential Input Level

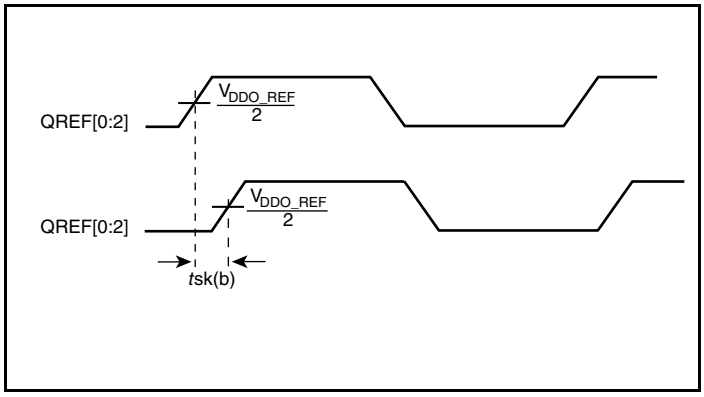


Half Period Jitter

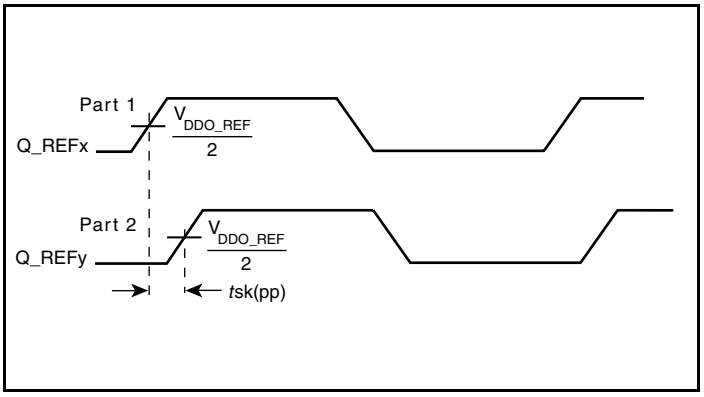


Period Jitter

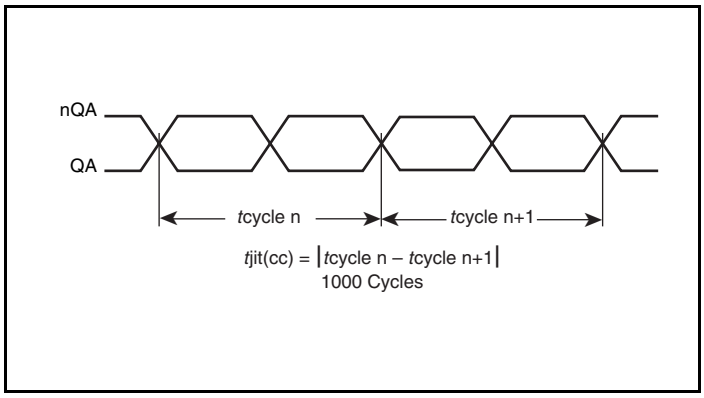
Parameter Measurement Information, continued



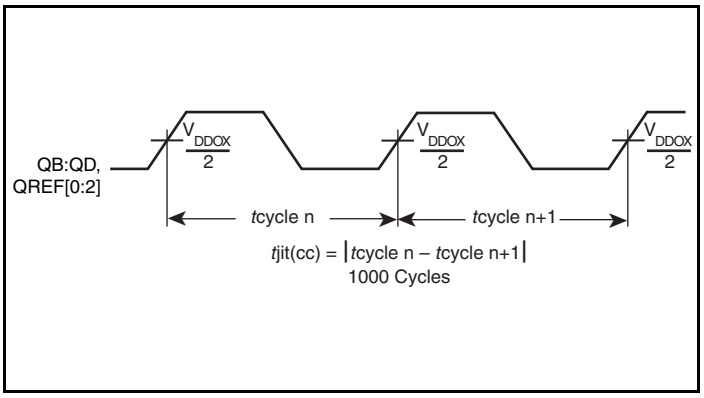
LVCMOS Bank Skew



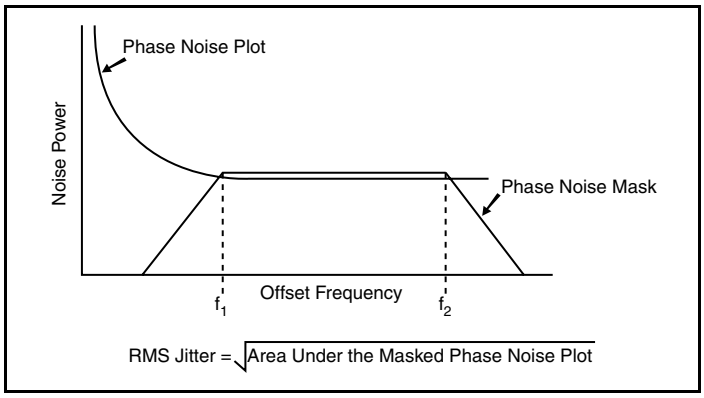
LVCMOS Part-to-Part Skew



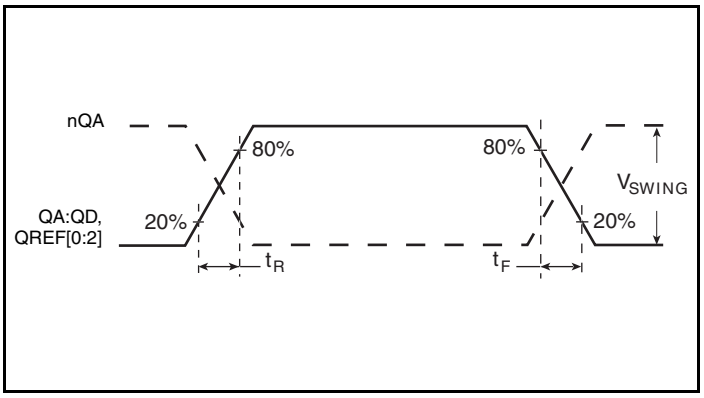
LVPECL Cycle-to-Cycle Jitter



LVCMOS Cycle-to-Cycle Jitter

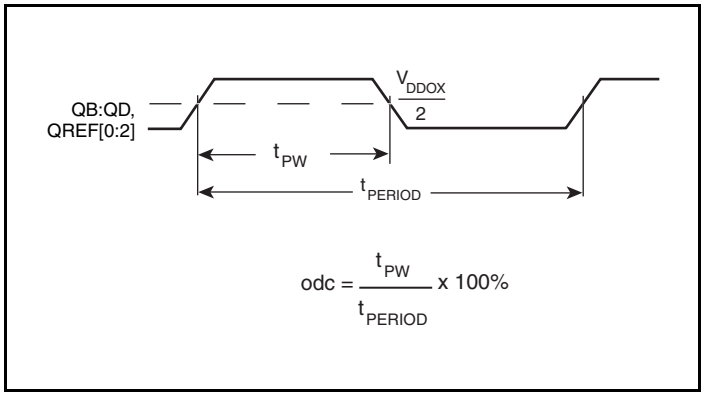


RMS Phase Jitter

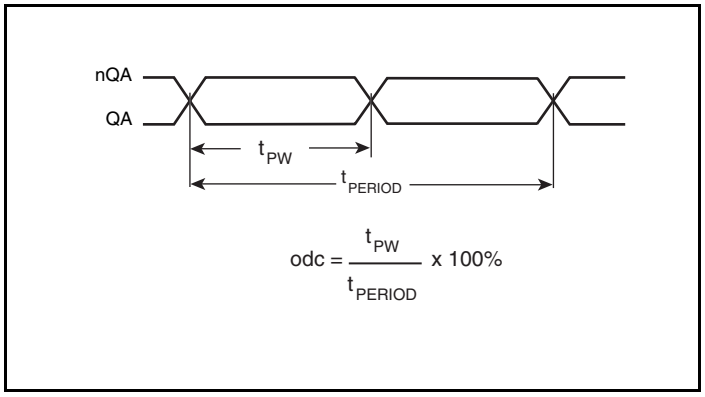


Output Rise/Fall Time

Parameter Measurement Information, continued



LVCMOS Output Duty Cycle/Pulse Width/Period



LVPECL Output Duty Cycle/Pulse Width/Period

Application Information

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how the differential input can be wired to accept single-ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

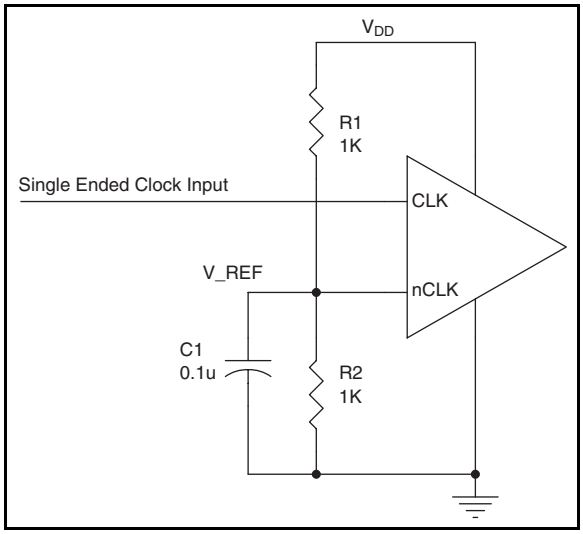


Figure 1. Single-Ended Signal Driving Differential Input

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter perform ance, power supply isolation is required. The ICS8430S07I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA} and V_{DDO_X} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 2* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

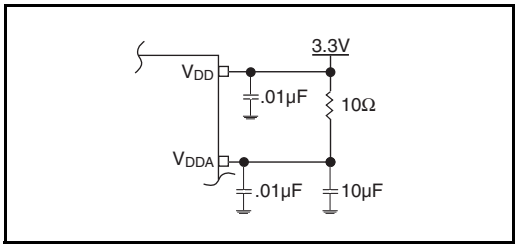


Figure 2. Power Supply Filtering

Recommendations for Unused Input and Output Pins

Inputs:

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

LVCMOS Control Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

The unused LVPECL output can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVCMOS Outputs

All unused LVCMOS output can be left floating. There should be no trace attached.

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3F* show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 3A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

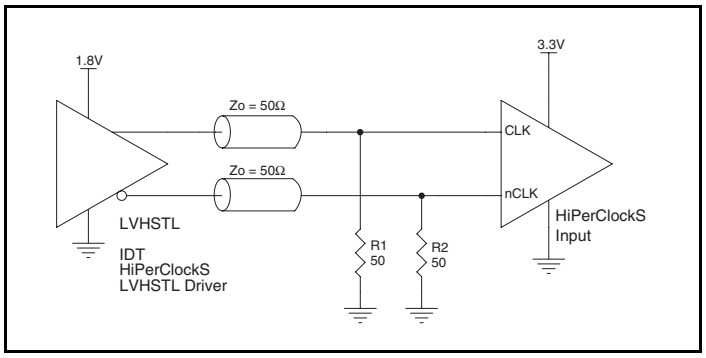


Figure 3A. HiPerClockS CLK/nCLK Input Driven by an IDT Open Emitter HiPerClockS LVHSTL Driver

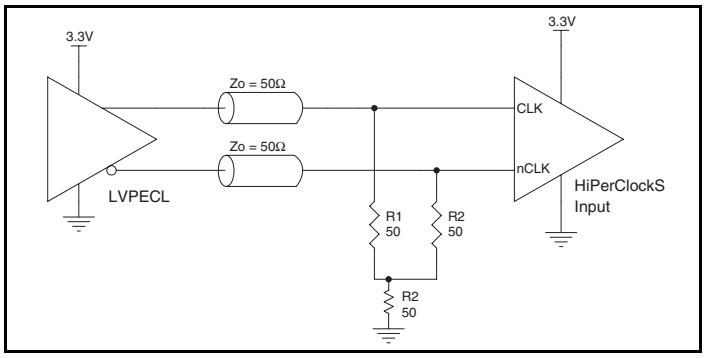


Figure 3B. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

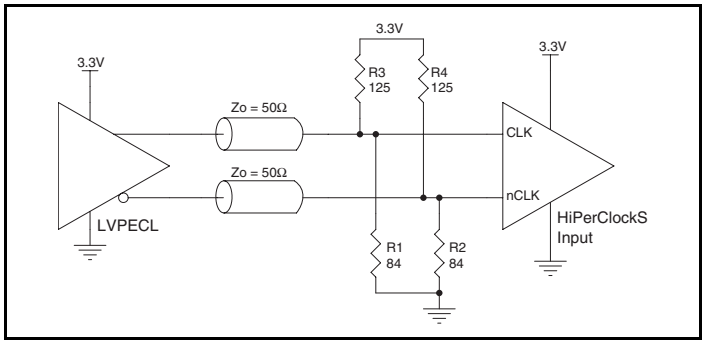


Figure 3C. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

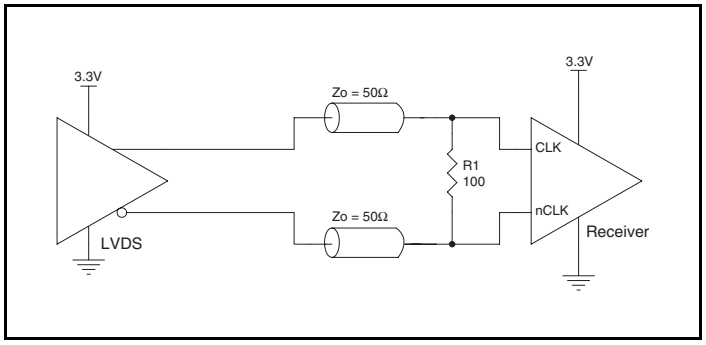


Figure 3D. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVDS Driver

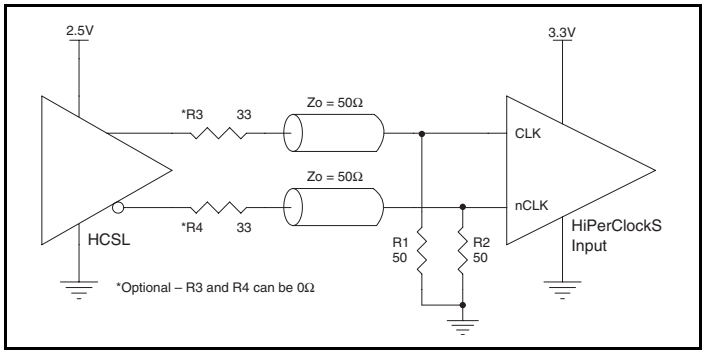


Figure 3E. HiPerClockS CLK/nCLK Input Driven by a 3.3V HCSL Driver

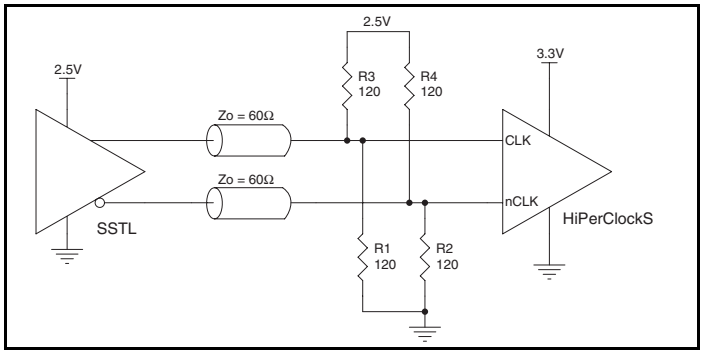


Figure 3F. HiPerClockS CLK/nCLK Input Driven by a 2.5V SSTL Driver

Crystal Input Interface

The ICS8430S07I has been characterized with 18pF parallel resonant crystals. The capacitors C1 and C2 are not required, but can be populated for optimal ppm accuracy. The C1 and C2 values can be slightly adjusted to minimize ppm error for different board layouts.

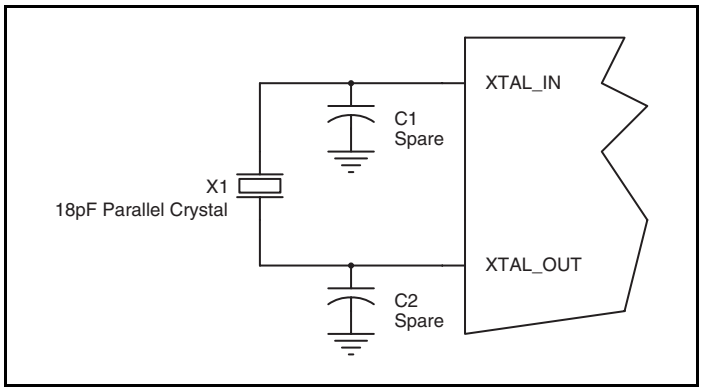


Figure 4. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 5.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS signals, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

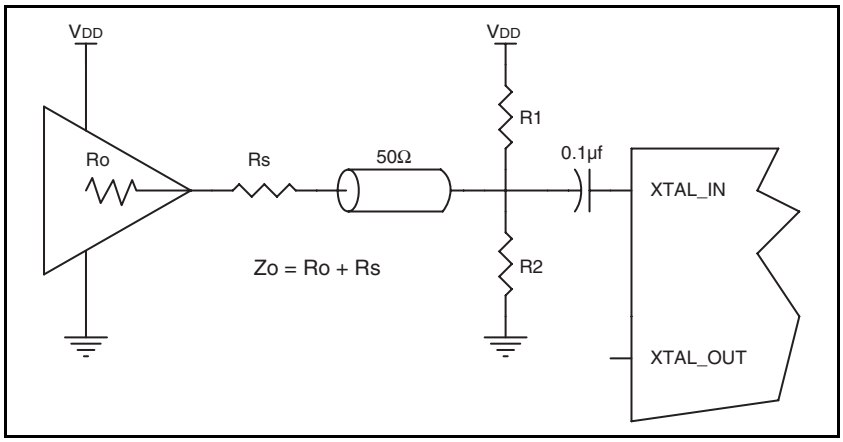


Figure 5. General Diagram for LVCMOS Driver to XTAL Input Interface

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential output pair is low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 6A and 6B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

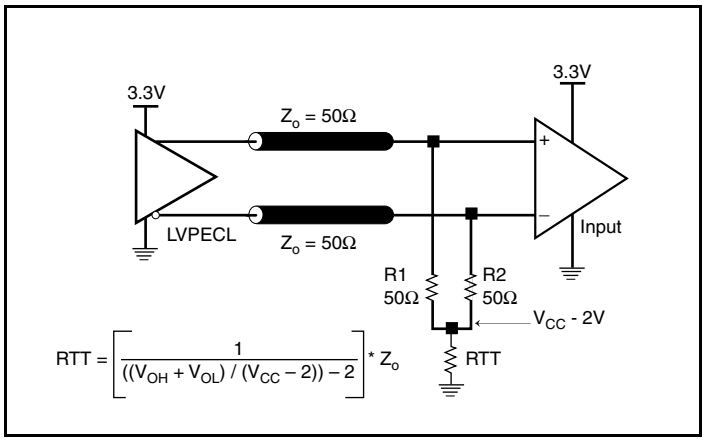


Figure 6A. 3.3V LVPECL Output Termination

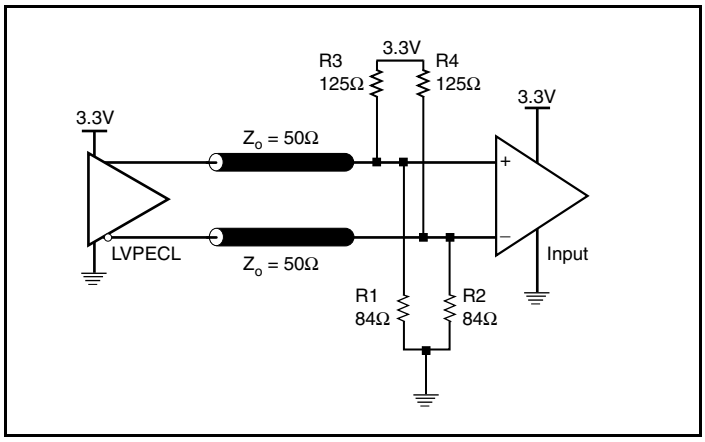


Figure 6B. 3.3V LVPECL Output Termination

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 7*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

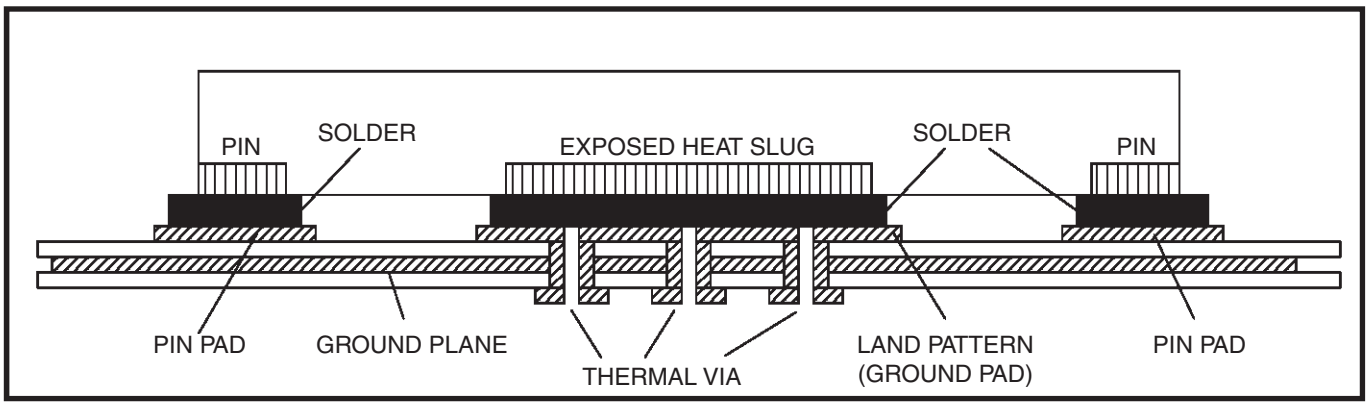


Figure 7. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Application Schematic

Figure 8 shows a schematic example of using an ICS8430S07I. The crystal inputs are parallel resonant crystal with load capacitor CL=18pF. The frequency fine tuning capacitors C1 and C2 are optional. The tuning capacitor value can be slightly adjusted to optimize the frequency accuracy. This schematic example shows hardwired logic control input handling. The logic inputs can also be driven by 3.3V LVCMOS drivers. It is recommended to have one bypass capacitor per power pin. In general, the bypass capacitor values are ranged from 0.01uF to 0.1uF. Each bypass capacitor should be located as close as possible to the power pin. The low pass filter R6, C3 and C4 for clean analog supply should also be located as close to the V_{DDA} pin as possible. Only two examples of LVPECL termination and one example of LVCMOS termination are shown in this schematic. Additional examples of LVPECL terminations and LVCMOS terminations can be found in the LVPECL Termination and LVCMOS Termination Application Notes.

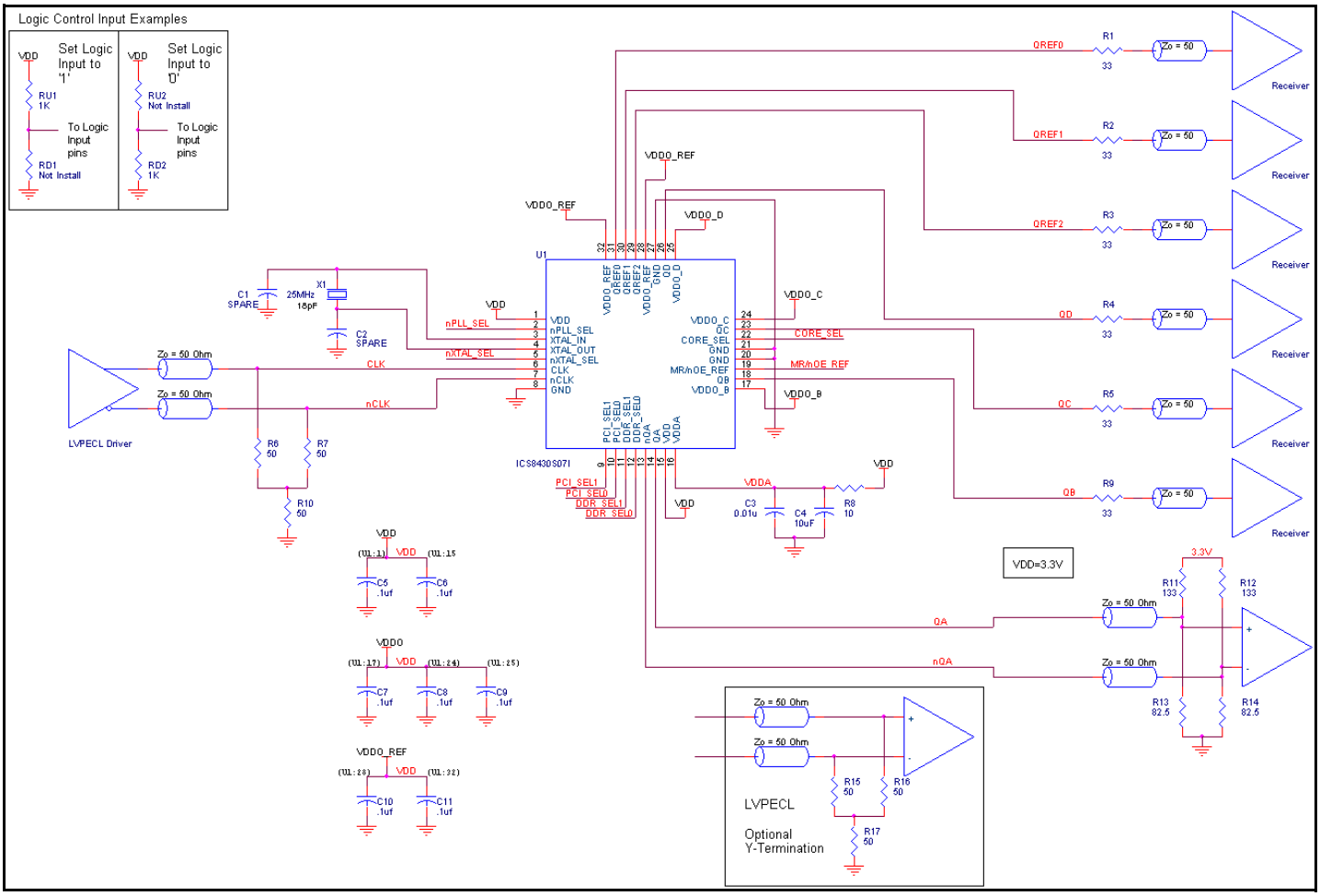


Figure 8. ICS8430S07I Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8430S07I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS8430S07I is the sum of the core power plus the analog power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

Core and LVPECL Output Power Dissipation

- Power (core)$_{\_MAX}$ = V_{DD_MAX} * (I_{EE_MAX} + I_{DDA} + I_{DDO}) = 3.465V * (170mA + 20mA + 25mA) = **744.98mW**
- Power (output)$_{\_MAX}$ = **30mW/Loaded Output Pair**

LVCMOS Output Power Dissipation

- Output Impedance R_{OUT} Power Dissipation due to Loading 50Ω to V_{DDO}/2
  Output Current I_{OUT} = V_{DDO_MAX} / [2 * (50Ω + R_{OUT})] = 3.465V / [2 * (50Ω + 15Ω)] = **26.7mA**
- Power Dissipation on the R_{OUT} per LVCMOS output
  Power (R_{OUT}) = R_{OUT} * (I_{OUT})^2 = 15Ω * (26.7mA)^2 = **10.7mW per output**
- Total Power Dissipation on the R_{OUT}
  Total Power (R_{OUT}) = 10.7mW * 6 = **64.2mW**
- Dynamic Power Dissipation at 25MHz
  Power (25MHz) = C_{PD} * Frequency * (V_{DDO})^2 = 4pF * 25MHz * (3.465V)^2 = **1.5mW per output**
  Total Power (25MHz) = **1.5mW * 3 = 4.5mW**

- Dynamic Power Dissipation at 133MHz
  Power (133MHz) = C_{PD} * Frequency * (V_{DDO})^2 = 4pF * 133MHz * (3.465V)^2 = **8mW per output**
  Total Power (133MHz) = **8mW * 3 = 24mW**

Total Power Dissipation

- **Total Power**
  = Power (core) + Power (LVPECL output) + Total Power (R_{OUT}) + Total Power (25MHz) + Total Power (125MHz)
  = 745mW + 30mW + 64.2mW + 4.5mW + 24mW
  = 867.7mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 39.5°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.868W * 39.5°C/W = 119.2°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board.

Table 7. Thermal Resistance θ_{JA} for 32 Lead VFQFN, Forced Convection

θ_{JA} **Vs. Air Flow**			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	39.5°C/W	34.5°C/W	31.0°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 9.*

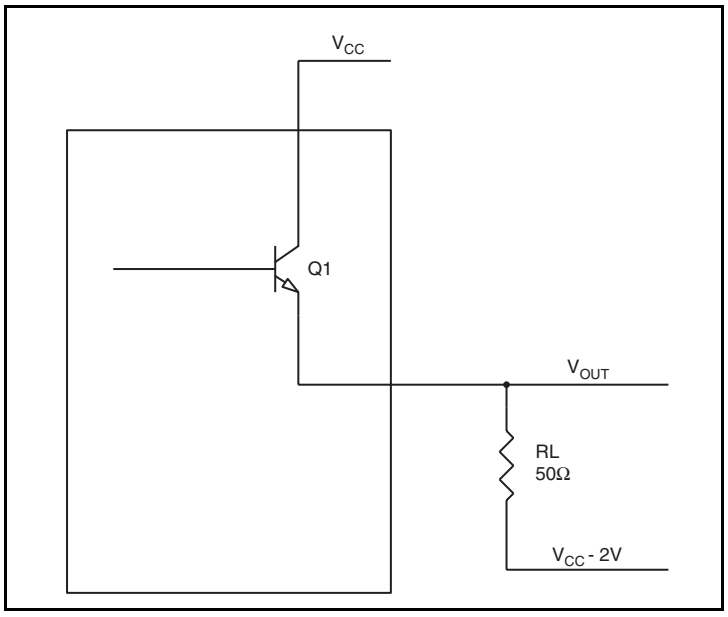


Figure 9. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{DD} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{DD\_MAX} – 0.9V}$
  $(V_{DD\_MAX} – V_{OH\_MAX}) = \mathbf{0.9V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{DD\_MAX} – 1.7V}$
  $(V_{DD\_MAX} – V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{DD\_MAX} – 2V))/R_L] * (V_{DD\_MAX} – V_{OH\_MAX}) = [(2V – (V_{DD\_MAX} – V_{OH\_MAX}))/R_L] * (V_{DD\_MAX} – V_{OH\_MAX}) =$
$[(2V – 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{DD\_MAX} – 2V))/R_L] * (V_{DD\_MAX} – V_{OL\_MAX}) = [(2V – (V_{DD\_MAX} – V_{OL\_MAX}))/R_L] * (V_{DD\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 32 Lead VFQFN

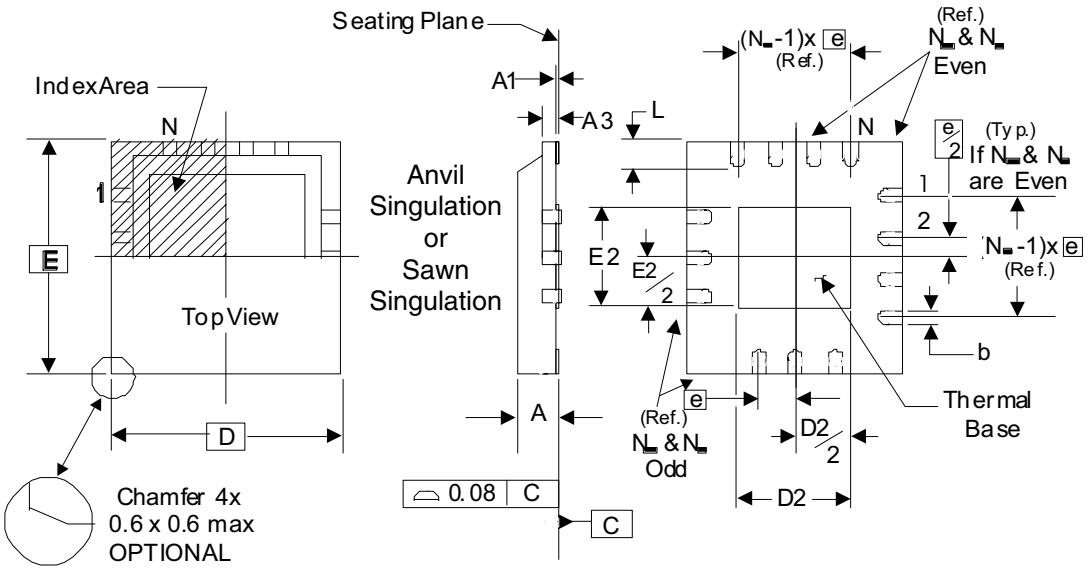
θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	39.5°C/W	34.5°C/W	31.0°C/W

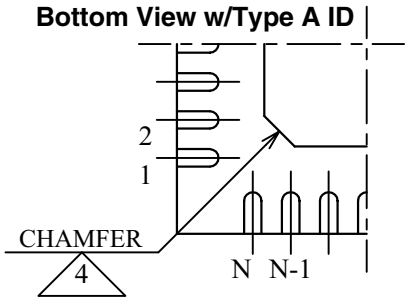
Transistor Count

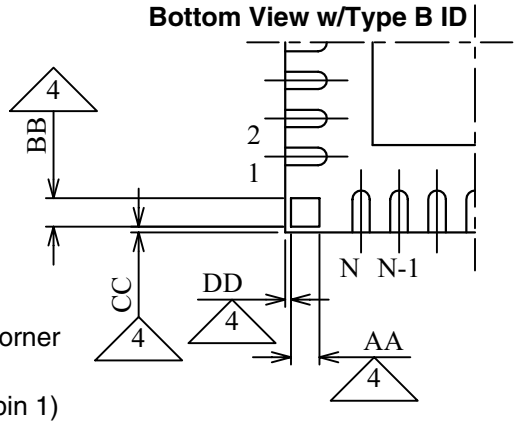
The transistor count for ICS8430S07I is: 10,871

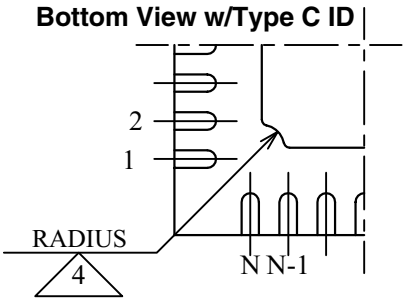
Package Outline and Package Dimensions

Package Outline - K Suffix for 32 Lead VFQFN









There are 3 methods of indicating pin 1 corner at the back of the VFQFN package are:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type B: Dummy pad between pin 1 and N.
3. Type C: Mouse bite on the paddle (near pin 1)

Table 9. Package Dimensions

JEDEC Variation: VHHD-2/-4 All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A	0.80		1.00
A1	0		0.05
A3		0.25 Ref.	
b	0.18	0.25	0.30
N_D & N_E			8
D & E		5.00 Basic	
D2 & E2	3.0		3.3
e		0.50 Basic	
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 9.

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8430S07AKILF	ICS30S07AIL	“Lead-Free” 32 Lead VFQFN	Tray	-40°C to 85°C
8430S07AKILFT	ICS30S07AIL	“Lead-Free” 32 Lead VFQFN	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A		23	Package Outline & Dimensions - added pin 1 indicator in package drawing.	9/3/09

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