

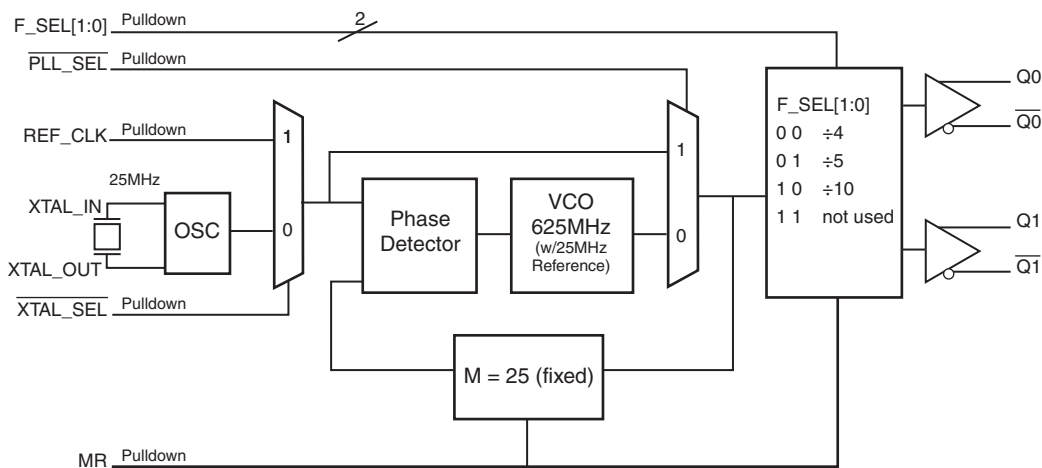
## Description

The 844002-01 is a 2 output LVDS Synthesizer optimized to generate Ethernet reference clock frequencies. Using a 25MHz, 18pF parallel resonant crystal, the following frequencies can be generated based on the 2 frequency select pins (F\_SEL[1:0]): 156.25MHz, 125MHz and 62.5MHz. The 844002-01 uses IDT's 3<sup>rd</sup> generation low phase noise VCO technology and can achieve <1ps typical rms phase jitter, easily meeting Ethernet jitter requirements. The 844002-01 is packaged in a small 20-pin TSSOP package.

## Features

- Two differential LVDS outputs
- Selectable crystal oscillator interface or single-ended LVCMOS/LVTTL input
- Supports the following output frequencies: 156.25MHz, 125MHz, 62.5MHz
- VCO range: 560MHz – 680MHz
- RMS phase jitter @ 156.25MHz, using a 25MHz crystal (1.875MHz – 20MHz): 0.41ps (typical)
- Full 3.3V and 2.5V supply modes
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package

## Block Diagram



## Pin Assignment

nc	1	20	VDDO
VDDO	2	19	Q1
Q0	3	18	Q1̄
Q0̄	4	17	GND
MR	5	16	nc
PLL_SEL	6	15	XTAL_SEL
nc	7	14	REF_CLK
VDDA	8	13	XTAL_IN
F_SEL0	9	12	XTAL_OUT
VDD	10	11	F_SEL1

**844002-01**  
**20-Lead TSSOP**  
**6.5mm x 4.4mm x 0.925mm**  
**package body**  
**G Package**  
**Top View**

**Table 1. Pin Descriptions**

Number	Name	Type		Description
1, 7	nc	Unused		No connect.
2, 20	V <sub>DDO</sub>	Power		Output supply pins.
3, 4	Q0, Q0	Output		Differential output pair. LVDS interface levels.
5	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs Qx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
6	PLL_SEL	Input	Pulldown	Selects between the PLL and REF_CLK as input to the dividers. When LOW, selects PLL (PLL Enable). When HIGH, deselects the reference clock (PLL Bypass). LVCMOS/LVTTL interface levels.
8	V <sub>DDA</sub>	Power		Analog supply pin.
9, 11	FSEL0, F_SEL1	Input	Pulldown	Frequency select pins. LVCMOS/LVTTL interface levels.
10	V <sub>DD</sub>	Power		Core supply pins.
12, 13	XTAL_OUT, XTAL_IN	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.
14	REF_CLK	Input	Pulldown	Non-inverting differential clock input.
15	XTAL_SEL	Input	Pulldown	Selects between crystal or REF_CLK inputs as the PLL Reference source. Selects XTAL inputs when LOW. Selects REF_CLK when HIGH. LVCMOS/LVTTL interface levels.
16	nc	Unused		No connect.
17	GND	Power		Power supply ground.
18, 19	Q1, Q1	Output		Differential output pair. LVDS interface levels.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5V$
Outputs, $I_O$ Continuous Current Surge Current	10mA 15mA
Package Thermal Impedance, $\theta_{JA}$	73.2°C/W (0 lfpm)
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

**Table 3A. Power Supply DC Characteristics,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{DDA}$	Analog Supply Voltage		$V_{DD} - 0.13$	3.3	$V_{DD}$	V
$V_{DDO}$	Output Supply Voltage		3.135	3.3	3.465	V
$I_{DD}$	Power Supply Current				105	mA
$I_{DDA}$	Analog Supply Current				13	mA
$I_{DDO}$	Output Supply Current				110	mA

**Table 3B. Power Supply DC Characteristics,  $V_{DD} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Core Supply Voltage		2.375	2.5	2.625	V
$V_{DDA}$	Analog Supply Voltage		$V_{DD} - 0.12$	2.5	$V_{DD}$	V
$V_{DDO}$	Output Supply Voltage		2.375	2.5	2.625	V
$I_{DD}$	Power Supply Current				98	mA
$I_{DDA}$	Analog Supply Current				12	mA
$I_{DDO}$	Output Supply Current				98	mA

**Table 3C. LVCMOS/LVTTL DC Characteristics,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	3.465V	2		$V_{DD} + 0.3$	V
		2.625V	1.7		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage	3.465V	-0.3		0.8	V
		2.625V	-0.3		0.7	V
$I_{IH}$	Input High Current	REF_CLK, MR, FSEL0, FSEL1, PLL_SEL, XTAL_SEL	$V_{DD} = V_{IN} = 3.465V$ or $2.625V$		150	$\mu A$
$I_{IL}$	Input Low Current	REF_CLK, MR, FSEL0, FSEL1, PLL_SEL, XTAL_SEL	$V_{DD} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	-5		$\mu A$

**Table 3D. LVDS DC Characteristics,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OD}$	Differential Output Voltage		300		600	mV
$\Delta V_{OD}$	$V_{OD}$ Magnitude Change			40		mV
$V_{OS}$	Offset Voltage		1.3	1.5	1.7	V
$\Delta V_{OS}$	$V_{OS}$ Magnitude Change			50		mV

**Table 3E. LVDS DC Characteristics,  $V_{DD} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OD}$	Differential Output Voltage		240		550	mV
$\Delta V_{OD}$	$V_{OD}$ Magnitude Change			40		mV
$V_{OS}$	Offset Voltage		0.7	1.1	1.5	V
$\Delta V_{OS}$	$V_{OS}$ Magnitude Change			50		mV

**Table 4. Crystal Characteristics**

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		22.4	25	27.2	MHz
Equivalent Series Resistance (ESR)				50	$\Omega$
Shunt Capacitance				7	pF
Drive Level				1	mW

## AC Electrical Characteristics

**Table 5A. AC Characteristics,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$**

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency	FSEL[1:0] = 00	140		170	MHz
		FSEL[1:0] = 01	112		136	MHz
		FSEL[1:0] = 10	56		68	MHz
$t_{sk(o)}$	Output Skew; NOTE 1, 2			5	20	ps
$f_{jit}(\emptyset)$	RMS Phase Jitter, (Random); NOTE 3	156.25MHz, (1.875MHz – 20MHz)		0.41		ps
		125MHz, (1.875MHz – 20MHz)		0.44		ps
		62.5MHz, (1.875MHz – 20MHz)		0.47		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80% @ 50MHz	250		550	ps
odc	Output Duty Cycle		48		52	%

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at  $V_{DDO}/2$ .

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Please refer to the Phase Noise Plot.

**Table 5B. AC Characteristics,  $V_{DD} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$**

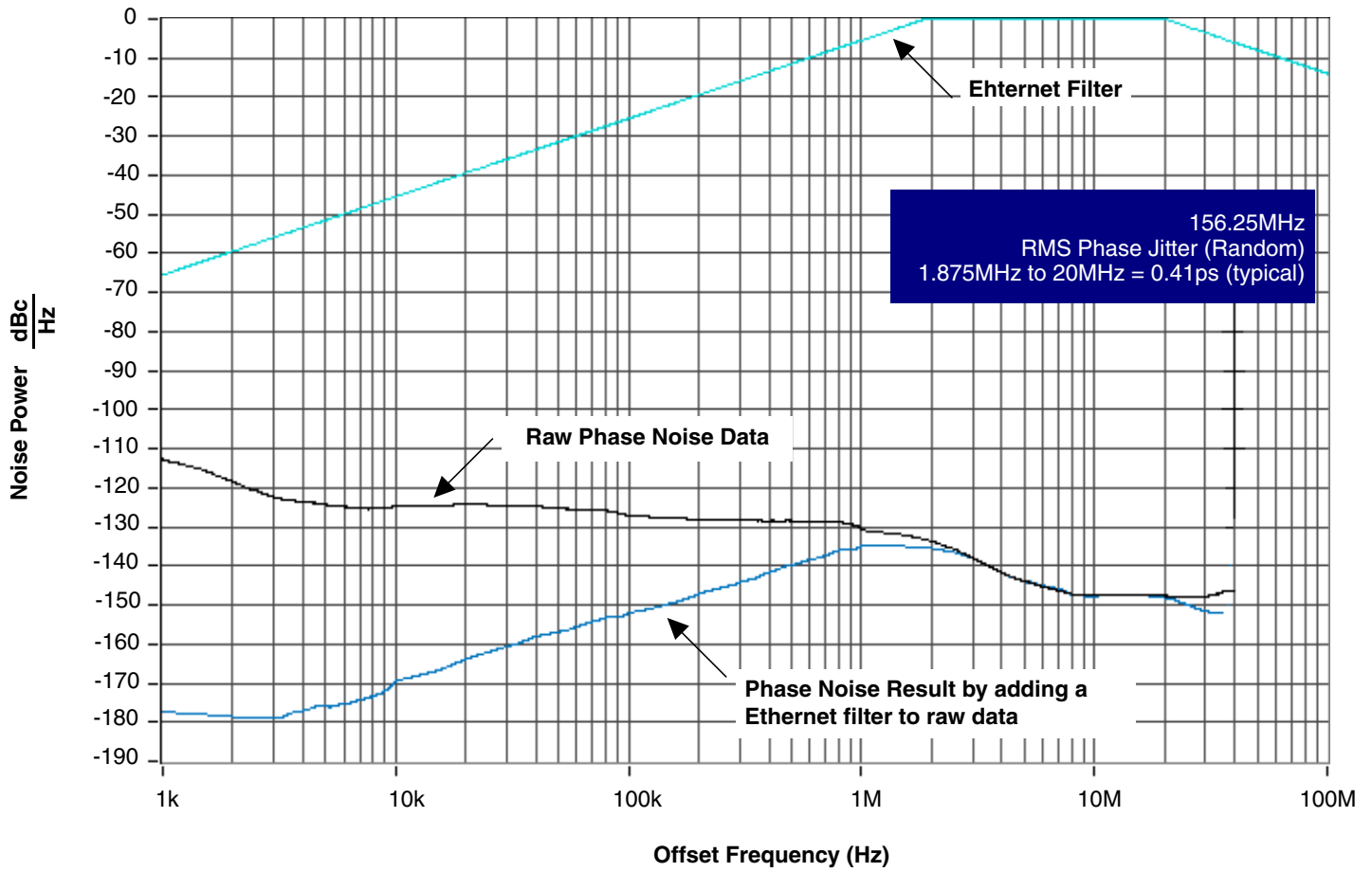
Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency	FSEL[1:0] = 00	140		170	MHz
		FSEL[1:0] = 01	112		136	MHz
		FSEL[1:0] = 10	56		68	MHz
$t_{sk(o)}$	Output Skew; NOTE 1, 2			5	20	ps
$f_{jit}(\emptyset)$	RMS Phase Jitter, (Random); NOTE 3	156.25MHz, (1.875MHz – 20MHz)		0.41		ps
		125MHz, (1.875MHz – 20MHz)		0.44		ps
		62.5MHz, (1.875MHz – 20MHz)		0.47		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80% @ 50MHz	250		550	ps
odc	Output Duty Cycle		48		52	%

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at  $V_{DDO}/2$ .

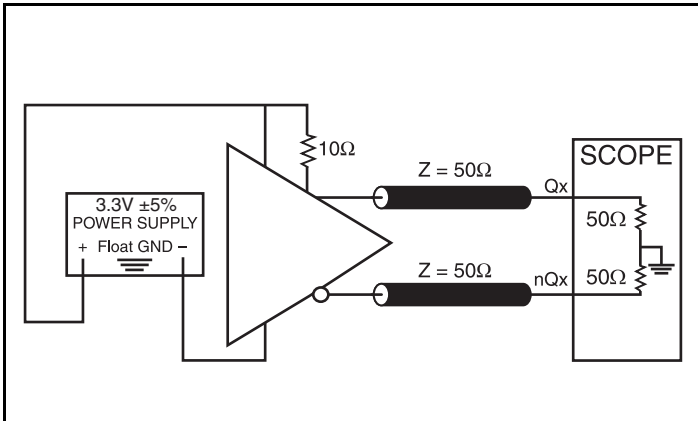
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Please refer to the Phase Noise Plot.

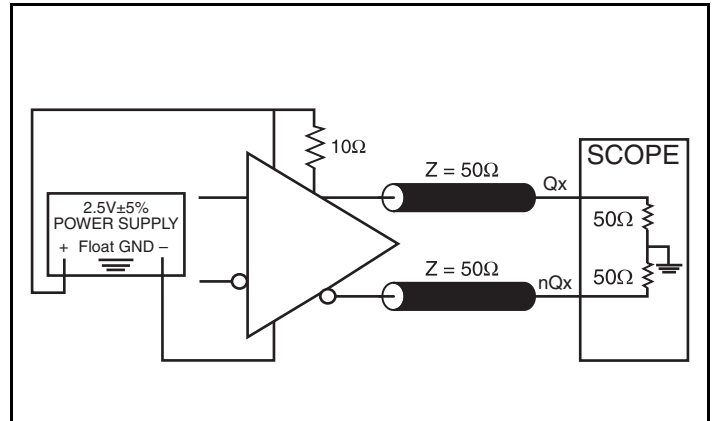
## Typical Phase Noise at 156.25MHz



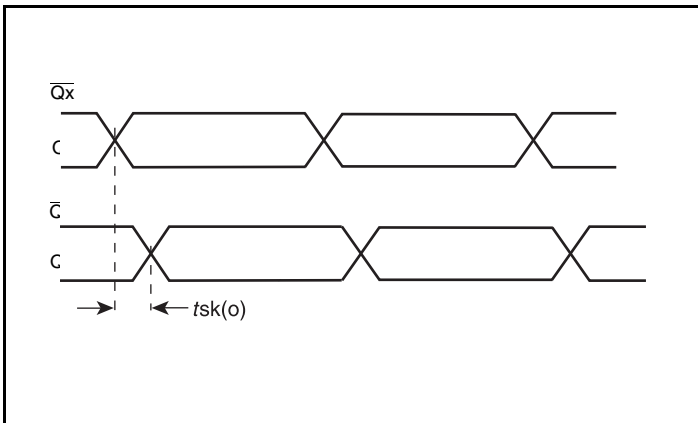
## Parameter Measurement Information



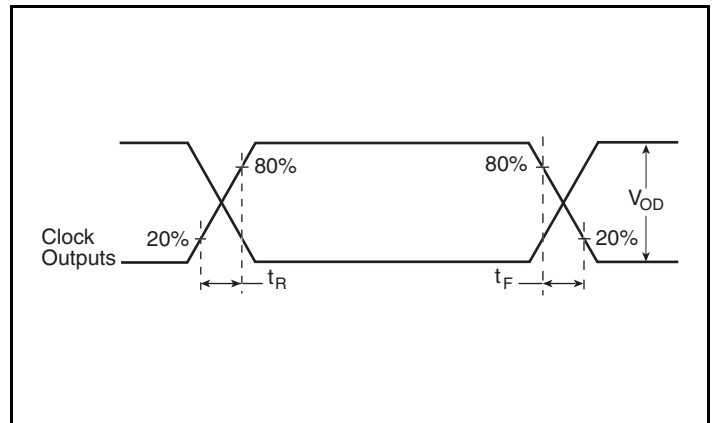
3.3V Output Load AC Test Circuit



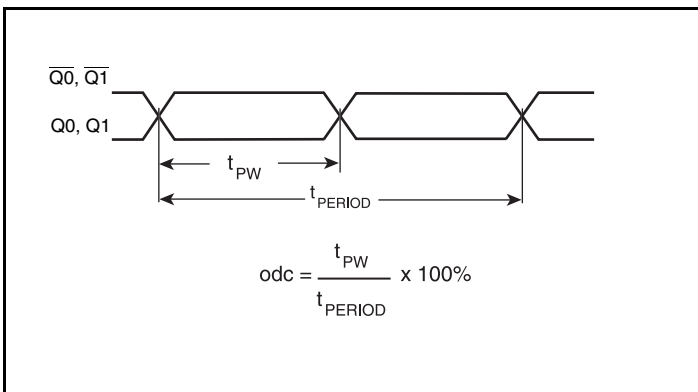
2.5V Output Load AC Test Circuit



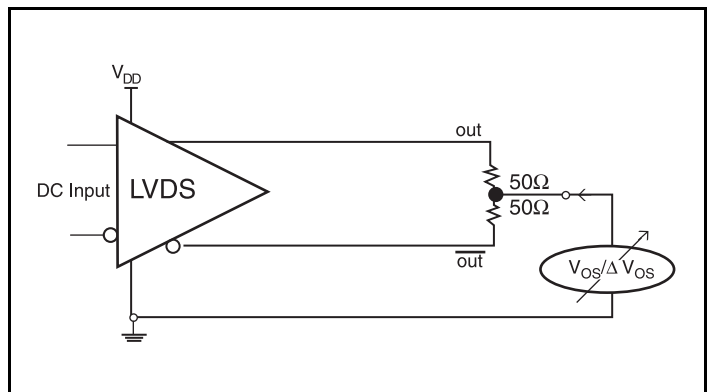
Output Skew



Output Rise/Fall Time

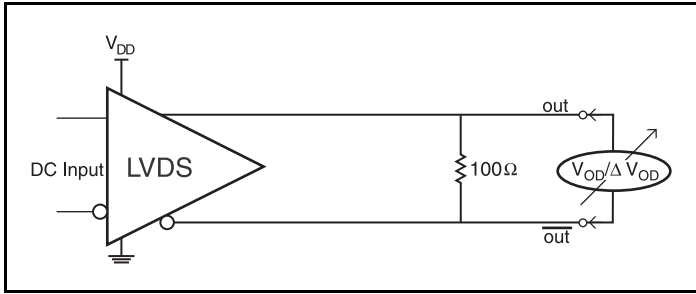


Output Duty Cycle/Pulse Width/Period



Offset Voltage Setup

## Parameter Measurement Information, continued



Differential Offset Voltage Setup

## Application Information

### Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The 844002-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{DD}$ ,  $V_{DDA}$  and  $V_{DDO}$  should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a  $10\Omega$  resistor along with a  $10\mu\text{F}$  and a  $0.01\mu\text{F}$  bypass capacitor should be connected to each  $V_{DDA}$  pin.

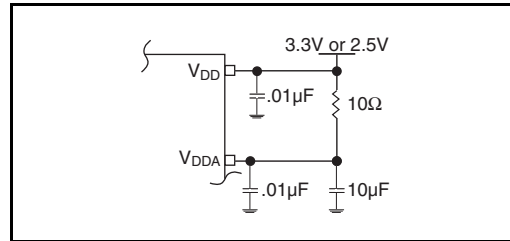


Figure 1. Power Supply Filtering

## Recommendations for Unused Input and Output Pins

### Inputs:

#### LVC MOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A  $1\text{k}\Omega$  resistor can be used.

#### REF\_CLK INPUT

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a  $1\text{k}\Omega$  resistor can be tied from the REF\_CLK to ground.

#### Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL\_IN and XTAL\_OUT can be left floating. Though not required, but for additional protection, a  $1\text{k}\Omega$  resistor can be tied from XTAL\_IN to ground.

### Outputs:

#### LVDS Outputs

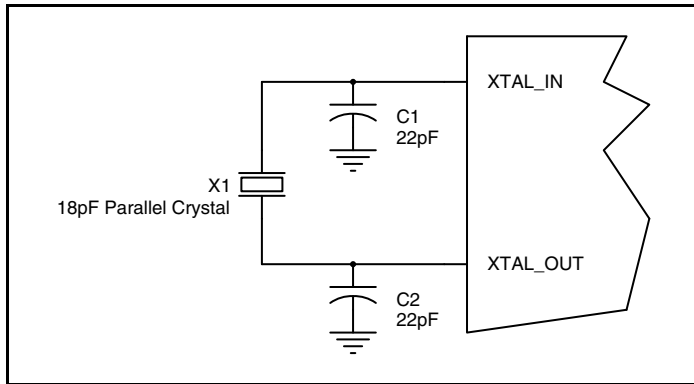
All unused LVDS output pairs can be either left floating or terminated with  $100\Omega$  across. If they are left floating, we recommend that there is no trace attached.



## Crystal Input Interface

The 844002-01 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were

determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

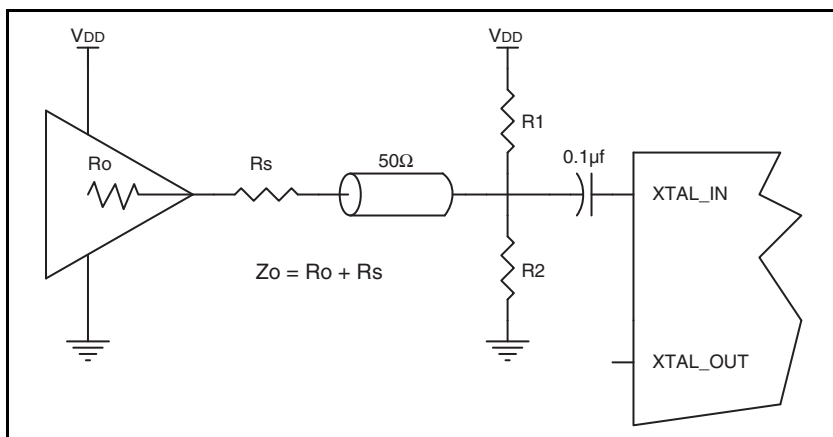


**Figure 2. Crystal Input Interface**

## LVC MOS to XTAL Interface

The XTAL\_IN input can accept a single-ended LVC MOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3*. The XTAL\_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVC MOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output

impedance of the driver ( $R_o$ ) plus the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First,  $R_1$  and  $R_2$  in parallel should equal the transmission line impedance. For most  $50\Omega$  applications,  $R_1$  and  $R_2$  can be  $100\Omega$ . This can also be accomplished by removing  $R_1$  and making  $R_2$   $50\Omega$ .

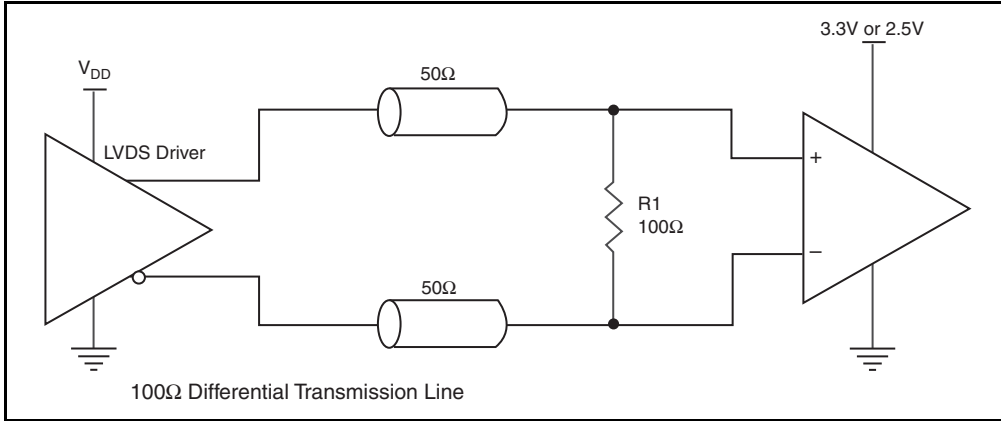


**Figure 3. General Diagram for LVC MOS Driver to XTAL Input Interface**

### 3.3V, 2.5V LVDS Driver Termination

A general LVDS interface is shown in *Figure 4*. In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple

LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.



**Figure 4. Typical LVDS Driver Termination**

## Power Considerations

This section provides information on power dissipation and junction temperature for the 844002-01. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS44002-01 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX}) = 3.465V * (105mA + 13mA) = \mathbf{408.87mW}$
- Power (outputs)<sub>MAX</sub> =  $V_{DDO\_MAX} * I_{DDO\_MAX} = 3.465V * 110mA = \mathbf{381.15mW}$

**Total Power<sub>MAX</sub> = 381.15mW + 408.87mW = 790.02mW**

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 6 below.

Therefore,  $T_j$  for an ambient temperature of 70°C with all outputs switching is:

$$70^\circ\text{C} + 0.790\text{W} * 66.6^\circ\text{C}/\text{W} = 123^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

**Table 6. Thermal Resistance  $\theta_{JA}$  for 20 Lead TSSOP, Forced Convection**

Linear Feet per Minute	$\theta_{JA}$ by Velocity		
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

## Reliability Information

Table 7.  $\theta_{JA}$  vs. Air Flow Table for a 20 Lead TSSOP

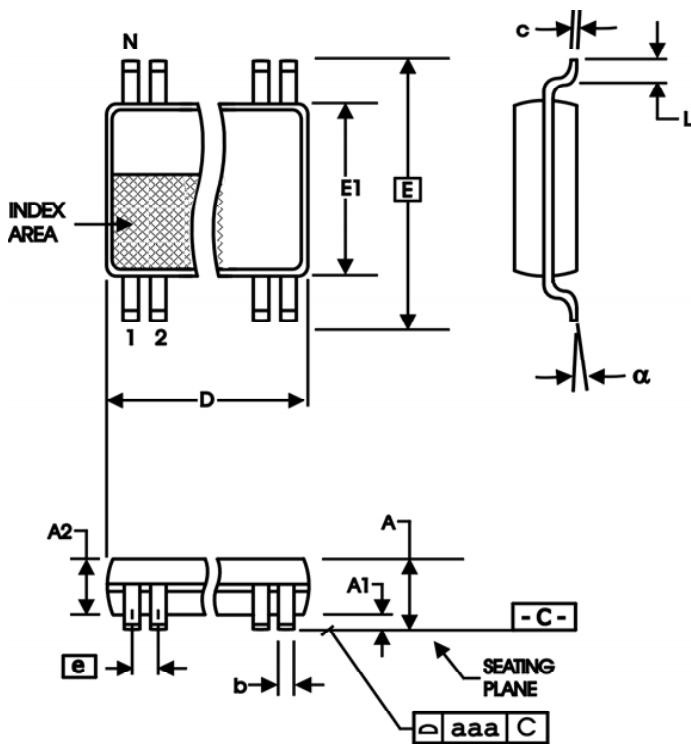
$\theta_{JA}$ by Velocity			
Linear Feet per Minute	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

## Transistor Count

The transistor count for 844002-01 is: 2914

## Package Outline and Package Dimension

Package Outline - G Suffix for 20 Lead TSSOP



All Dimensions in Millimeters		
Symbol	Minimum	Maximum
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Table 8. Package Dimensions

All Dimensions in Millimeters		
Symbol	Minimum	Maximum
N	20	
A		1.20
A1	0.05	0.15
A2	0.80	1.05

## Ordering Information

**Table 9. Ordering Information**

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
844002AG-01LF	ICS44002A01L	"Lead-Free" 20 Lead TSSOP	Tube	0°C to 70°C
844002AG-01LFT	ICS44002A01L	"Lead-Free" 20 Lead TSSOP	Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

## Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T1	1	Pin Assignment - correct pin 16 from VDD to nc.	9/28/07
		2	Pin Description Table - deleted pin 16 from VDD row. Added Pin 16 row, "nc".	
		7	Parameter Measurement Information - corrected Output Rise/Fall Time diagram.	
A	T9	13	Ordering Information - removed leaded devices. Updated data sheet format.	6/9/15



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