FemtoClock® Crystal-to-LVDS Clock Generator

ICS844252-04

DATASHEET

General Description

The ICS844252-04 is a 10Gb/12Gb Ethernet Clock Generator. The ICS844252-04 can synthesize 10 Gigabit Ethernet and 12 Gigabit Ethernet with a 25MHz crystal. It can also generate SATA and 10Gb Fibre Channel reference clock frequencies with the appropriate choice of crystals. The ICS844252-04 has excellent phase jitter performance and is packaged in a small 16-pin TSSOP, making it ideal for use in systems with limited board space.

Features

- Two differential LVDS output pairs
- Crystal input frequency range: 20MHz – 30MHz
- Output frequency range: 150MHz – 187.5MHz
- VCO range: 600MHz - 750MHz
- RMS phase jitter @ 156.25MHz (1.875MHz – 20MHz): 0.31ps (typical)
- Full 3.3V supply mode
- 0°C to 70°C ambient operating temperature
- Lead-free (RoHS 6) packaging

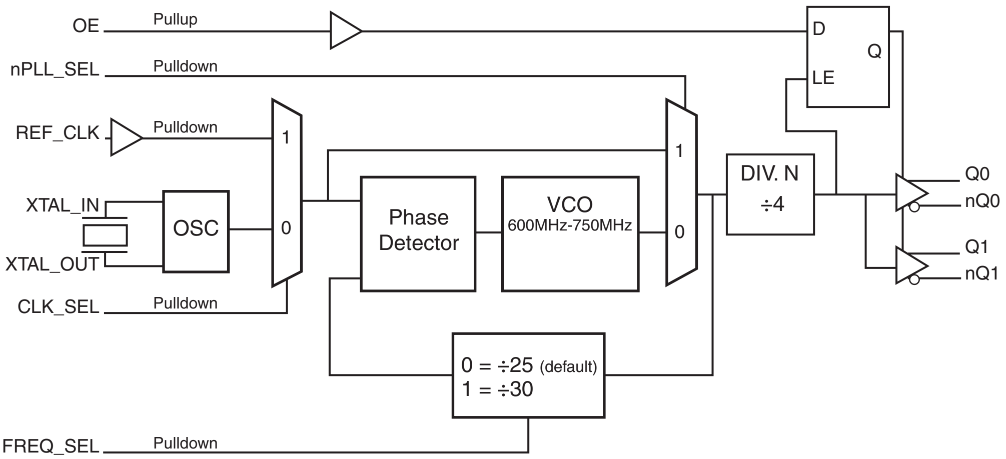
Configuration Table with 25MHz Crystal

Inputs					
Crystal Frequency (MHz)	Feedback Divide	VCO Frequency (MHz)	N Output Divide	Output Frequency (MHz)	Application
25	30	750	4	187.5	12 Gigabit Ethernet
25	25	625	4	156.25	10 Gigabit Ethernet

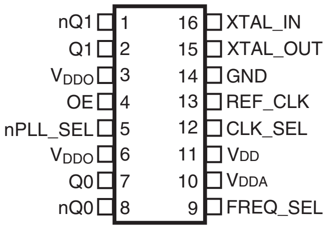
Configuration Table with Selectable Crystals

Inputs					
Crystal Frequency (MHz)	Feedback Divide	VCO Frequency (MHz)	N Output Divide	Output Frequency (MHz)	Application
20	30	600	4	150	SATA
21.25	30	637.5	4	159.375	10 Gigabit Ethernet
24	25	600	4	150	SATA
25.5	25	637.5	4	159.375	10 Gigabit Ethernet
30	25	750	4	187.5	12 Gigabit Ethernet

Block Diagram



Pin Assignment



ICS844252-04

16-Lead TSSOP
4.4mm x 5mm x 0.925mm
package body
G Package
Top View

Pin Descriptions and Characteristics

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	nQ1, Q1	Output		Differential output pair. LVDS interface levels.
3, 6	V_{DDO}	Power		Output supply pins.
4	OE	Input	Pullup	Output enable. When HIGH, clock outputs follow clock input. When LOW, Qx outputs are forced low, nQx outputs are forced high. LVCMOS/LVTTL interface levels.
5	nPLL_SEL	Input	Pulldown	When Low, selects PLL. When High, bypasses the PLL. LVCMOS/LVTTL interface levels.
7, 8	Q0, nQ0	Output		Differential output pair. LVDS interface levels.
9	FREQ_SEL	Input	Pulldown	Frequency select pin. LVCMOS/LVTTL interface levels.
10	V_{DDA}	Power		Analog supply pin.
11	V_{DD}	Power		Core supply pin.
12	CLK_SEL	Input	Pulldown	Clock select input. When Low, selects crystal inputs. When High, selects REF_CLK. LVCMOS/LVTTL interface levels.
13	REF_CLK	Input	Pulldown	Single-ended reference clock input. LVCMOS/LVTTL interface levels.
14	GND	Power		Power supply ground.
15, 16	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance	REF_CLK, OE, nPLL_SEL, CLK_SEL, FREQ_SEL		4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	**Rating**
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
XTAL_IN	0V to V_{DD}
Outputs, I_O Continuous Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	92.4°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 3A. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ to 70°C

Symbol	**Parameter**	**Test Conditions**	**Minimum**	**Typical**	**Maximum**	**Units**
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.16	3.3	V_{DD}	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				84	mA
I_{DDA}	Analog Supply Current				16	mA
I_{DDO}	Output Supply Current				52	mA

Table 3B. LVCMOS/LVTTL DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ to 70°C

Symbol	**Parameter**		**Test Conditions**	**Minimum**	**Typical**	**Maximum**	**Units**
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	nPLL_SEL, REF_CLK FREQ_SEL, CLK_SEL	$V_{DD} = V_{IN} = 3.465V$			150	µA
		OE	$V_{DD} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	nPLL_SEL, REF_CLK FREQ_SEL, CLK_SEL	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-5			µA
		OE	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-150			µA

Table 3C. LVDS DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247		485	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.125		1.45	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Table 4. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		20		30	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Capacitive Loading (CL)			12	18	pF

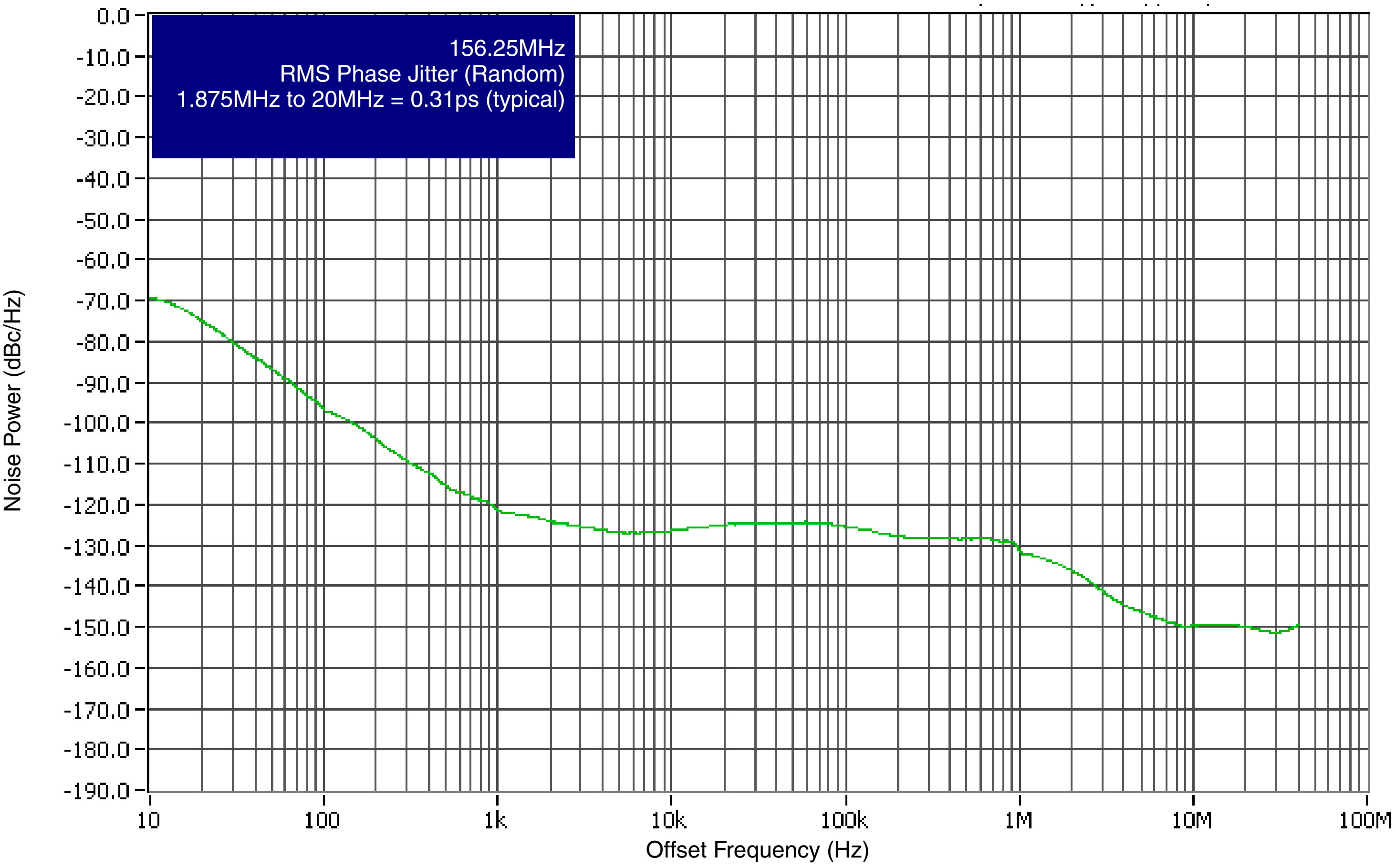
AC Electrical Characteristics

Table 5. AC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ to $70°C$

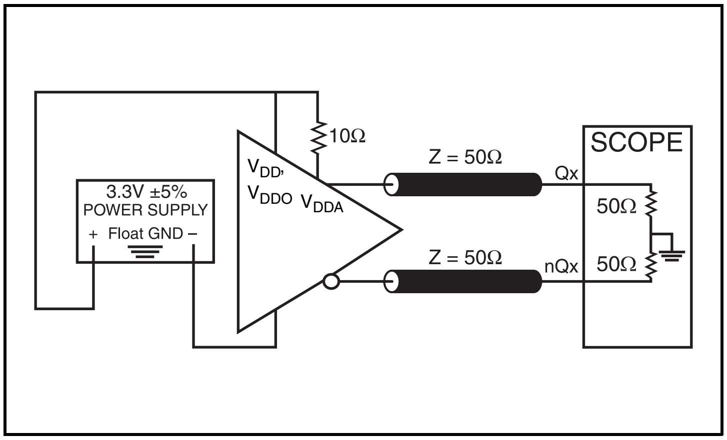
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency Range		150		187.5	MHz
*t*sk(o)	Output Skew; NOTE 1, 2				15	ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 3	156.25MHz (1.875MHz – 20MHz)		0.31		ps
		159.375MHz (1.875MHz – 20MHz):		0.31		ps
		187.5MHz (1.875MHz – 20MHz)		0.33		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	300		500	ps
odc	Output Duty Cycle	nPLL_SEL = 0	48		52	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Characterized using a crystal with CL = 18pF.
NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions.
Measured at the output differential cross points.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Refer to the Phase Noise Plots.

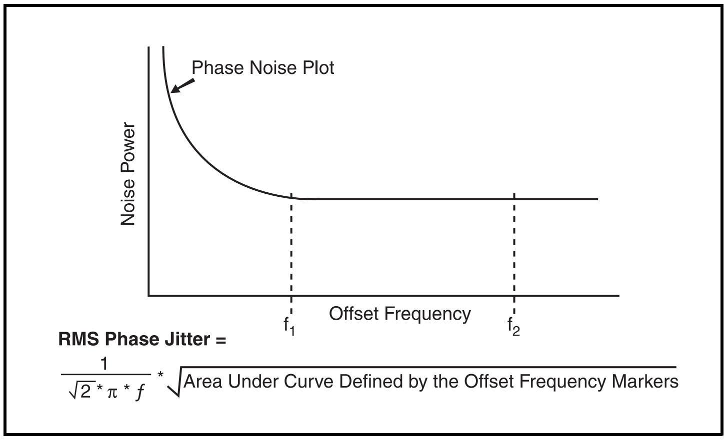
Typical Phase Noise at 156.25MHz



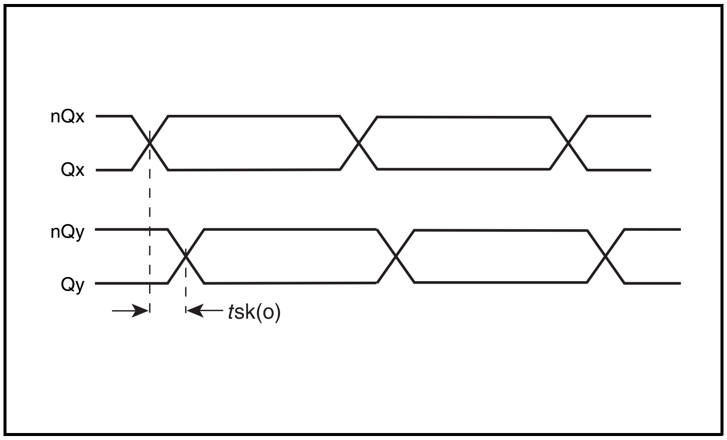
Parameter Measurement Information



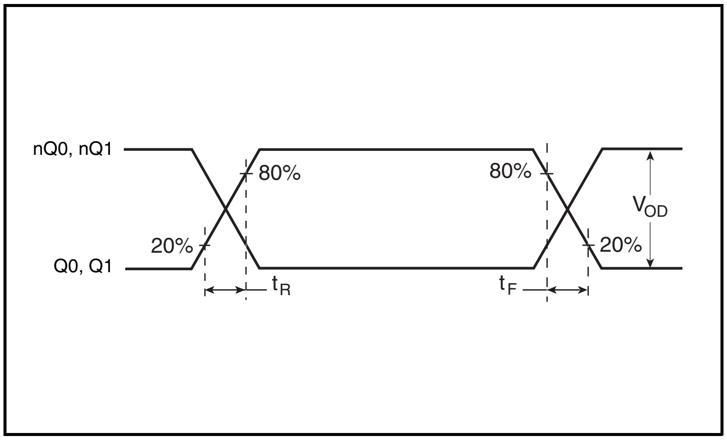
3.3V LVDS Output Load AC Test Circuit



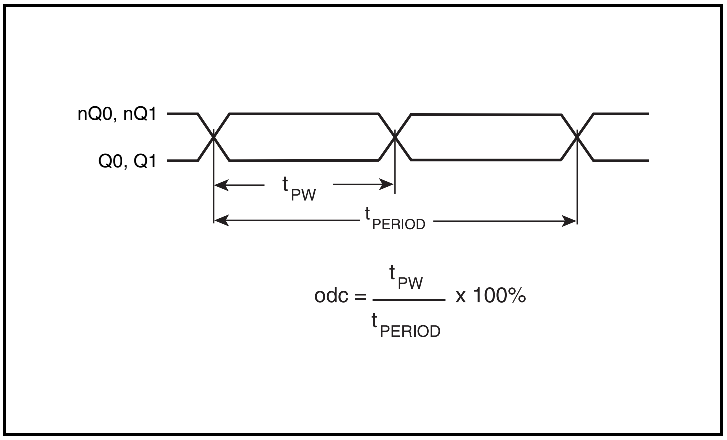
RMS Phase Jitter



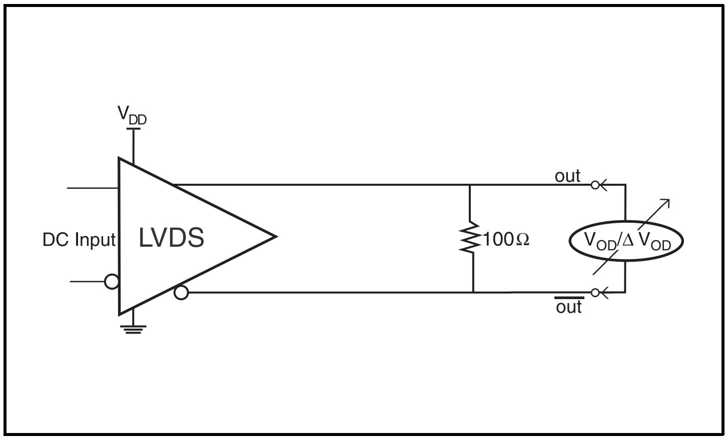
Output Skew



Output Rise/Fall Time

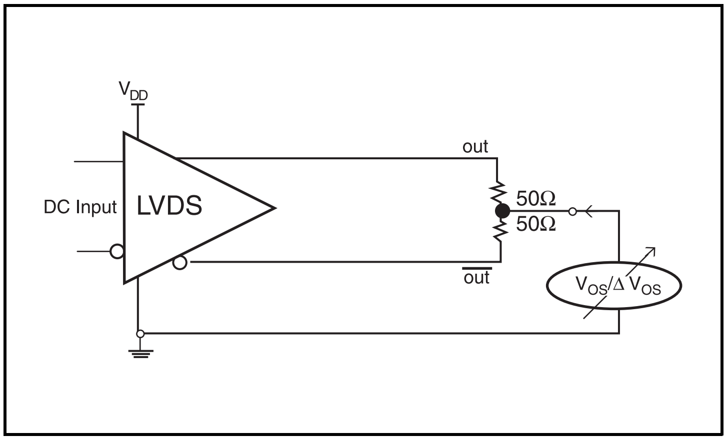


Output Duty Cycle/Pulse Width/Period



Differential Output Voltage Setup

Parameter Measurement Information, continued



Offset Voltage Setup

Application Information

Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/ns. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 3A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 3B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

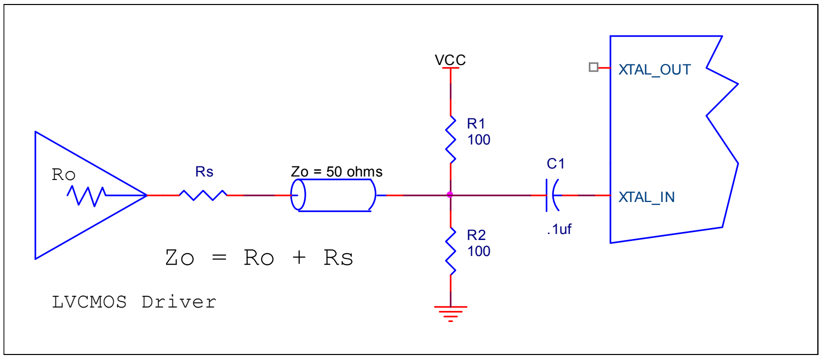


Figure 3A. General Diagram for LVCMOS Driver to XTAL Input Interface

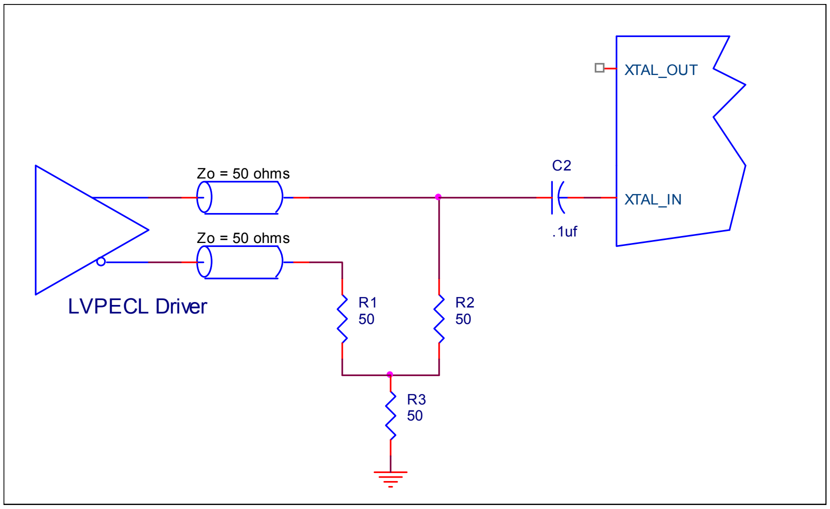


Figure 3B. General Diagram for LVPECL Driver to XTAL Input Interface

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

REF_CLK Input

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK to ground.

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 4A* can be used with either type of output structure. *Figure 4B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

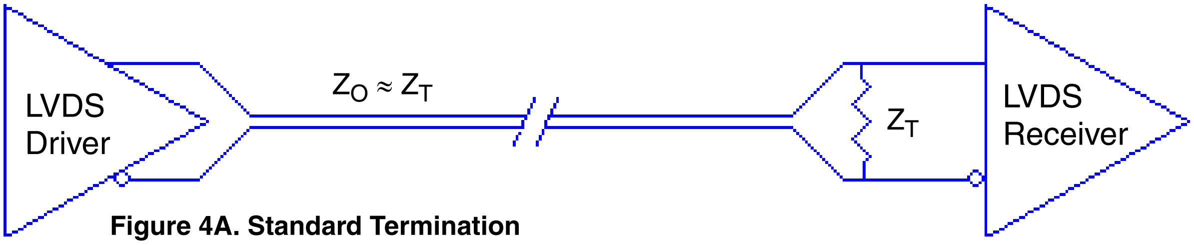


Figure 4A. Standard Termination

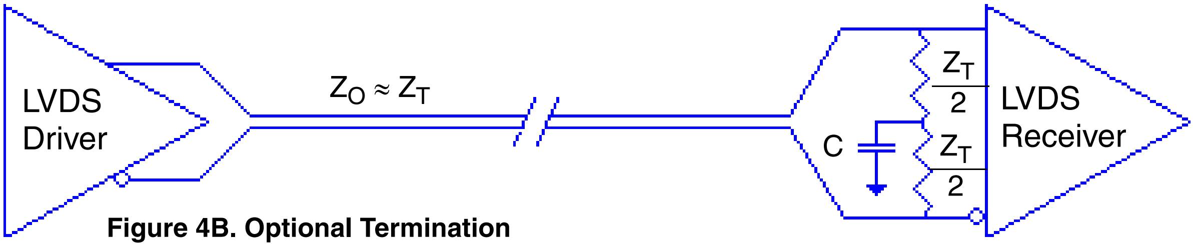


Figure 4B. Optional Termination

LVDS Termination

Schematic Example

Figure 1 shows an example of ICS844252-04 application schematic. The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set.

In this example, the device is operated VDD = V_{DDA} = V_{DDO} = 3.3V and a 12pF parallel resonant 25MHz crystal. The load capacitance C1 = C2 = 10pF are recommended for frequency accuracy. Depending on the parasitic of the printed circuit board layout, these values might require a slight adjustment to optimize the frequency accuracy. For this device, the crystal load capacitors are required for proper operation. Crystals with other load capacitance specifications can be used, but will require different values for C1 and C2.

Crystal layout is very important to minimize capacitive coupling between the crystal pads and leads and other metal in the circuit board. Capacitive coupling to other conductors has two adverse effects; it reduces the oscillator frequency leaving less tuning margin and noise coupling from power planes and logic transitions on signal traces can pull the phase of the crystal resonance, inducing jitter. Routing I^2C under the crystal is a very common layout error, based on the assumption that it is a low frequency signal and will not affect the crystal oscillation. In fact, I^2C transition times are short enough to capacitively couple into the crystal if they are routed close enough to the crystal traces.

In layout, all capacitive coupling to the crystal from any signal trace is to be minimized, that is to the XTAL_IN and XTAL_OUT pins, traces to the crystal pads, the crystal pads and the tuning capacitors. Using a crystal on the top layer as an example, void all signal and power layers under the crystal connections between the top layer and the ground plane used by the ICS844252-04. Then calculate the parasitic capacity to the ground and determine if it is large enough to preclude tuning the oscillator. If the coupling is excessive, particularly if the first layer under the crystal is a ground plane, a layout option is to void the ground plane and all deeper layers until the next ground plane is reached. The ground connection of the tuning capacitors should first be made between the capacitors on the top layer, then a single ground via is dropped to connect the tuning cap ground to the ground plane as close to the ICS844252-04 as possible as shown in the schematic.

Two LVDS terminations are shown for the outputs, one is a standard DC termination and the other is an example of an AC termination, typically used when connecting an LVDS driver to a receiver with a different logic threshold, such as CML.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS844252-04 provides separate power supplies to isolate any high switching noise from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1µf capacitor in each power pin filter should be placed on the device side. The other components can be on the opposite side of the PCB.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for wide range of noise frequency. This low-pass filter starts to attenuate noise at approximately 10 kHz. If a specific frequency noise component with high amplitude interference is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally general design practice for power plane voltage stability suggests adding bulk capacitances in the general area of all devices.

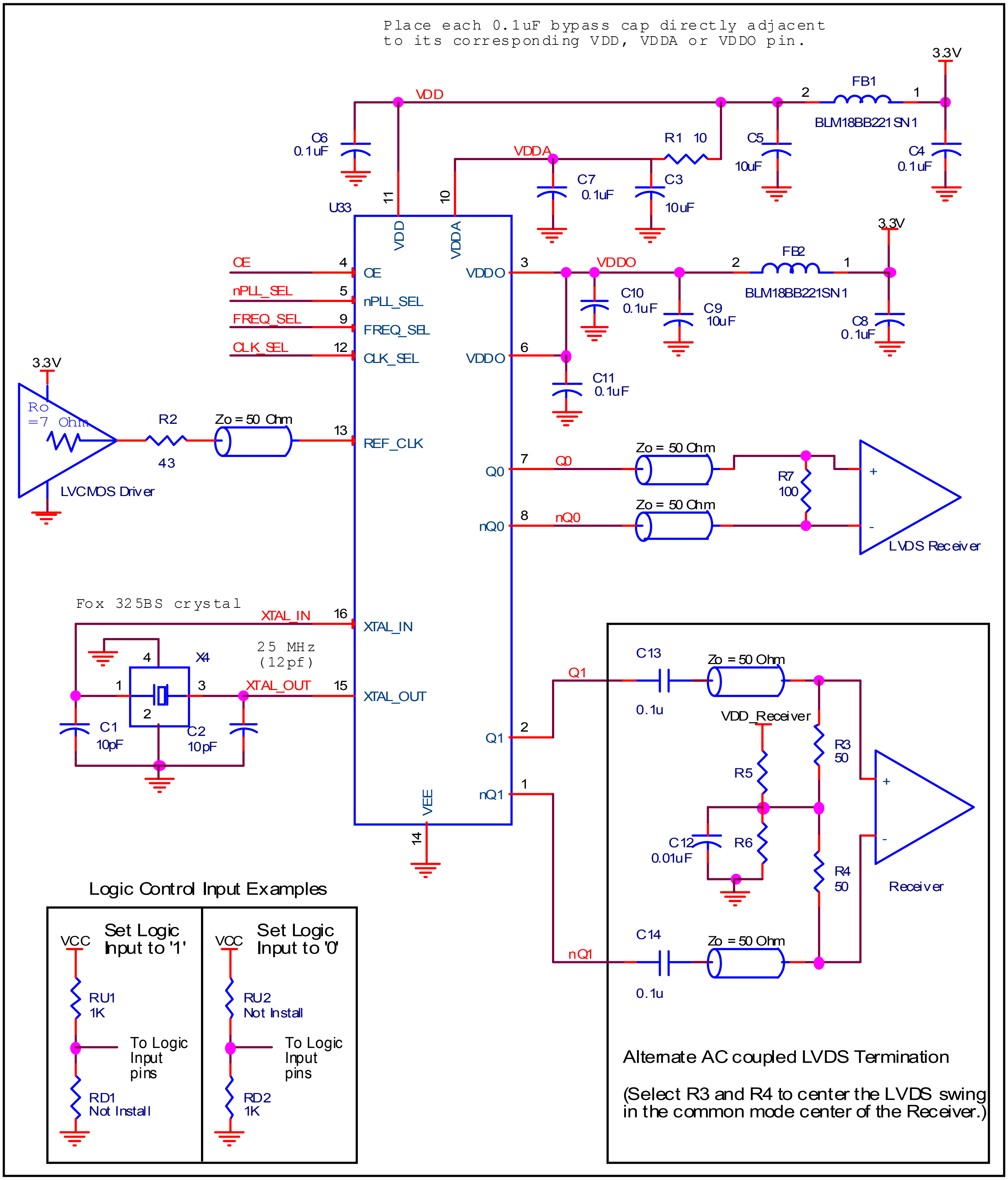


Figure 5. ICS844252-04 Schematic Layout Example

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS844252-04.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS844252-04 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for $V_{DD} = 3.3V + 5\% = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(\text{core})_{MAX} = V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX}) = 3.465V * (84mA + 16mA) =$ **346.5mW**
- Power $(\text{outputs})_{MAX} = V_{DDO\_MAX} * I_{DDO\_MAX} = 3.465V * 52mA =$ **180.18mW**

Total Power$_{\_MAX}$ = 346.5mW + 180.18mW = **526.68mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 92.4°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.527W * 92.4°C/W = 118.7°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 16 Lead TSSOP, Forced Convection

θ_{JA} **by Velocity**			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	92.4°C/W	88.0°C/W	85.9°C/W

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 16 Lead TSSOP

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	92.4°C/W	88.0°C/W	85.9°C/W

Transistor Count

The transistor count for ICS844252-04 is: 2234

Package Outline and Package Dimensions

Package Outline - G Suffix for 16 Lead TSSOP

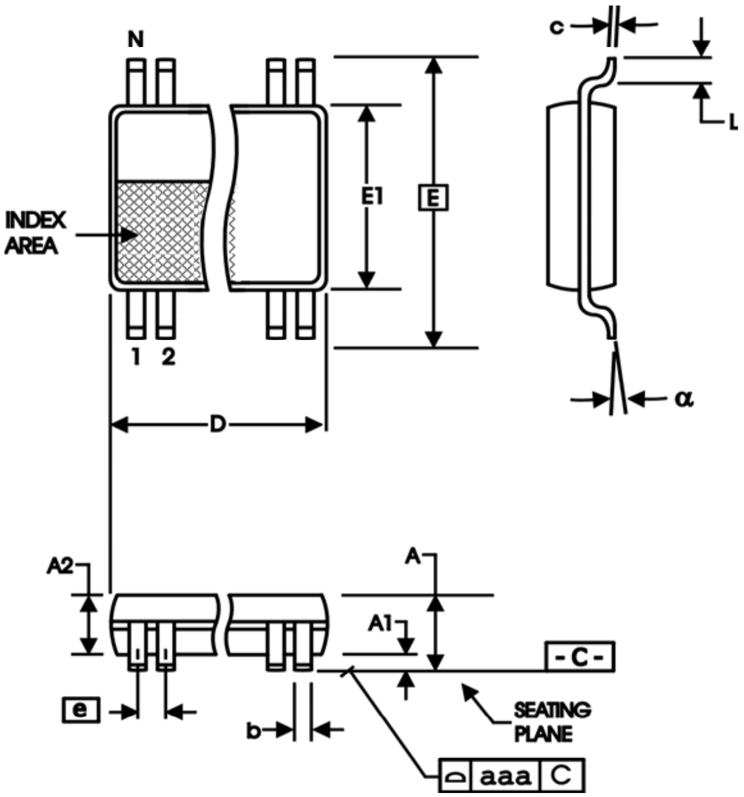


Table 8. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	16	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
844252AG-04LF	4252A04L	“Lead-Free” 16 Lead TSSOP	Tube	0°C to 70°C
844252AG-04LFT	4252A04L	“Lead-Free” 16 Lead TSSOP	Tape & Reel	0°C to 70°C

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