2:2 Differential-to-HCSL Multiplexer with Low Input Level Alarm

ICS851S201I

Datasheet

Description

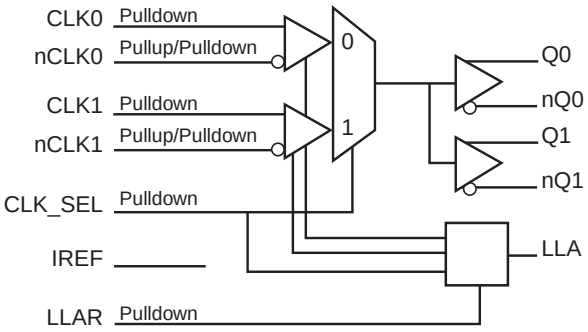
The ICS851S201I is a high-performance 2-input, 2-output Differential-to-HCSL Multiplexer. The ICS851S201I operates up to 250MHz and accepts HCSL and other low level differential inputs levels. Input level detection circuitry is available to flag input levels that drops below a specified value and on the selected input. This signal is latched until the status is reset via the alarm reset input.

The ICS851S201I is packaged in a small 3mm x 3mm 16 lead VFQFPN package, making it ideal for use on space constrained boards.

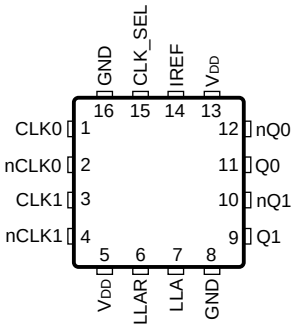
Features

- Two differential HCSL output pairs
- Two selectable differential clock input pairs
- CLKx, nCLKx pairs can accept HCSL level inputs
- Low level input detection on selected input (latched)
- Maximum Input frequency: 250MHz
- Output skew: 5ps (typical)
- Propagation delay: 1.4ns (typical)
- Additive RMS phase jitter at 133.33MHz (12kHz - 20MHz): 0.151ps (typical)
- Full 3.3V operating supply
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) packaging

Block Diagram



Pin Assignment



ICS851S201I

16-Lead VFQFPN
Top View

Pin Descriptions and Characteristics

Table 1. Pin Descriptions

Number	Name	Type		Description
1	CLK0	Input	Pulldown	Non-inverting differential HCSL clock input.
2	nCLK0	Input	Pullup/ Pulldown	Inverting differential HCSL clock input. $V_{DD}/2$ default when left floating.
3	CLK1	Input	Pulldown	Non-inverting differential HCSL clock input.
4	nCLK1	Input	Pullup/ Pulldown	Inverting differential HCSL clock input. $V_{DD}/2$ default when left floating.
5, 13	V_{DD}	Power		Positive supply pins.
6	LLAR	Input	Pulldown	Low Level Alarm Reset. When HIGH, resets LLA latch. Must be LOW to allow LLA to set. LVCMOS/LVTTL interface levels.
7	LLA	Output		Low Level Alarm. When HIGH, low level input has been detected on selected differential input (latched).
8, 16	GND	Power		Power supply ground.
9, 10	Q1, nQ1	Output		Differential output pair. HCSL interface levels.
11, 12	Q0, nQ0	Output		Differential output pair. HCSL interface levels.
14	IREF	Input		External fixed precision resistor (475Ω) from this pin to ground provides a reference current used for differential current-mode Qx, nQx clock outputs.
15	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK1, nCLK1 inputs. When LOW, selects CLK0, nCLK0 inputs. LVCMOS/LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			2		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			50		kΩ
R_{PULLUP}	Input Pullup Resistor			50		kΩ

Function Tables

Table 3A. Low Level Alarm Function Table

Valid Input Level on Selected Input	LLAR	LLA
$V_{IH} \geq 550mV$	0	LOW (default)
$V_{IH} \leq 325mV$	0	HIGH
n/a	1	Forced LOW

NOTE: Input amplitude that is <550mV and >325mV will not reliably cause the LLA output to go HIGH. Input amplitude that is <325mV will always flag the LLA output HIGH.
NOTE: Logic High, logic Low, and a differential short on the inputs will cause the LLA output to go HIGH. This feature is only available when both differential inputs are being used, and their respective frequencies are within ±50% of one another (i.e.: CLK0 is 100MHz, CLK1 must be within 50MHz to 150MHz).

Table 3B. Control Input Function Table

CLK_SEL	Input Selected
0	CLK0, nCLK0 (default)
1	CLK1, nCLK1

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	74.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V±5%; T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current	unloaded outputs			44	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V±5%; T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2.2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	LLAR, CLK_SEL	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	LLAR, CLK_SEL	V_{DD} = 3.465V, V_{IN} = 0V	-10			µA
V_{OH}	Output High Voltage	LLA; NOTE 1		2.6			V
V_{OL}	Output Low Voltage	LLA; NOTE 1				0.5	V

NOTE 1: See Parameter Measurement Information Section, *3.3V Output Load Test Circuit diagram*.

Table 4C. DC Characteristics, V_{DD} = 3.3V±5%; T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK0, CLK1, nCLK0, nCLK1	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	CLK0, CLK1	V_{DD} = 3.465V, V_{IN} = 0V	-10			µA
		nCLK0, nCLK1	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage			150		1300	mV
V_{CMR}	Common Mode Input Voltage; NOTE 1			GND – 0.5		V_{DD} – 0.85	V

NOTE 1: Common mode input voltage is defined at the cross point.

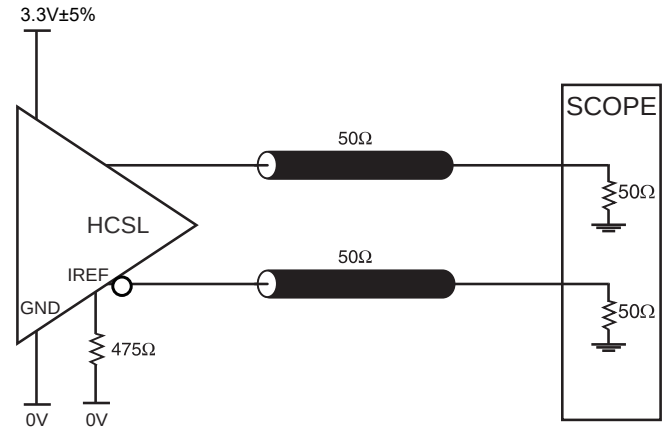
AC Electrical Characteristics

Table 5. AC Characteristics, V_{DD} = 3.3V±5%; T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				250	MHz
t_{PD}	Propagation Delay; NOTE 1		1.24	1.4	1.70	ns
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3				150	ps
tsk(o)	Output Skew, Note 2, 4			5	34	ps
tjit	Buffer Additive Phase Jitter, RMS	133.33MHz, Integration Range: 12kHz - 20MHz		0.151	0.166	ps
	Rise/Fall Edge Rate; NOTE 5, 6		1.60	2.56	3.74	V/ns
V_{MAX}	Absolute Max Output Voltage; NOTE 7, 8				1150	mV
V_{MIN}	Absolute Min Output Voltage NOTE 7, 9		-300			mV
V_{CROSS}	Absolute Crossing Voltage; NOTE 7, 10, 11		250		550	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all edges; NOTE 7, 10, 12				140	mV
odc	Output Duty Cycle		47	50	53	%
MUX_{ISOL}	MUX Isolation; NOTE 13	f_{OUT} = 100MHz	-65	-63	-62	dB

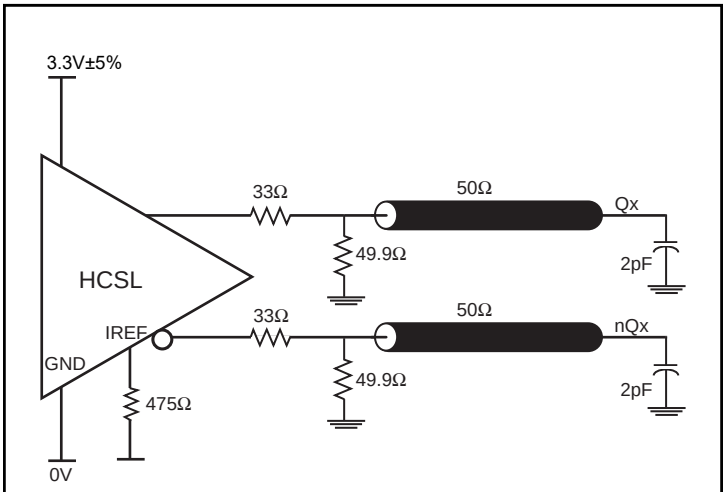
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters measured at $f \leq$ 250MHz unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at the output differential cross points.
NOTE 5: Measurement taken from differential waveform.
NOTE 6: Measured from -150mV to +150mV on the differential waveform (derived from Qx minus nQx). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing. See Parameter Measurement Information Section.
NOTE 7: Measurement taken from single ended waveform.
NOTE 8: Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.
NOTE 9: Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.
NOTE 10: Measured at crossing point where the instantaneous voltage value of the rising edge of Qx equals the falling edge of nQx. See Parameter Measurement Information Section
NOTE 11: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Parameter Measurement Information Section.
NOTE 12: Defined as the total variation of all crossing voltage of rising Qx and falling nQx. This is the maximum allowed variance in the V_{CROSS} for any particular system. See Parameter Measurement Information Section.
NOTE 13: Qx, nQx output measured differentially. See *Parameter Measurement Information* for MUX Isolation diagram.

Parameter Measurement Information

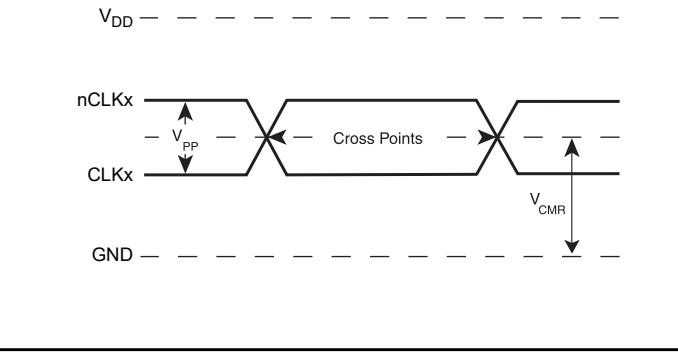


This load condition is used for $I_{DD,}$ tjit, tsk(pp), tsk(o) and t_{PD} measurements.

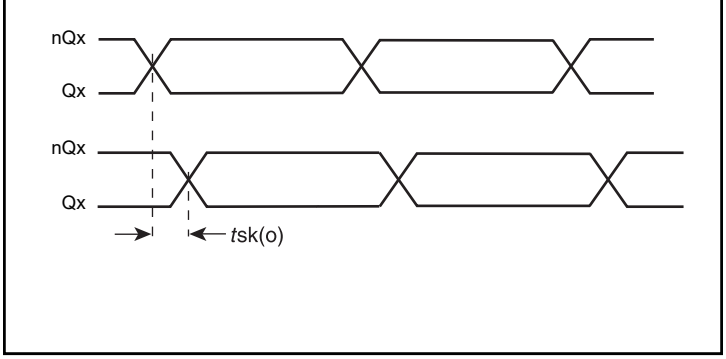
Output Load AC Test Circuit



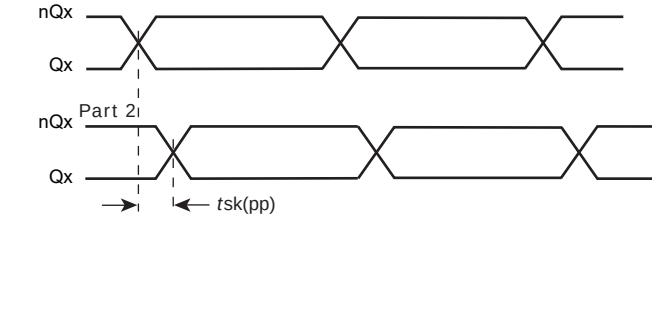
Output Load AC Test Circuit



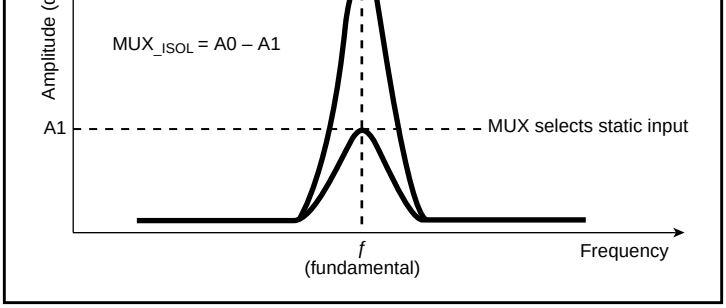
Differential Input Level



Output Skew

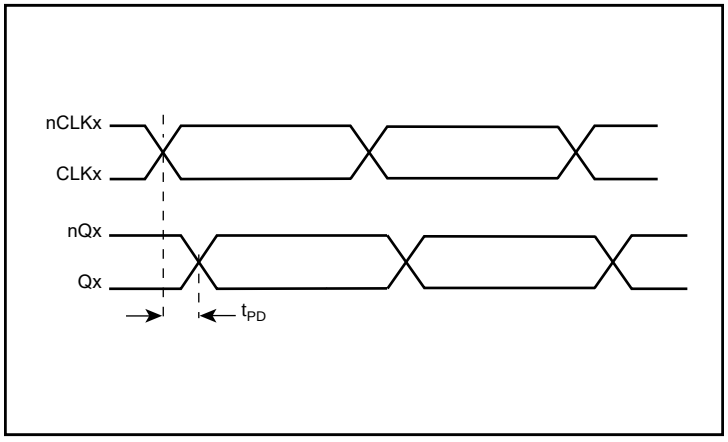


Part-to-Part Skew

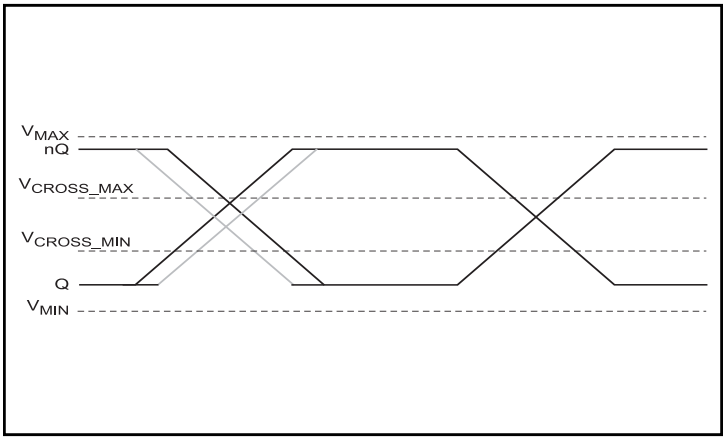


MUX Isolation

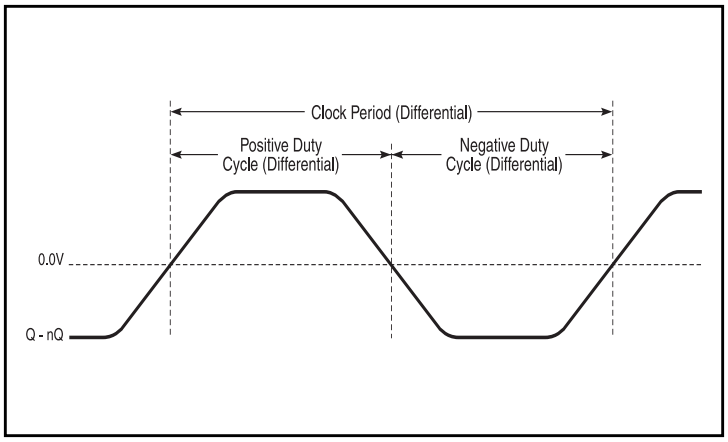
Parameter Measurement Information, continued



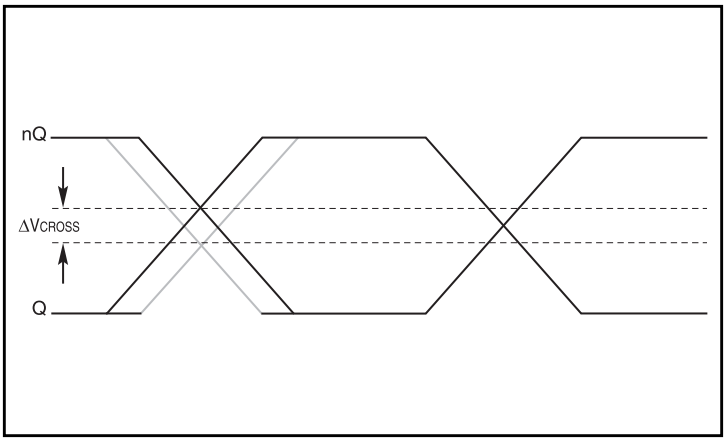
Propagation Delay



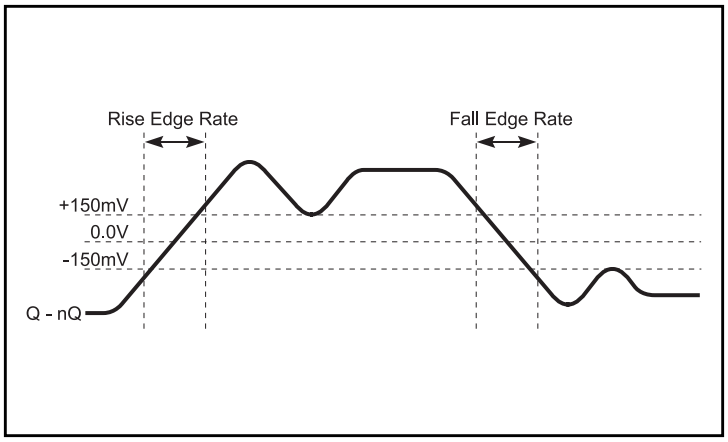
Single-ended Measurement Points for Absolute Cross Point and Swing



Differential Measurement Points for Duty Cycle/Period



Single-ended Measurement Points for Delta Cross Point



Output Rise/Fall Edge Rate

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

CLK/nCLK Inputs

For applications not requiring the use of a differential input, both the CLK and nCLK pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

LVCMOS Control Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

Differential Outputs

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Differential Clock Input Interface

The CLK /nCLK accepts HCSL and other differential signals. Both differential signals must meet the V_{PP} and V_{CMR} input requirements. *Figure 2* shows interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements.

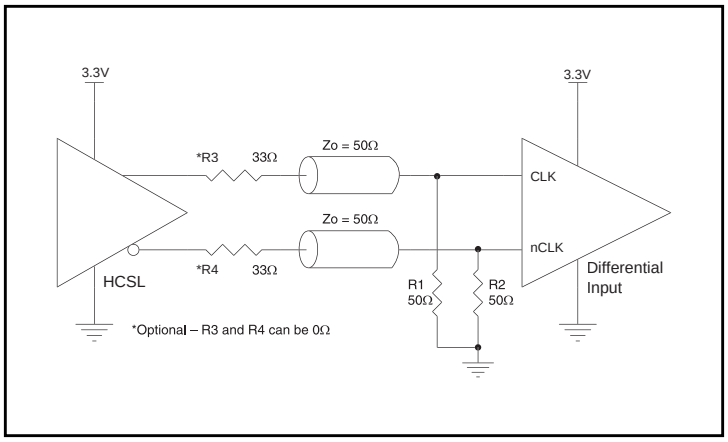


Figure 2. CLK/nCLK Input Driven by a 3.3V HCSL Driver

VFQFPN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 3.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

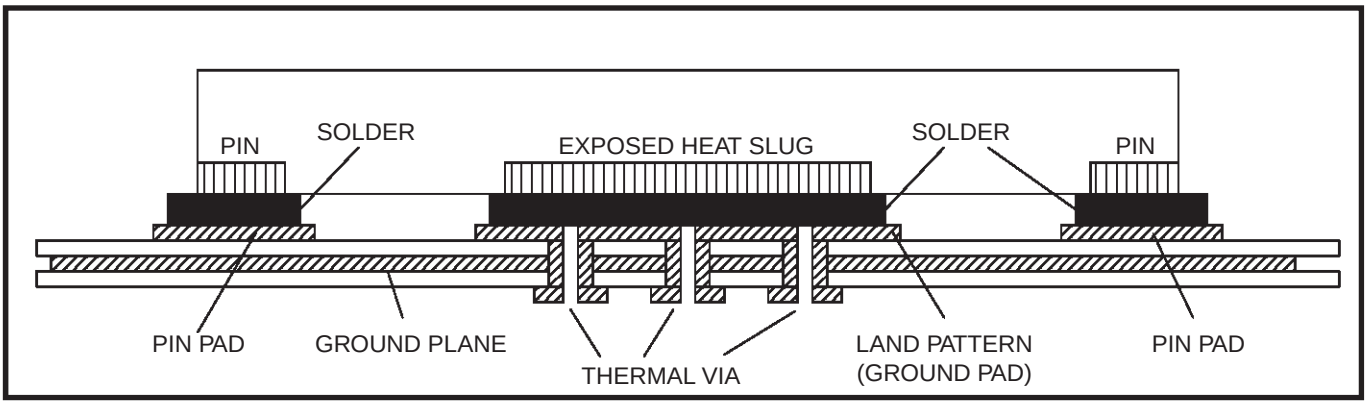


Figure 3. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Recommended Termination

Figure 4A is the recommended source termination for applications where the driver and receiver will be on a separate PCBs. This termination is the standard for PCI Express™ and HCSL output types. All traces should be 50Ω impedance single-ended or 100Ω differential.

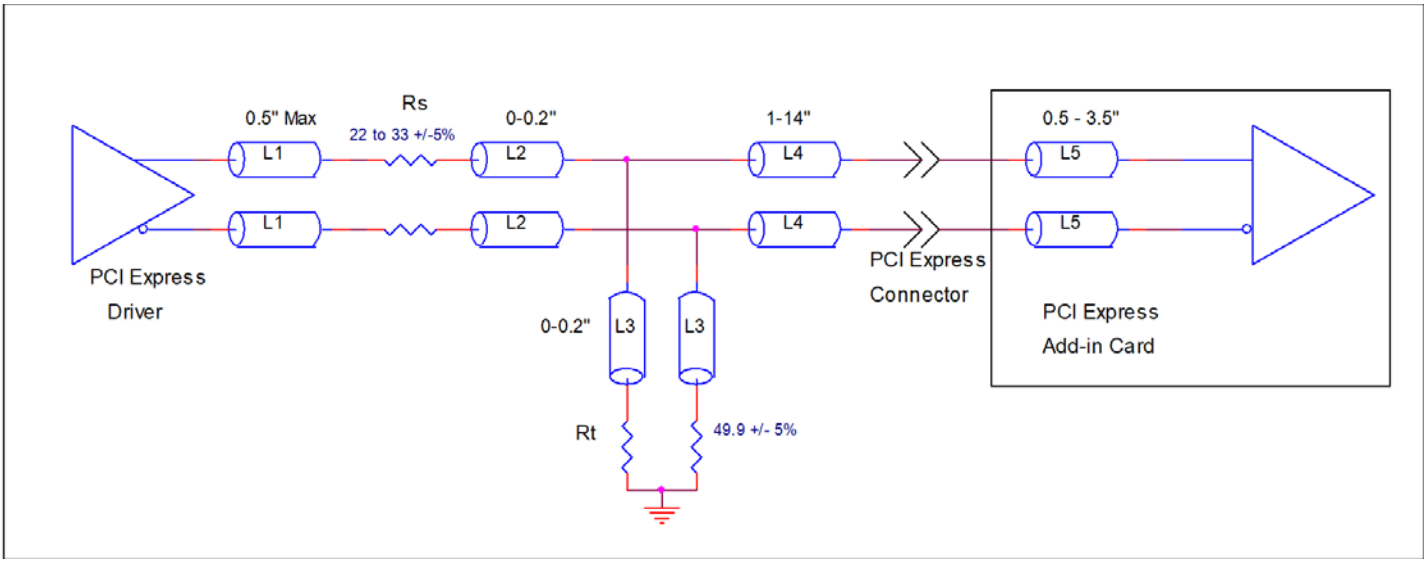


Figure 4A. Recommended Source Termination (where the driver and receiver will be on separate PCBs)

Figure 4B is the recommended termination for applications where a point-to-point connection can be used. A point-to-point connection contains both the driver and the receiver on the same PCB. With a matched termination at the receiver, transmission-line reflections will be minimized. In addition, a series resistor (Rs) at the driver offers flexibility and can help dampen unwanted reflections. The optional resistor can range from 0Ω to 33Ω. All traces should be 50Ω impedance single-ended or 100Ω differential.

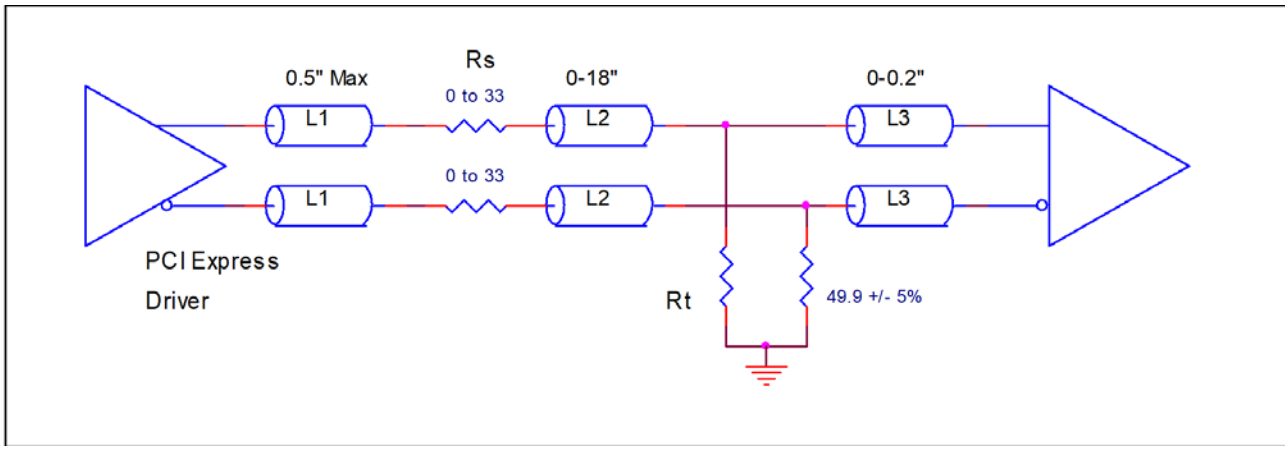


Figure 4B. Recommended Termination (where a point-to-point connection can be used)

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS851S201I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS851S201I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

The maximum current at 85°C is as follows:
I_{DD_MAX} = 37mA

- Power $(core)_{MAX} = V_{DD\_MAX} * I_{DD}$ = 3.465V * 44mA = **152.46mW**
- Power $(HCSL)_{MAX}$ = 2 * 44.5mW = 89mW

Total Power$_{MAX}$ = 152.46mW + 89mW = **241.46mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 74.7°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.242W * 74.7°C/W = 103°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 16 Lead VFQFPN, Forced Convection

θ_{JA} **vs. Air Flow**			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

3. Calculations and Equations.

The purpose of this section is to calculate power dissipation on the IC per HCSL output pair.

HCSL output driver circuit and termination are shown in *Figure 6.*

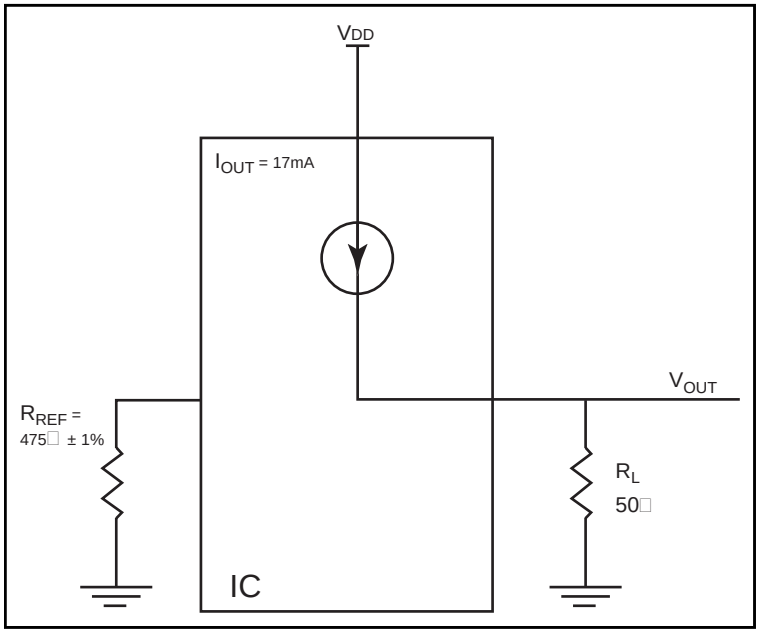


Figure 6. HCSL Driver Circuit and Termination

HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs when V_{DD_MAX}.

Power = $(V_{DD\_MAX} - V_{OUT}) * I_{OUT}$
since $V_{OUT} = I_{OUT} * R_L$

Power = $(V_{DD\_MAX} - I_{OUT} * R_L) * I_{OUT}$

= (3.465V – 17mA * 50Ω) * 17mA

Total Power Dissipation per output pair = **44.5mW**

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 16 Lead VFQFPN

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

Transistor Count

The transistor count for ICS851S201I is: 713

Package Outline Drawings

The package outline drawings are located at the end of this document. The package information is the most current data available and is subject to change without notice or revision of this document.

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
851S201CKILF	1CIL	“Lead-Free” 16 Lead VFQFPN	Tube	-40°C to 85°C
851S201CKILFT	1CIL	“Lead-Free” 16 Lead VFQFPN	Tape & Reel	-40°C to 85°C

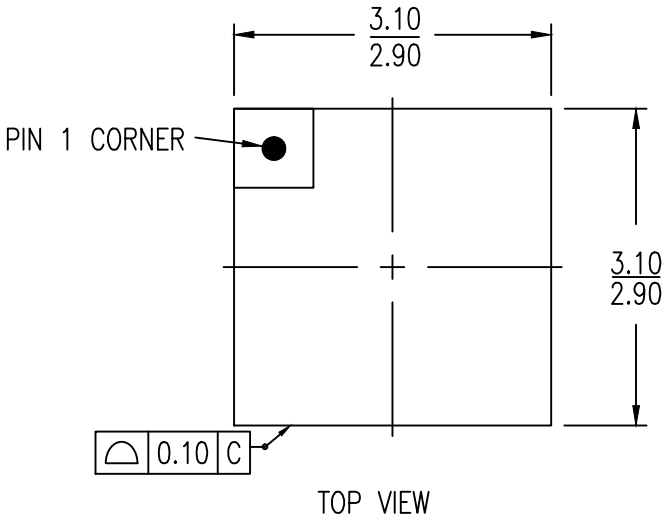
Revision History

Revision Date	Description of Change
February 1, 2018	Changed all references to 2:1 to 2:2 (input/output) Changed all package references to VFQFN to VFQFPN Updated the package outline drawings; however, no technical changes
May 27, 2017	Updated the package outline drawings.
September 6, 2013	AMR -- Supply Voltage, V_{DD} = 4.6V. T4B -- Note 1: Deleted 'Outputs terminated with 50Ω to VDD/2. T5 -- Output Duty Cycle: 47%(Min), 53%(Max). T5 -- MUX_{ISOL}: -65dB (Min)

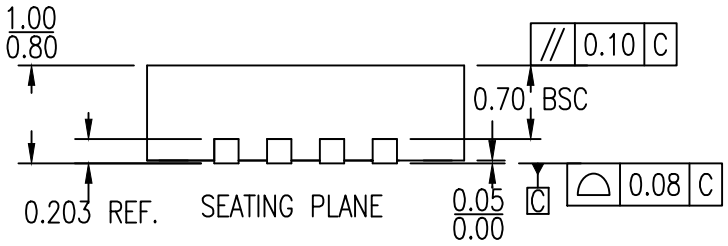
16-VFQFPN Package Outline Drawing

3.0 x 3.0 x 0.9 mm, 0.5mm Pitch, 1.70 x 1.70 mm Epad

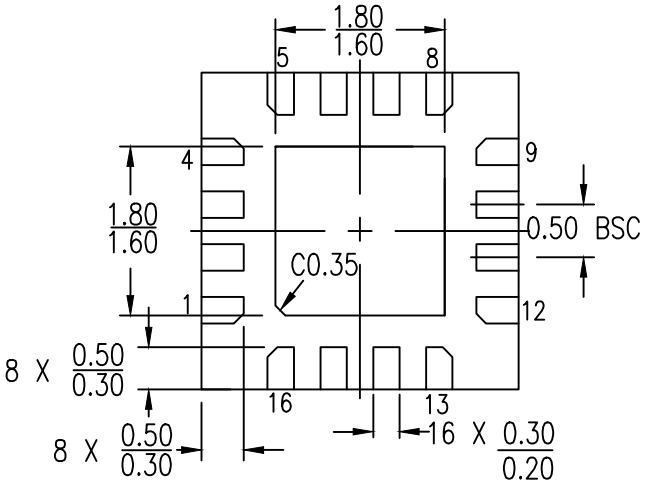
NL/NLG16P2, PSC-4169-02, Rev 05, Page 1



TOP VIEW

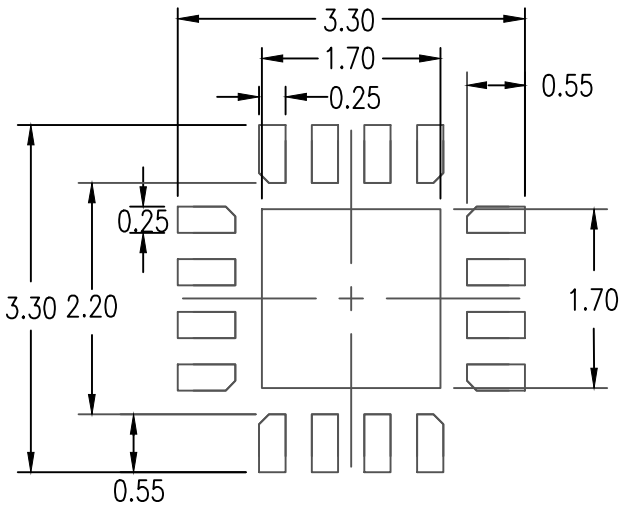


SIDE VIEW



BOTTOM VIEW

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES



RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES
2. TOP DOWN VIEW–AS VIEWED ON PCB
3. LAND PATTERN RECOMMENDATION IS PER IPC–7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN

Package Revision History		
Date Created	Rev No.	Description
Oct 25, 2017	Rev 04	Remove Bookmak at Pdf Format & Update Thickness Tolerance
Jan 18, 2018	Rev 05	Change QFN to VFQFPN

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