Dual LVCMOS / LVTTL-to-Differential HSTL Translator

85222-01

DATASHEET

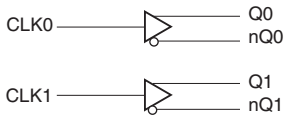
General Description

The 85222-01 is a Dual LVCMOS / LVTTL-to-Differential HSTL translator. The 85222-01 has two single ended clock inputs. The single ended clock input accepts LVCMOS or LVTTL input levels and translates them to HSTL levels. The small outline 8-pin SOIC package makes this device ideal for applications where space, high performance and low power are important.

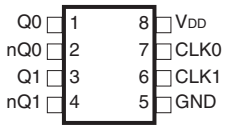
Features

- Two differential HSTL outputs
- CLK0, CLK1 LVCMOS/LVTTL clock inputs
- CLK0 and CLK1 can accept the following input levels: LVCMOS or LVTTL
- Maximum output frequency: 350MHz
- Part-to-part skew: 375ps (maximum)
- Propagation delay: 1075ps (maximum)
- V_{OH}: 1.4V (maximum)
- Full 3.3V and 2.5V operating supply voltage
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request
- Available in lead-free RoHS-compliant package

Block Diagram



Pin Assignment



85222-01
8-Lead SOIC
3.90mm x 4.92mm x 1.37mm body package
M Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	Q0, nQ0	Output		Differential output pair. HSTL interface levels.
3, 4	Q1, nQ1	Output		Differential output pair. HSTL interface levels.
5	GND	Power		Power supply ground.
6	CLK1	Input	Pullup	LVCMOS / LVTTL clock input.
7	CLK0	Input	Pullup	LVCMOS / LVTTL clock input.
8	V_{DD}	Power		Positive supply pin.

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.
NOTE: Unused output pairs must be terminated.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	112.7°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 3A. Power Supply DC Characteristics, V_{DD} = 3.3V±5% or V_{DD} = 2.5V±5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DD}	Positive Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				35	mA

Table 3B. LVCMOS / LVTTL DC Characteristics, V_{DD} = 3.3V±5% or V_{DD} = 2.5V±5%, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	CLK0, CLK1		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	CLK0, CLK1		-0.3		1.3	V
I_{IH}	Input High Current	CLK0, CLK1	$V_{DD} = V_{IN}$ = 3.465V			5	µA
			$V_{DD} = V_{IN}$ = 2.625V				
I_{IL}	Input Low Current	CLK0, CLK1	V_{DD} = 3.465, V_{IN} = 0V	-150			µA
			V_{DD} = 2.625, V_{IN} = 0V				

Table 3C. HSTL DC Characteristics, V_{DD} = 3.3V±5% or V_{DD} = 2.5V±5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		1		1.4	V
V_{OL}	Output Low Voltage; NOTE 1	V_{DD} = 3.3V±5%	0		0.4	V
		V_{DD} = 2.5V±5%	0		0.55	V
V_{SWING}	Peak-to-Peak Output Voltage Swing	V_{DD} = 3.3V±5%	0.6		1.4	V
		V_{DD} = 2.5V±5%	0.45		1.4	V

NOTE 1: Outputs terminated with 50Ω to GND.

TABLE 4A. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				350	MHz
t_{PD}	Propagation Delay; NOTE 1		700		1075	ps
tsk(pp)	Part-to-Part Skew; NOTE 2, 3				375	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	150		800	ps
odc	Output Duty Cycle	$f \leq 150$MHz	48		52	%
		150 < $f \leq 250$MHz	46		54	%
		250 < $f \leq 350$MHz	45		55	%

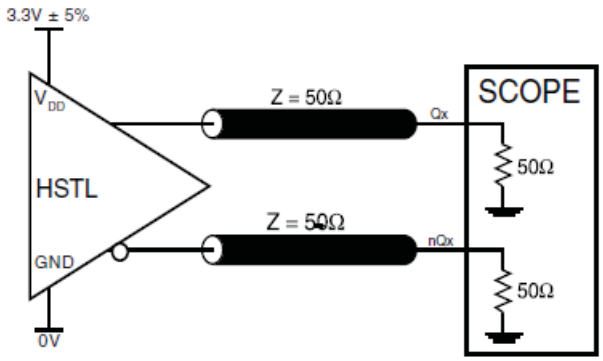
NOTE 1: Measured from V_{DD}/2 of the input to the differential output crossing point.
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 4B. AC CHARACTERISTICS, V_{DD} = 2.5V±5%, T_A = 0°C TO 70°C

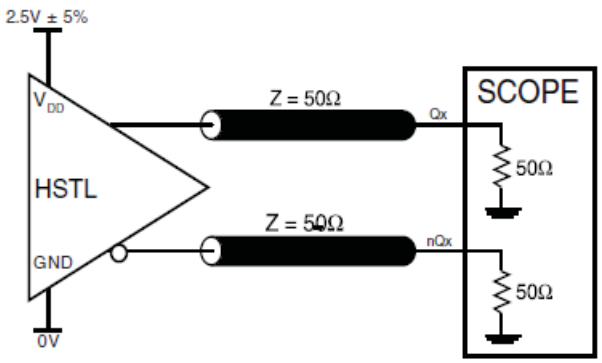
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				350	MHz
t_{PD}	Propagation Delay; NOTE 1		700		1200	ps
tsk(pp)	Part-to-Part Skew; NOTE 2, 3				475	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	150		800	ps
odc	Output Duty Cycle	$f \leq 150$MHz	48		52	%
		150 < $f \leq 350$MHz	46		54	%

NOTE 1: Measured from V_{DD}/2 of the input to the differential output crossing point.
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

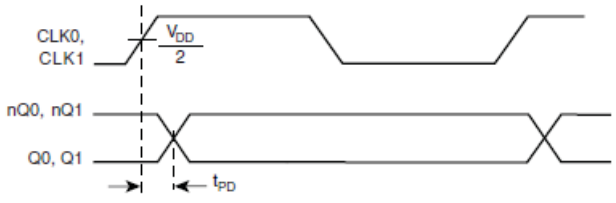
Parameter Measurement Information



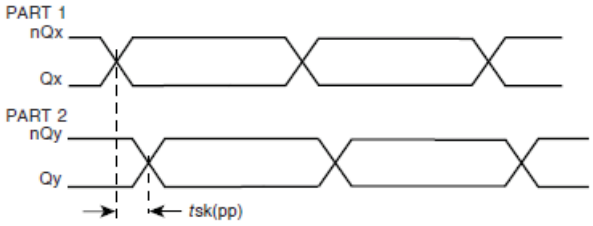
3.3V Core/3.3V Output Load AC Test Circuit



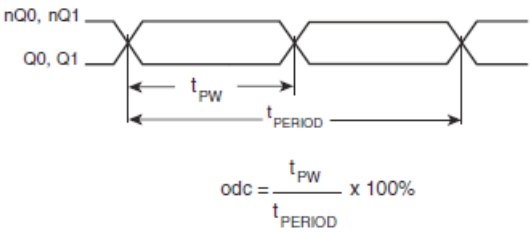
2.5V Core/2.5V Output Load AC Test Circuit



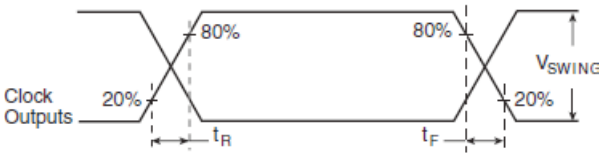
Propagation Delay



Part-to-Part Skew



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

Application Information

Wiring the Differential Input to Accept Single Ended Levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{CC} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

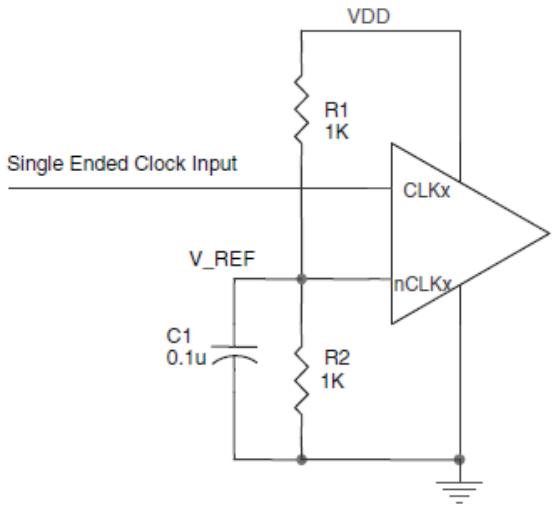


Figure 1. Single Ended Signal Driving Differential Input

Recommendations for Unused Input and Output Pins

Inputs:

CLK Input:

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

Outputs:

HSTL Output

All unused LVHSTL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Schematic Example

Figure 2 shows a schematic example of 85222-01. In this example, the inputs are driven by 7Ω output LVCMOS drivers with series terminations. The decoupling capacitors should be physically located near the power pin. For 85222-01, the unused output need to be terminated.

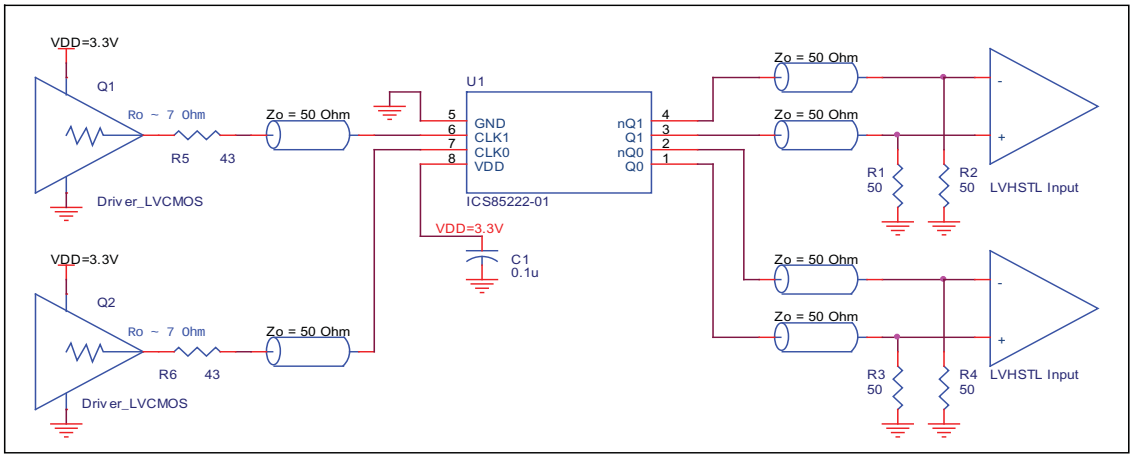


Figure 2. 85222-01 HSTL Buffer Schematic Example

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 85222-01.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the 85222-01 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{DD\_MAX} * I_{DD\_MAX}$ = 3.465V * 35mA = **121.3mW**
- Power $(outputs)_{MAX}$ = **82.34mW/Loaded Output pair**
  If all outputs are loaded, the total power is 2 * 82.34mW = **164.68mW**

Total Power $_{MAX}$ (3.465V, with all outputs switching) = 121.3mW + 164.68mW = **285.98mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for the devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total device power dissipation (example calculation is in Section 1 above)
T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 103.3°C/W per Table 5 below. Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.286W * 103.3°C/W = 99.5°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 5. THERMAL RESISTANCE θ_{JA} FOR 8-PIN SOIC, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

HSTL output driver circuit and termination are shown in *Figure 3.*

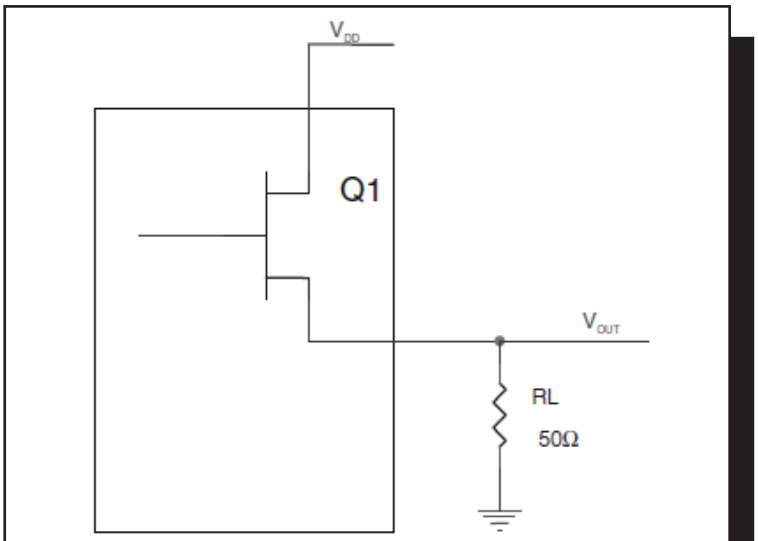


FIGURE 3. HSTL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load.

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = (V_{OH\_MAX}/R_L) * (V_{DD\_MAX} - V_{OH\_MAX})$

$Pd\_L = (V_{OL\_MAX}/R_L) * (V_{DD\_MAX} - V_{OL\_MAX})$

Pd_H = (1.4V/50Ω) * (3.465V - 1.4V) = **57.82mW**
Pd_L = (0.4V/50Ω) * (3.465V - 0.4V) = **24.52mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **82.34mW**

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE 8 LEAD SOIC

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for 85222-01 is: 443

Package Outline - M Suffix for 8 Lead SOIC

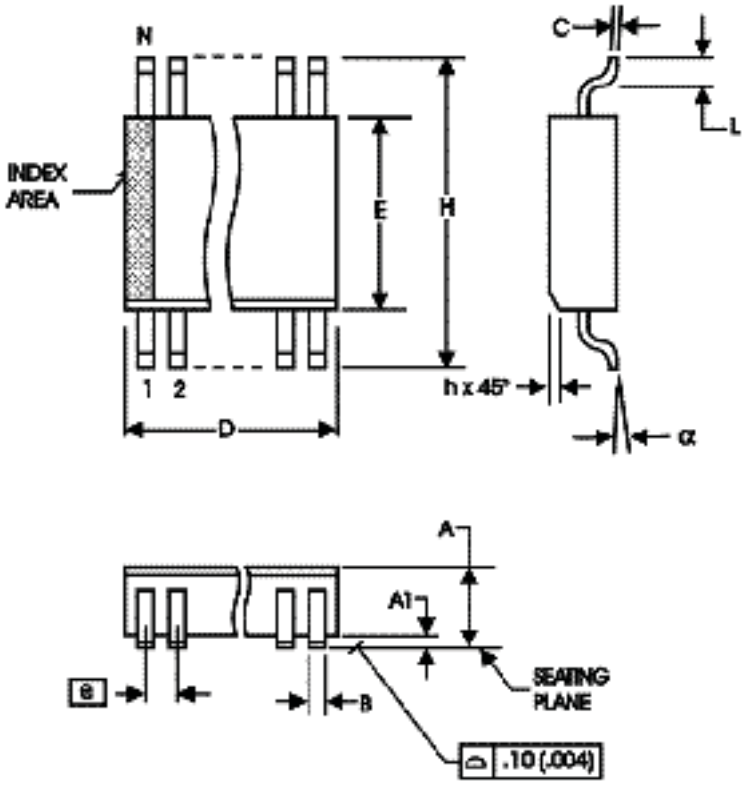


Table 7. Package Dimensions

SYMBOL	Millimeters	
	MINIMUM	MAXIMUM
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BASIC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
85222AM-01LF	5222A01L	8 Lead “Lead-Free” SOIC	tube	0°C to 70°C
85222AM-01LFT	5222A01L	8 Lead “Lead-Free” SOIC	tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	T8	6 11	Added Application Note, “Wiring the Differential Input to Accept Single Ended Levels”. Ordering Information Table - added Lead-Free part number.	1/11/05
A	T8	1 6 8-9 12	Added lead-free bullet. Added Recommendations for Unused Input and Output Pins. Corrected Power Considerations, Power Dissipation calculation. Ordering Information Table - added tape & reel quantity and lead-free note.	11/15/05
A	T8	12 14	Updated datasheet’s header/footer with IDT from ICS. Removed ICS prefix from Part/Order Number column. Added Contact Page.	8/4/10
A	T8	12	Product Discontinuation Notice - PDN CQ-15-03. Ordering Information - removed leaded devices.	5/7/15

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