DATASHEET

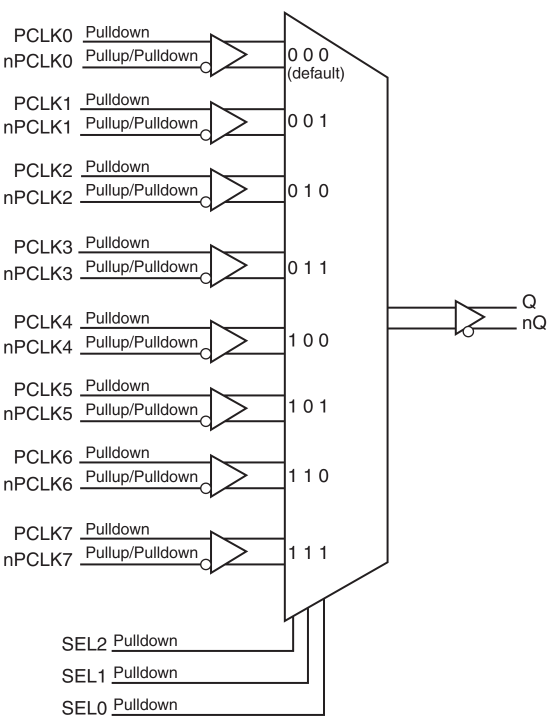
General Description

The ICS854S058I is an 8:1 Differential-to-LVDS Clock Multiplexer which can operate up to 2.5GHz. The ICS854S058I has 8 selectable differential clock inputs. The PCLK, nPCLK input pairs can accept LVPECL, LVDS, SSTL or CML levels. The fully differential architecture and low propagation delay make it ideal for use in clock distribution circuits. The select pins have internal pulldown resistors. The SEL2 pin is the most significant bit and the binary number applied to the select pins will select the same numbered data input (i.e., 000 selects PCLK0, nPCLK0).

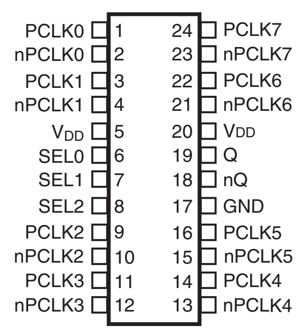
Features

- High speed 8:1 differential multiplexer
- One differential LVDS output pair
- Eight selectable differential PCLK, nPCLK input pairs
- PCLKx, nPCLKx pairs can accept the following differential input levels: LVPECL, LVDS, SSTL, CML
- Maximum output frequency: 2.5GHz
- Translates any single ended input signal to LVDS levels with resistor bias on nPCLKx input
- Additive phase jitter, RMS: 0.065ps (typical)
- Part-to-part skew: 300ps (maximum)
- Propagation delay: 600ps (maximum)
- Supply voltage range: 3.135V to 3.465V
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) packaging

Block Diagram



Pin Assignment



ICS854S058I
24-Lead TSSOP, 173-MIL
7.8mm x 4.4mm x 0.925mm package body

G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1	PCLK0	Input	Pulldown	Non-inverting differential LVPECL clock input.
2	nPCLK0	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. $V_{DD}/2$ default when left floating.
3	PCLK1	Input	Pulldown	Non-inverting differential LVPECL clock input.
4	nPCLK1	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. $V_{DD}/2$ default when left floating.
5, 20	V_{DD}	Power		Positive supply pins.
6, 7, 8	SEL0, SEL1, SEL2	Input	Pulldown	Clock select input pins. LVCMOS/LVTTL interface levels.
9	PCLK2	Input	Pulldown	Non-inverting differential LVPECL clock input.
10	nPCLK2	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. $V_{DD}/2$ default when left floating.
11	PCLK3	Input	Pulldown	Non-inverting differential LVPECL clock input.
12	nPCLK3	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. $V_{DD}/2$ default when left floating.
13	nPCLK4	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. $V_{DD}/2$ default when left floating.
14	PCLK4	Input	Pulldown	Non-inverting differential LVPECL clock input.
15	nPCLK5	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. $V_{DD}/2$ default when left floating.
16	PCLK5	Input	Pulldown	Non-inverting differential LVPECL clock input.
17	GND	Power		Power supply ground.
18, 19	nQ, Q	Output		Differential output pair. LVDS interface levels.
21	nPCLK6	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. $V_{DD}/2$ default when left floating.
22	PCLK6	Input	Pulldown	Non-inverting differential LVPECL clock input.
23	nPCLK7	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. $V_{DD}/2$ default when left floating.
24	PCLK7	Input	Pulldown	Non-inverting differential LVPECL clock input.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			2		pF
$R_{PULLDOWN}$	Pulldown Resistor			75		kΩ
$R_{VDD}/2$	RPullup/Pulldown Resistor			50		kΩ

Table 3. Clock Input Function Table

Inputs			Outputs	
SEL2	SEL1	SEL0	Q	nQ
0 (default)	0	0	PCLK0	nPCLK0
0	0	1	PCLK1	nPCLK1
0	1	0	PCLK2	nPCLK2
0	1	1	PCLK3	nPCLK3
1	0	0	PCLK4	nPCLK4
1	0	1	PCLK5	nPCLK5
1	1	0	PCLK6	nPCLK6
1	1	1	PCLK7	nPCLK7

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O Continuous Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	85.1°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				66	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2.2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	SEL[0:2]	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	SEL[0:2]	V_{DD} = 3.465V, V_{IN} = 0V	-10			µA

Table 4C. LVPECL Differential DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK[0:7], nPCLK[0:7]	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	PCLK[0:7]	V_{DD} = 3.465V, V_{IN} = 0V	-10			µA
		nPCLK[0:7]	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			0.15		1.2	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 1.2		V_{DD}	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.

Table 4D. LVDS DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247		454	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.125		1.375	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

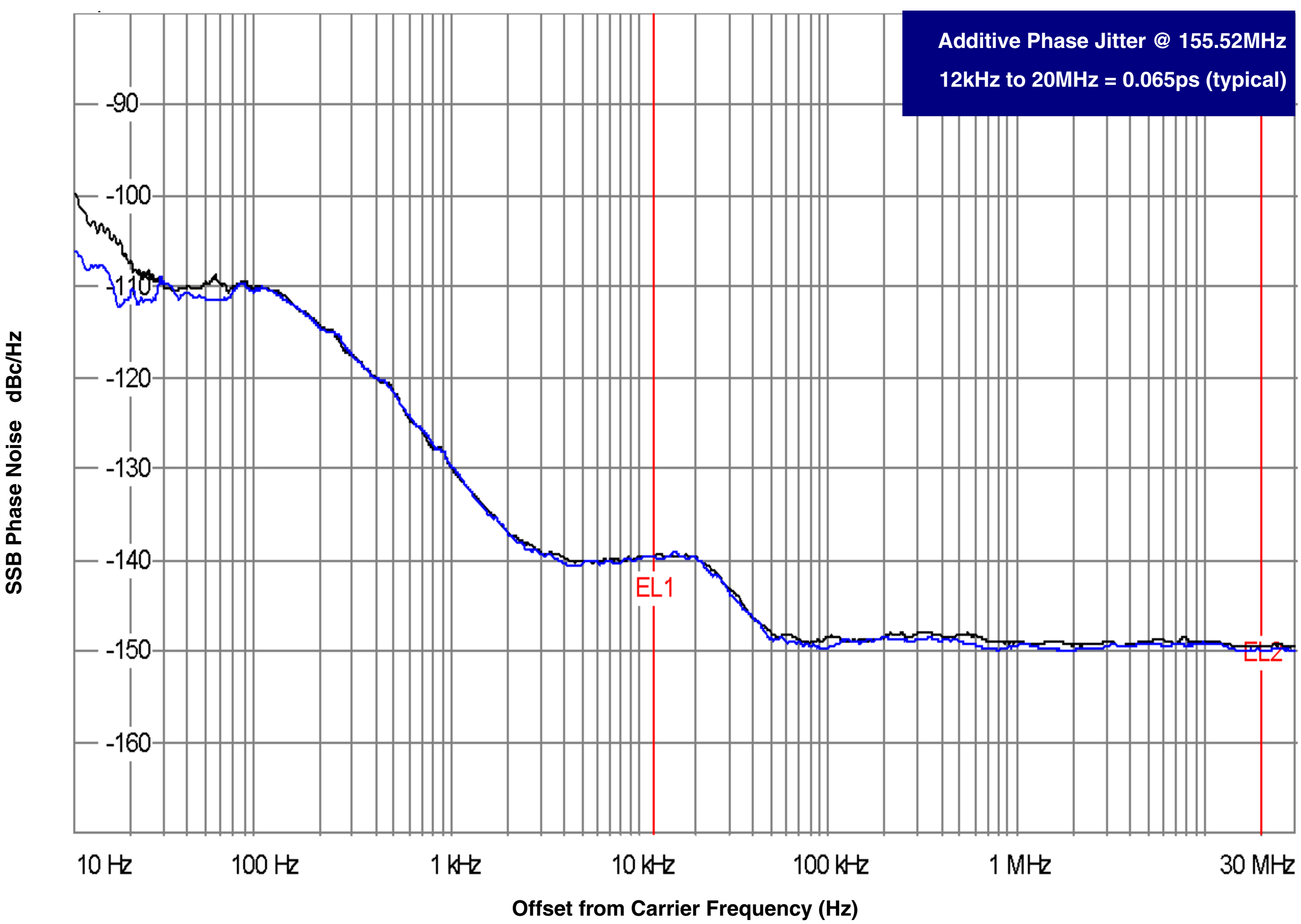
Table 5. AC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				2.5	GHz
t_{PD}	Propagation Delay; NOTE 1		300		600	ps
*t*jit(Ø)	Buffer Additive Phase Jitter, RMS; Refer to Additive Phase Jitter Section	155.52MHz, Integration Range: 12kHz – 20MHz		0.065		ps
tsk(pp)	Part-to-Part Skew; NOTE 2, 3				300	ps
tsk(i)	Input Skew				50	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	75		250	ps
$MUX_{ISOLATION}$	MUX Isolation; NOTE 4	155.52MHz, V_{PP} = 400mV		85		dB

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
All parameters measured ≤ 1.0GHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Q/nQ output measured differentially. See *Parameter Measurement Information* for MUX Isolation diagram.

Additive Phase Jitter

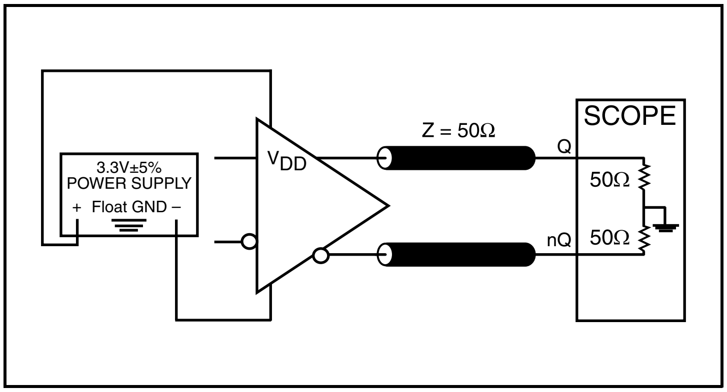
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



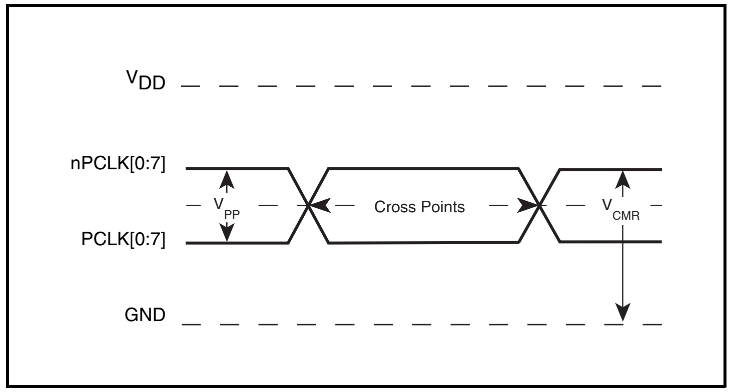
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

The source generator "IFR2042 10kHz – 56.4GHz Low Noise Signal Generator as external input to an Agilent 8133A 3GHz Pulse Generator".

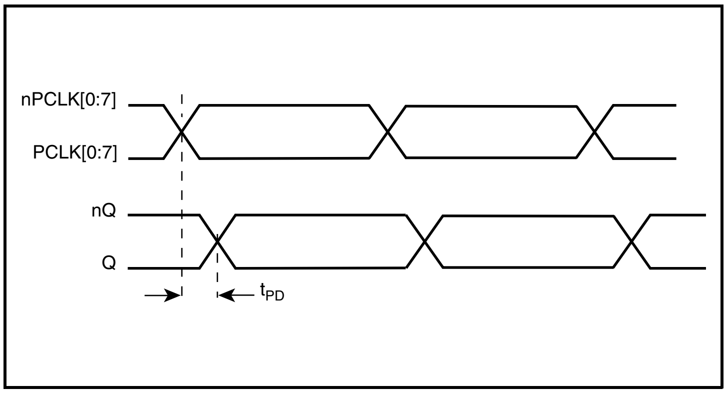
Parameter Measurement Information



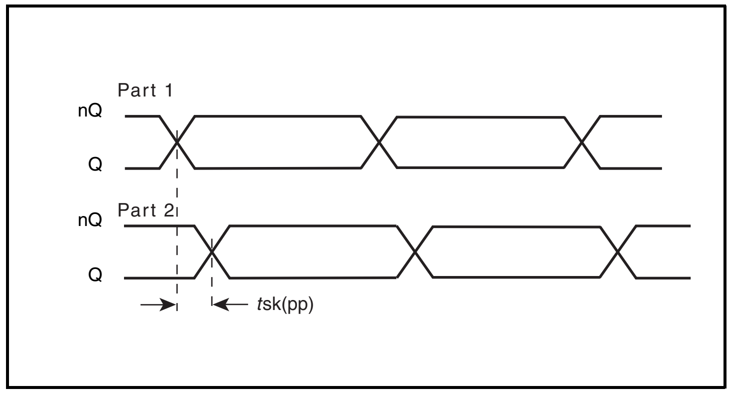
3.3V LVDS Output Load AC Test Circuit



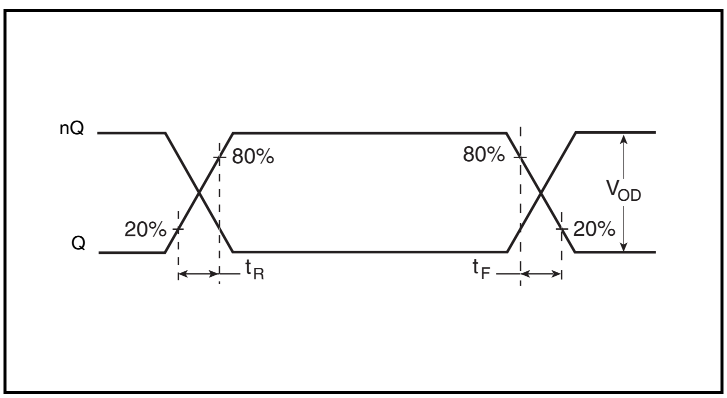
Differential Input Level



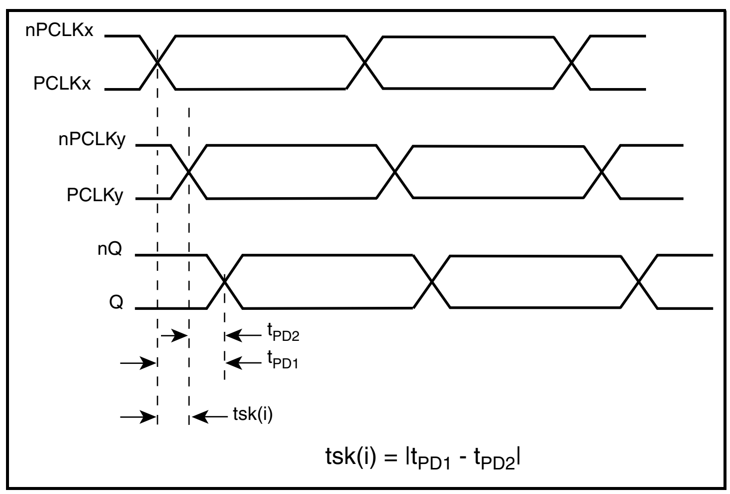
Propagation Delay



Part-to-Part Skew

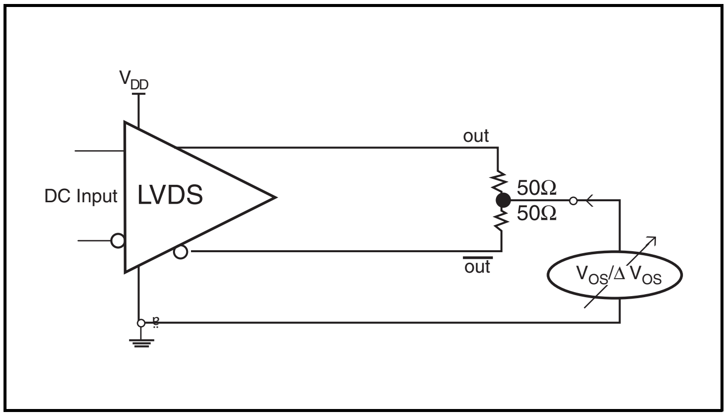


Output Rise/Fall Time

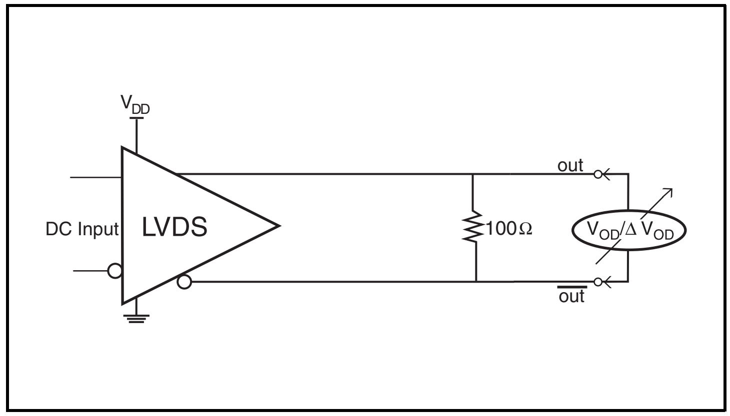


Input Skew

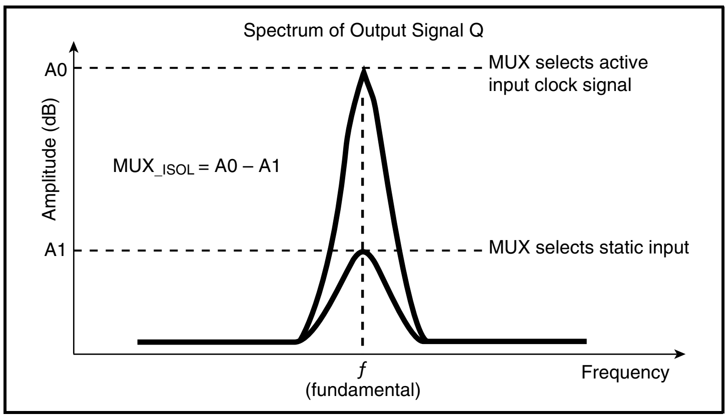
Parameter Measurement Information, continued



Offset Voltage Setup



Differential Output Voltage



MUX Isolation

Application Information

Recommendations for Unused Input Pins

Inputs:

PCLK/nPCLK Inputs

For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground.

LVCMOS Control Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, LVDS, SSTL and other differential signals. The differential signal must meet the V_{PP} and V_{CMR} input requirements. *Figures 1A to 1D* show interface examples for the PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

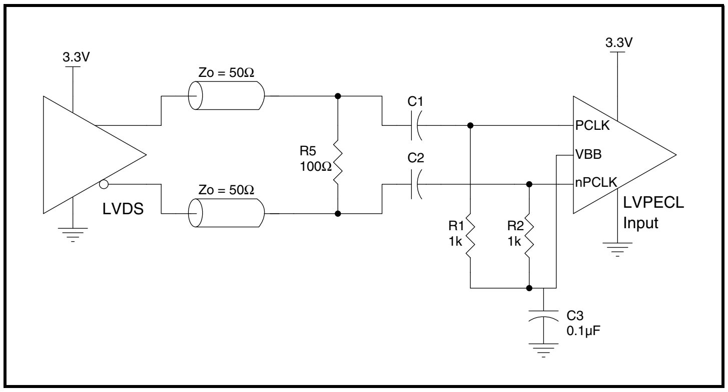


Figure 1A. PCLK/nPCLK Input Driven by a 3.3V LVDS Driver

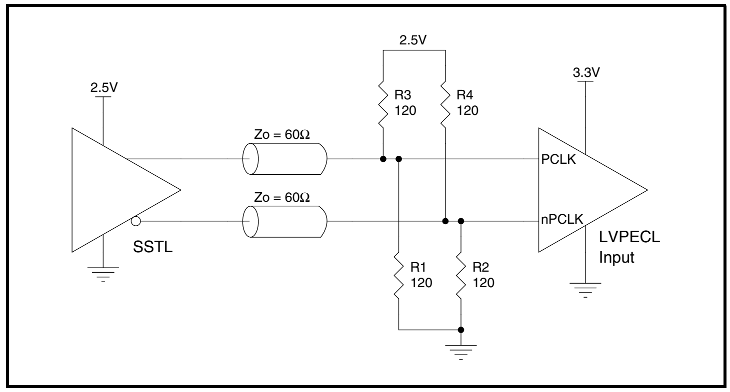


Figure 1B. PCLK/nPCLK Input Driven by an SSTL Driver

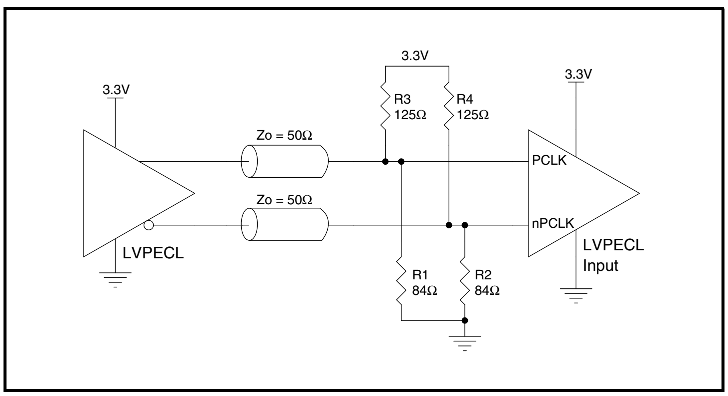


Figure 1C. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

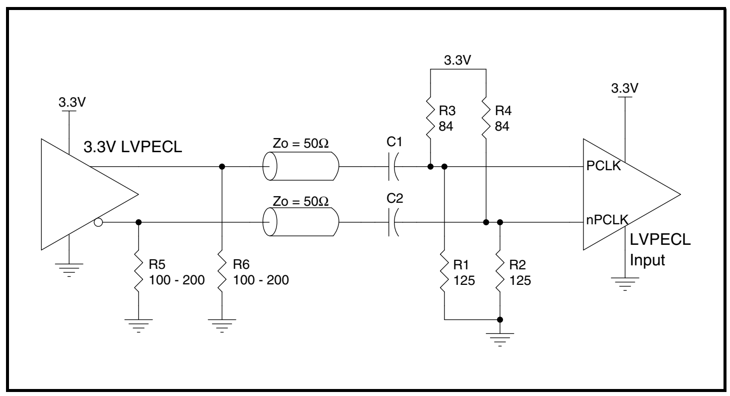


Figure 1D. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

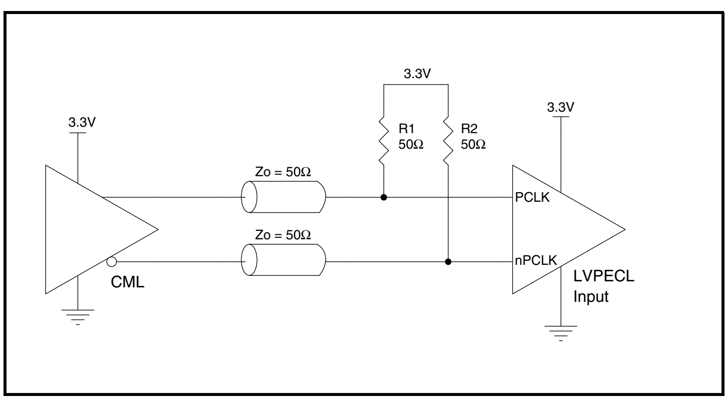


Figure 1E. PCLK/nPCLK Input Driven by a CML Driver

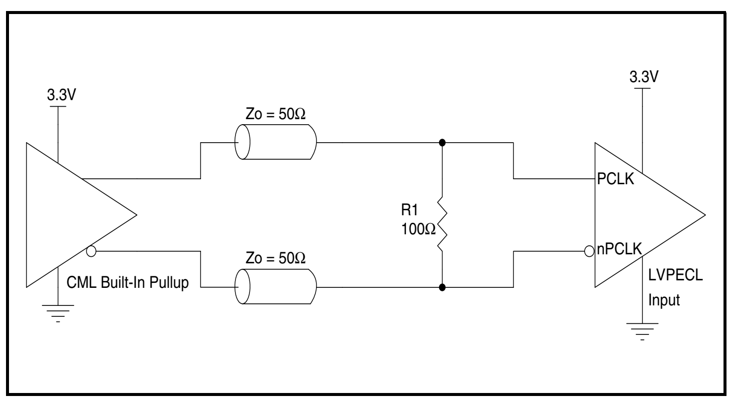


Figure 1F. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

Wiring the Differential Input to Accept Single-Ended Levels

Figure 2 shows how the differential input can be wired to accept single-ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

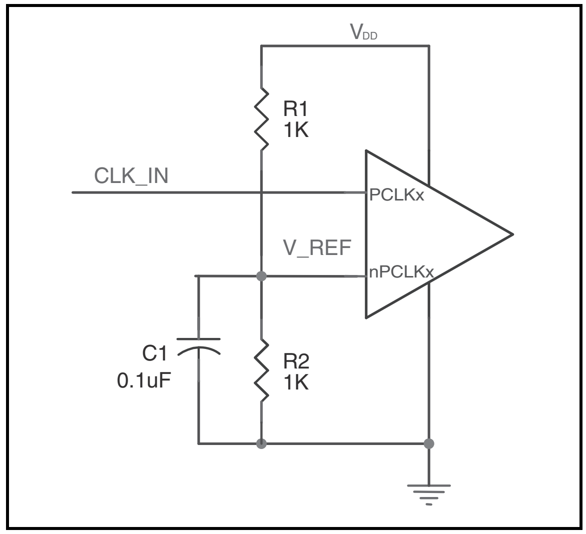


Figure 2. Single-Ended Signal Driving Differential Input

3.3V LVDS Driver Termination

A general LVDS interface is shown in *Figure 3.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

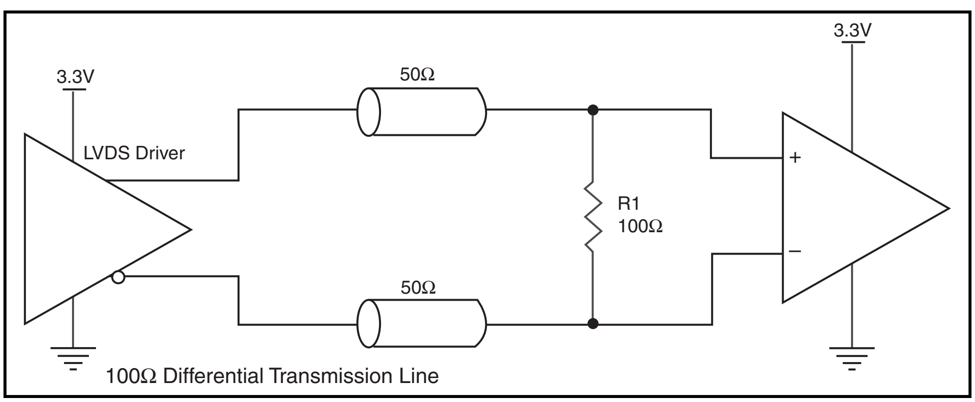


Figure 3. Typical LVDS Driver Termination

Schematic Example

An application schematic example of ICS854S058I is shown in *Figure 4.* The inputs can accept various types of differential signals. In this example, the inputs are driven by LVDS drivers. The transmission lines are assumed to be 100Ω differential. The 100Ω matched loads termination should be located near the receivers. It is recommended at least one decoupling capacitor per power pin. The decoupling capacitor should be low ESR and located as close as possible to the power pin.

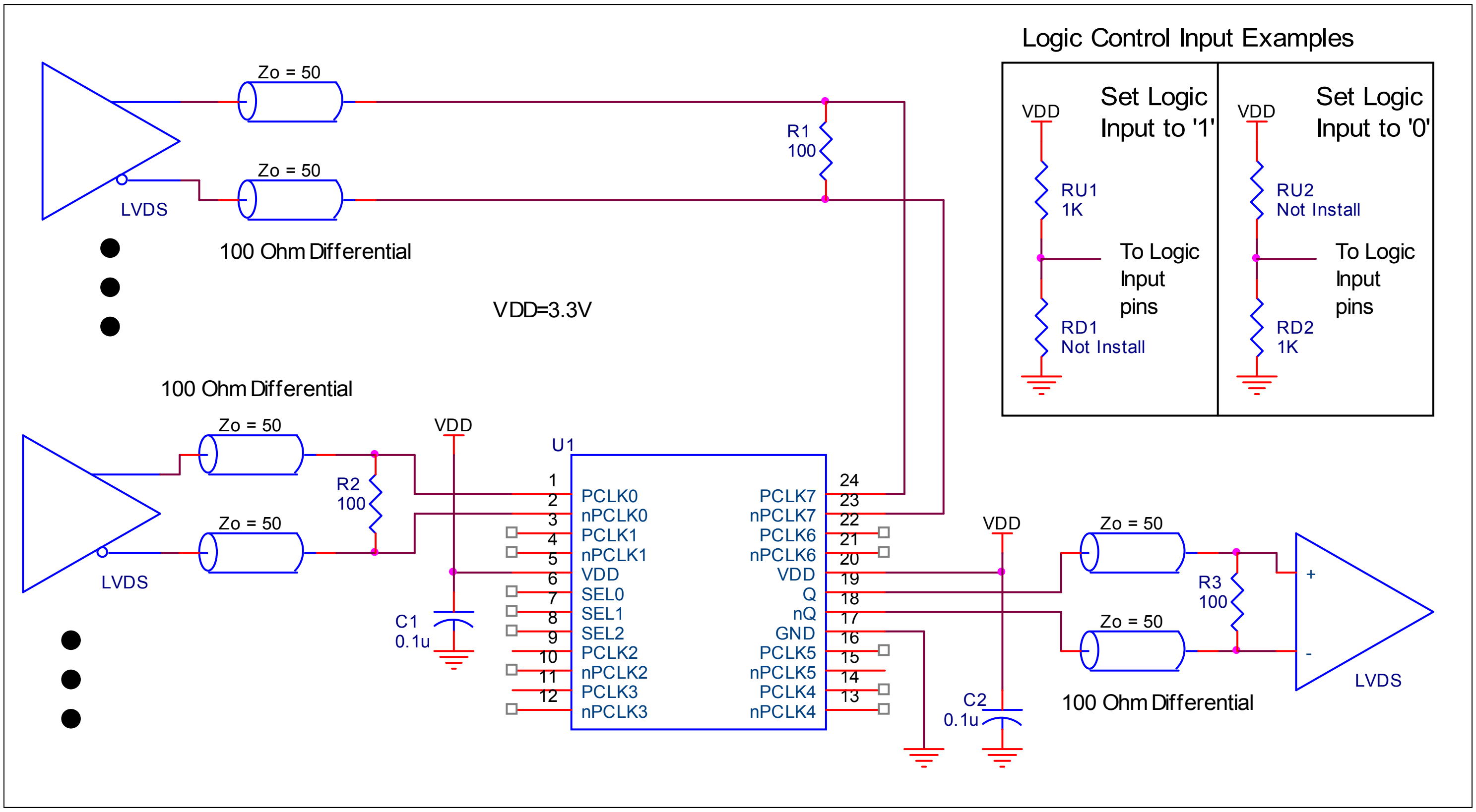


Figure 4. ICS854S058I Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS854S058I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS854S058I is the sum of the core power plus the power dissipation in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipation in the load.

- Power $(core)_{MAX} = V_{DD\_MAX} * I_{DD\_MAX}$ = 3.465V * 66mA = **228.7mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 85.1°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.229W * 85.16°C/W = 104.5°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 24 Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	85.1°C/W	79.7°C/W	76.5°C/W

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 24 Lead TSSOP

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	85.1°C/W	79.7°C/W	76.5°C/W

Transistor Count

The transistor count for ICS854S058I is: 446

This device is pin and function compatible, and a suggested replacement for ICS854058.

Package Outline and Package Dimensions

Package Outline - G Suffix for 24 Lead TSSOP

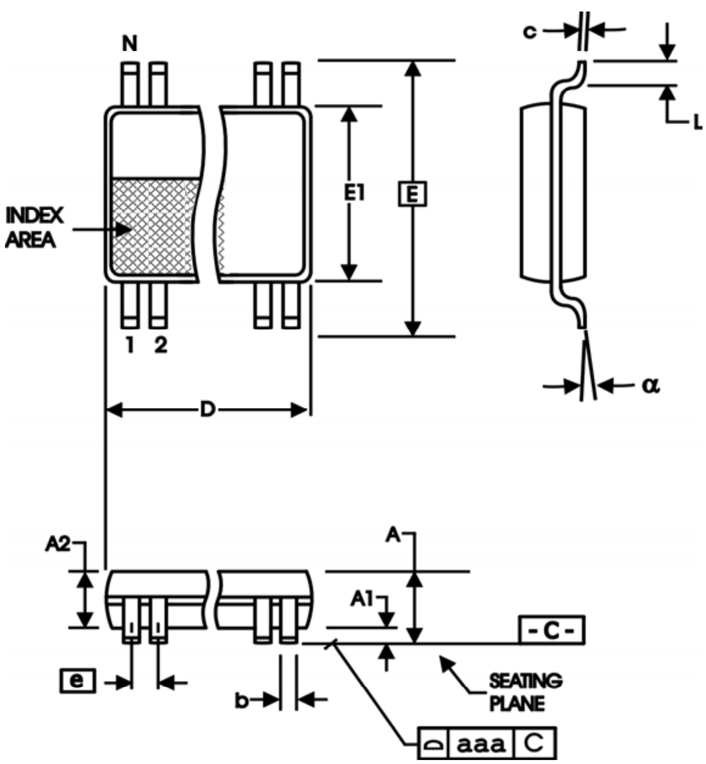


Table 8. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	24	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
854S058AGILF	ICS854S058AIL	“Lead-Free” 24 Lead TSSOP	Tube	-40°C to 85°C
854S058AGILFT	ICS854S058AIL	“Lead-Free” 24 Lead TSSOP	Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A		1	Deleted HiperClockS Logo. Updated GD paragraph to include CML. Added CML to 3rd bullet.	10/29/12
		9	Added figures 1E and 1F.	
	T10	16	Deleted quantity from tape and reel.	

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