# 873991

# Low Voltage, LVCMOS/ LVPECL-to-LVPECL/ECL Clock Generator

## General Description

The 873991 is a low voltage, low skew, 3.3V LVPECL or ECL Clock Generator . The 873991 has two selectable clock inputs. The PCLK, nPCLK pair can accept an LVPECL input and the TEST_CLK pin can accept a LVCMOS or LVTTL input. This device has a fully integrated PLL along with frequency configurable outputs. An external feedback input and output regenerates clocks with “zero delay”.

The four independent banks of outputs each have their own output dividers, which allow the device to generate a multitude of different bank frequency ratios and output-to-input frequency ratios. The output frequency range is 25MHz to 400MHz and the input frequency range is 6.25MHz to 125MHz. The PLL_SEL input can be used to bypass the PLL for test and system debug purposes. In bypass mode, the input clock is routed around the PLL and into the internal output dividers.

The 873991 also has a SYNC output which can be used for system synchronization purposes. It monitors Bank A and Bank C outputs for coincident rising edges and signals a pulse per the timing diagrams in this data sheet. This feature is used primarily in applications where Bank A and Bank C are running at different frequencies, and is particularly useful when they are running at non-integer multiples of each other.

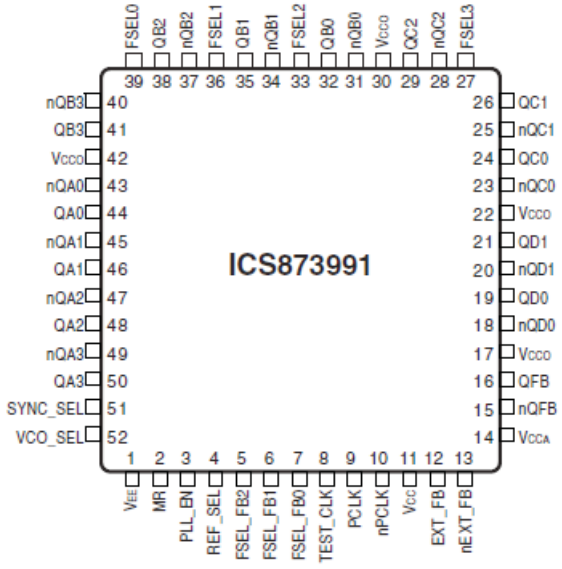
Example Applications:

1. Line Card Multiplier: Multiply 19.44MHz from a back-plane to 77.76MHz on the line card ASIC and Serdes.
2. Zero Delay Buffer: Fan out up to thirteen 100MHz copies from a reference clock to multiple processing units on an embedded system.

## Features

- 14 differential LVPECL outputs
- Selectable differential LVPECL or TEST_CLK inputs
- PCLK, nPCLK can accept the following input levels: LVPECL, CML, SSTL
- TEST_CLK accepts the following input levels: LVCMOS, LVTTL
- Input frequency range: 6.25MHz to 125MHz
- Output frequency: 400MHz (maximum)
- VCO range: 200MHz to 800MHz
- Output skew: 250ps (maximum)
- Cycle-to-cyle jitter: ±50ps (typical)
- LVPECL mode operating voltage supply range: $V_{CC}$ = 3.135V to 3.465V, $V_{EE}$ = 0V
- ECL mode operating voltage supply range: $V_{CC}$ = 0V, $V_{EE}$ = -3.465V to -3.135V
- 0°C to 70°C ambient operating temperature
- Industrial temperature available upon request
- Lead-Free package fully RoHS compliant
- Use replacement part 873996AYLF

## Pin Assignment




**52-Lead LQFP**
10mm x 10mm x 1.4mm package body
**Y package**
Top View

# BLOCK DIAGRAM

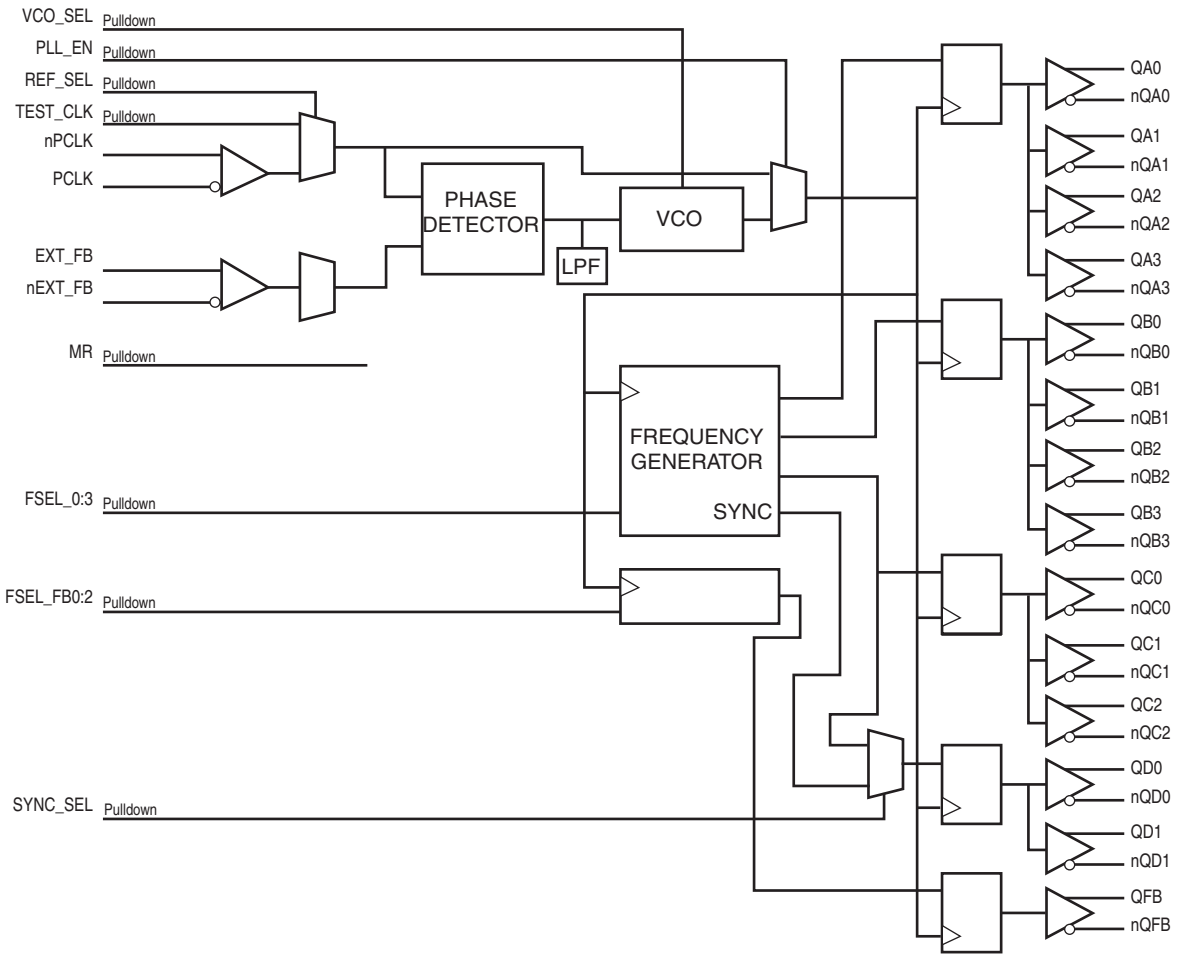


**TABLE 1. PIN DESCRIPTIONS**

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1 | $V_{EE}$ | Power | | Negative supply pin. |
| 2 | MR | Input | Pulldown | Active High Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs (Qx) to go low and the inverted outputs (nQx) to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels. |
| 3 | PLL_EN | Input | Pulldown | PLL enable pin. When logic LOW, PLL is enabled. When logic HIGH, PLL is in bypass mode. LVCMOS/LVTTL interface levels. |
| 4 | REF_SEL | Input | Pulldown | Selects between the different reference inputs as the PLL reference source. When logic LOW, selects PCLK/nPCLK. When logic HIGH, selects TEST_CLK. LVCMOS/LVTTL interface levels. |
| 5<br>6<br>7 | FSEL_FB2<br>FSEL_FB1<br>FSEL_FB0 | Input | Pulldown | Feedback frequency select pins. LVCMOS/LVTTL interface levels. |
| 8 | TEST_CLK | Input | Pulldown | LVCMOS/LVTTL test clock input. |
| 9 | PCLK | Input | Pulldown | Non-inverting differential LVPECL clock input. |
| 10 | nPCLK | Input | Pullup/ Pulldown | Inverting differential LVPECL clock input. $V_{CC}/2$ default when left floating. |
| 11 | $V_{CC}$ | Power | | Core supply pin. |
| 12 | EXT_FB | Input | Pulldown | External feedback input. |
| 13 | nEXT_FB | Input | Pullup/ Pulldown | External feedback input. t. $V_{CC}/2$ default when left floating. |
| 14 | $V_{CCA}$ | Power | | Analog supply pin. |
| 15<br>16 | nQFB<br>QFB | Output | | Differential feedback output pair. LVPECL Interface levels. |
| 17, 22, 30, 42 | $V_{CCO}$ | Power | | Output supply pins. |
| 18, 19 | nQD0, QD0 | Output | | Differential output pair. LVPECL interface levels. |
| 20, 21 | nQD1, QD1 | Output | | Differential output pair. LVPECL interface levels. |
| 23, 24 | nQC0, QC0 | Output | | Differential output pair. LVPECL interface levels. |
| 25, 26 | nQC1, QC1 | Output | | Differential output pair. LVPECL interface levels. |
| 27<br>33<br>36<br>39 | FSEL3<br>FSEL2<br>FSEL1<br>FSEL0 | Input | Pulldown | Frequency select pins. LVCMOS/LVTTL interface levels. |
| 28, 29 | nQC2, QC2 | Output | | Differential output pair. LVPECL interface levels. |
| 31, 32 | nQB0, QB0 | Output | | Differential output pair. LVPECL interface levels. |
| 34, 35 | nQB1, QB1 | Output | | Differential output pair. LVPECL interface levels. |
| 37, 38 | nQB2, QB2 | Output | | Differential output pair. LVPECL interface levels. |
| 40, 41 | nQB3, QB3 | Output | | Differential output pair. LVPECL interface levels. |
| 43, 44 | nQA0, QA0 | Output | | Differential output pair. LVPECL interface levels. |
| 45, 46 | nQA1, QA1 | Output | | Differential output pair. LVPECL interface levels. |
| 47, 48 | nQA2, QA2 | Output | | Differential output pair. LVPECL interface levels. |
| 49, 50 | nQA3, QA3 | Output | | Differential output pair. LVPECL interface levels. |
| 51 | SYNC_SEL | Input | Pulldown | SYNC output select pin. When LOW, the SYNC otuput follows the timing diagram (page 5). When HIGH, QD output follows QC output. |
| 52 | VCO_SEL | Input | Pulldown | Selects VCO range. LVCMOS/LVTTL interface levels. |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

### Table 2. Pin Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | 4 | | pF |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | 51 | | kΩ |
| $R_{PULLup}$ | Input Pullup Resistor | | | 51 | | kΩ |

### Table 3A. Select Pin Function Table

| Inputs | | | | Outputs | | |
|---|---|---|---|---|---|---|
| FSEL3 | FSEL2 | FSEL1 | FSEL0 | QAx | QBx | QCx |
| 0 | 0 | 0 | 0 | ÷ 2 | ÷ 2 | ÷ 2 |
| 0 | 0 | 0 | 1 | ÷ 2 | ÷ 2 | ÷ 4 |
| 0 | 0 | 1 | 0 | ÷ 2 | ÷ 4 | ÷ 4 |
| 0 | 0 | 1 | 1 | ÷ 2 | ÷ 2 | ÷ 6 |
| 0 | 1 | 0 | 0 | ÷ 2 | ÷ 6 | ÷ 6 |
| 0 | 1 | 0 | 1 | ÷ 2 | ÷ 4 | ÷ 6 |
| 0 | 1 | 1 | 0 | ÷ 2 | ÷ 4 | ÷ 8 |
| 0 | 1 | 1 | 1 | ÷ 2 | ÷ 6 | ÷ 8 |
| 1 | 0 | 0 | 0 | ÷ 2 | ÷ 2 | ÷ 8 |
| 1 | 0 | 0 | 1 | ÷ 2 | ÷ 8 | ÷ 8 |
| 1 | 0 | 1 | 0 | ÷ 4 | ÷ 4 | ÷ 6 |
| 1 | 0 | 1 | 1 | ÷ 4 | ÷ 6 | ÷ 6 |
| 1 | 1 | 0 | 0 | ÷ 4 | ÷ 6 | ÷ 8 |
| 1 | 1 | 0 | 1 | ÷ 6 | ÷ 6 | ÷ 8 |
| 1 | 1 | 1 | 0 | ÷ 6 | ÷ 8 | ÷ 8 |
| 1 | 1 | 1 | 1 | ÷ 8 | ÷ 8 | ÷ 8 |

### Table 3B. Feedback Control Function Table

| Inputs | | | Outputs |
|---|---|---|---|
| FSEL_FB2 | FSEL_FB1 | FSEL_FB0 | QFB |
| 0 | 0 | 0 | ÷2 |
| 0 | 0 | 1 | ÷4 |
| 0 | 1 | 0 | ÷6 |
| 0 | 1 | 1 | ÷8 |
| 1 | 0 | 0 | ÷8 |
| 1 | 0 | 1 | ÷16 |
| 1 | 1 | 0 | ÷24 |
| 1 | 1 | 1 | ÷32 |

### Table 3C. Input Control Function Table

| Control Input Pin | Logic 0 | Logic 1 |
|---|---|---|
| PLL_EN | Enables PLL | Bypasses PLL |
| VCO_SEL | fVCO | fVCO/2 |
| REF_SEL | Selects PCLK/nPCLK | Selects TEST_CLK |
| MR | --- | Resets outputs |
| SYNC_SEL | Selects outputs | Match QC Outputs |

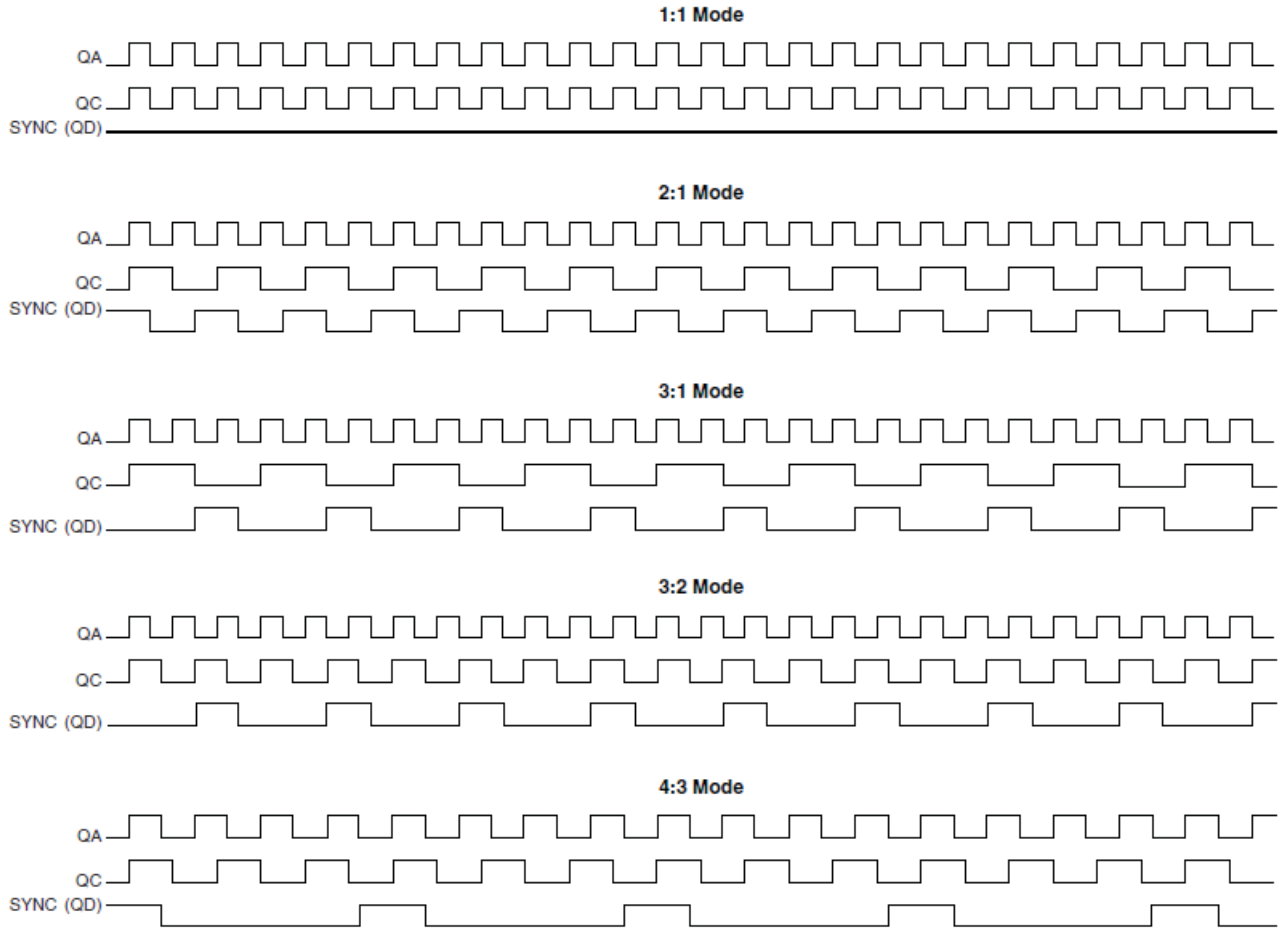



**FIGURE 1. TIMING DIAGRAMS**

## Absolute Maximum Ratings

| | |
|---|---|
| Supply Voltage, $V_{CC}$ | 4.6V |
| Inputs, $V_I$ | -0.5V to $V_{CC}$ + 0.5 V |
| Outputs, $I_O$ | |
| Continuous Current | 50mA |
| Surge Current | 100mA |
| Package Thermal Impedance, $\theta_{JA}$ | 42.3°C/W (0 lfpm) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

**NOTE:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maxi-mum rating conditions for extended periods may affect product reliability.

**Table 4A. Power Supply DC Characteristics,** $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ to $70°C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{CCA}$ | Analog Supply Voltage | | 3.135 | 3.3 | 3.465 | |
| $V_{CCO}$ | Output Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $I_{CC}$ | Power Supply Current | | | | 150 | mA |
| $I_{CCA}$ | Analog Supply Current | | | | 15 | mA |
| $I_{CCO}$ | Output Supply Current | | | | 95 | mA |

**Table 4B. LVCMOS/LVTTL DC Characteristics,** $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ to $70°C$

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | PLL_EN, VCO_SEL, REF_SEL, SYNC_SEL, FSEL_FB0:FSEL_FB2, FSEL0:FSEL3, MR | | 2 | | $V_{CC}$ + 0.3 | V |
| | | TEST_CLK | | 2 | | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | PLL_EN, VCO_SEL, REF_SEL, SYNC_SEL, FSEL_FB0:FSEL_FB2, FSEL0:FSEL3, MR | | -0.3 | | 0.8 | V |
| | | TEST_CLK | | -0.3 | | 1.3 | V |
| $I_{IH}$ | Input High Current | | $V_{CC} = V_{IN} = 3.465V$ | | | 150 | µA |
| $I_{IL}$ | Input Low Current | | $V_{IN} = 0V$, $V_{CC} = 3.465V$ | -5 | | | µA |

**Table 4C. LVPECL DC Characteristics,** $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ to $70°C$

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $I_{IH}$ | Input High Current | PCLK | $V_{CC} = V_{IN} = 3.465V$ | | | 150 | µA |
| | | nPCLK | $V_{CC} = V_{IN} = 3.465V$ | | | 5 | µA |
| $I_{IL}$ | Input Low Current | PCLK | $V_{CC} = 3.465V$, $V_{IN} = 0V$ | -5 | | | µA |
| | | nPCLK | $V_{CC} = 3.465V$, $V_{IN} = 0V$ | -150 | | | µA |
| $V_{PP}$ | Peak-to-Peak Input Voltage | | | 0.3 | | 1 | V |
| $V_{CMR}$ | Common Mode Input Voltage; NOTE 1, 2 | | | $V_{EE}$ + 1.5 | | $V_{CC}$ | V |
| $V_{OH}$ | Output High Voltage; NOTE 3 | | | $V_{CC}$ - 1.4 | | $V_{CC}$ - 0.9 | V |
| $V_{OL}$ | Output Low Voltage; NOTE 3 | | | $V_{CC}$ - 2.0 | | $V_{CC}$ - 1.7 | V |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing | | | 0.6 | | 1 | V |

NOTE 1: Common mode voltage is defined as $V_{IH}$.
NOTE 2: For single ended applications, the maximum input voltage for PCLK, nPCLK is $V_{CC}$ + 0.3V.
NOTE 3: Outputs terminated with 50Ω to $V_{CCO}$ - 2V. .

**TABLE 5. PLL INPUT REFERENCE CHARACTERISTICS,** $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, $T_A$ = 0°C TO 70°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $t_R$ / $t_R$ | Input Rise/Fall Time | TEST_CLK | | | | 3 | ns |
| $f_{REF}$ | Reference Frequency VCO_SEL = 0 | | Feedback ÷ 6 | 66.66 | | 133.33 | MHz |
| | | | Feedback ÷ 8 | 50 | | 100 | MHz |
| | | | Feedback ÷ 16 | 25 | | 50 | MHz |
| | | | Feedback ÷ 24 | 16.66 | | 33.33 | MHz |
| | | | Feedback ÷ 32 | 12.5 | | 25 | MHz |
| | Reference Frequency VCO_SEL = 1 | | Feedback ÷ 4 | 50 | | 100 | MHz |
| | | | Feedback ÷ 6 | 33.33 | | 66.66 | MHz |
| | | | Feedback ÷ 8 | 25 | | 50 | MHz |
| | | | Feedback ÷ 16 | 12.5 | | 25 | MHz |
| | | | Feedback ÷ 24 | 8.33 | | 16.66 | MHz |
| | | | Feedback ÷ 32 | 6.25 | | 12.5 | MHz |
| $f_{REFDC}$ | Reference Input Duty Cycle | | | 25 | | 75 | % |

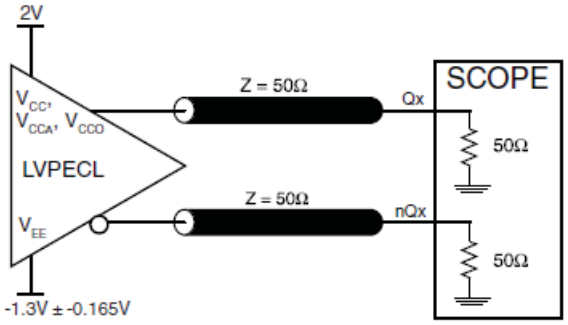
NOTE: These parameters are guaranteed by design, but are not tested in production.

**TABLE 6. AC CHARACTERISTICS,** $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, $T_A$ = 0°C TO 70°C

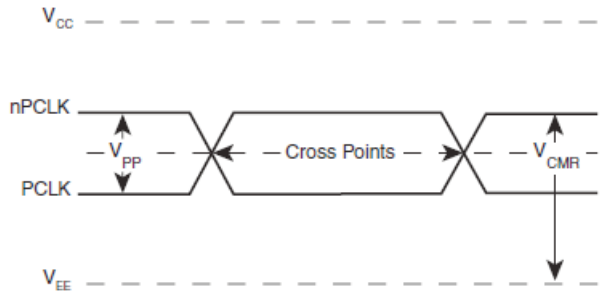
| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | Output Frequency | | | | | 400 | MHz |
| t(Ø) | Static Phase Offset; NOTE 1, 5 | PCLK, nPCLK | | 0 | 170 | 325 | ps |
| tsk(o) | Output Skew; NOTE 2, 3 | | | | | 250 | ps |
| tsk(w) | Multiple Frequency Skew; NOTE 3, 6 | | | | | 350 | ps |
| tjit(cc) | Cycle-to-Cycle Jitter; NOTE 3 | | | | ±50 | | ps |
| $f_{VCO}$ | PLL VCO Lock Range; NOTE 4 | | PLL_SEL = 0 | 400 | | 800 | MHz |
| | | | PLL_SEL = 1 | 200 | | 400 | MHz |
| $t_{LOCK}$ | PLL Lock Time | | | | | 10 | ms |
| $t_R$ / $t_F$ | Output Rise/Fall Time | | 20% to 80% | 0.2 | | 1 | ns |
| odc | Output Duty Cycle | | | 45 | | 55 | % |

All parameters measured at $f_{MAX}$ unless noted otherwise.
NOTE 1: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable.
NOTE 2:Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: When VCO_SEL = 0, the PLL will be unstable with feedback configurations of ÷2, ÷4 and some ÷6. When VCO_SEL = 1, the PLL will be unstable with a feedback configuration of ÷2.
NOTE 5: Static phase offset is specified for an input frequency of 50MHz with feedback in ÷8.
NOTE 6: Defined as skew across banks of outputs switching in the same direction operating at different frequencies with the same supply voltages and equal load conditions. Measured at $V_{CCO}/2$.

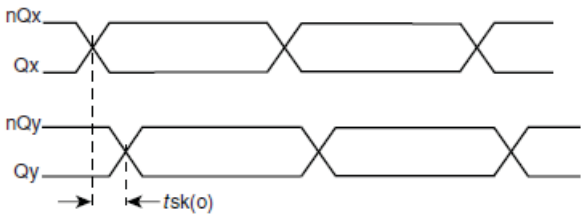
# PARAMETER MEASUREMENT INFORMATION



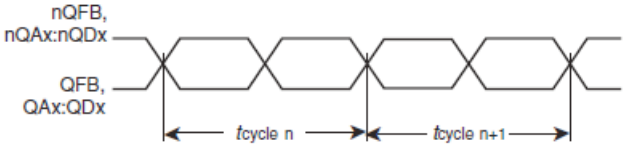

**OUTPUT LOAD AC TEST CIRCUIT**




**DIFFERENTIAL INPUT LEVELS**

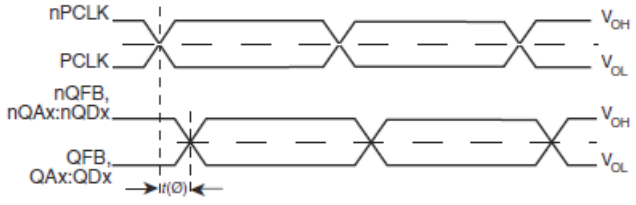



**OUTPUT SKEW**

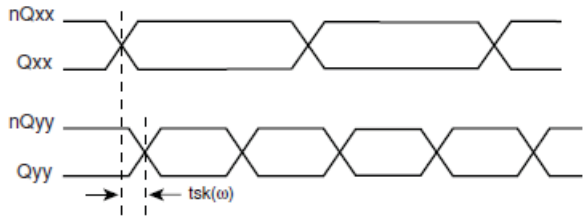



$t_{jit(cc)} = t_{cycle\ n} - t_{cycle\ n+1}$
1000 Cycles

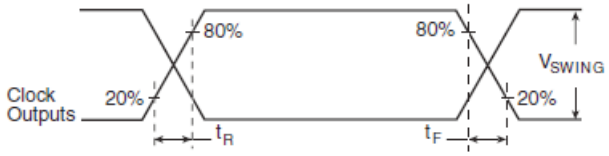
**CYCLE-TO-CYCLE JITTER**



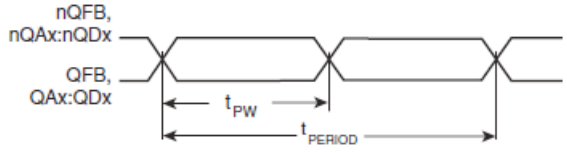

**STATIC PHASE OFFSET**




**MULTIPLE FREQUENCY SKEW**




**OUTPUT RISE/FALL TIME**




$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

**OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD**

# APPLICATION INFORMATION

## POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The 873991 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. $V_{CC}$, $V_{CCA}$, and $V_{CCO}$ should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 2* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each $V_{CCA}$ pin.

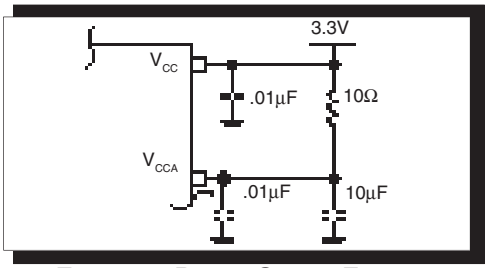



FIGURE 2. POWER SUPPLY FILTERING

## WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

*Figure 3* shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = $V_{CC}$/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{CC}$ = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

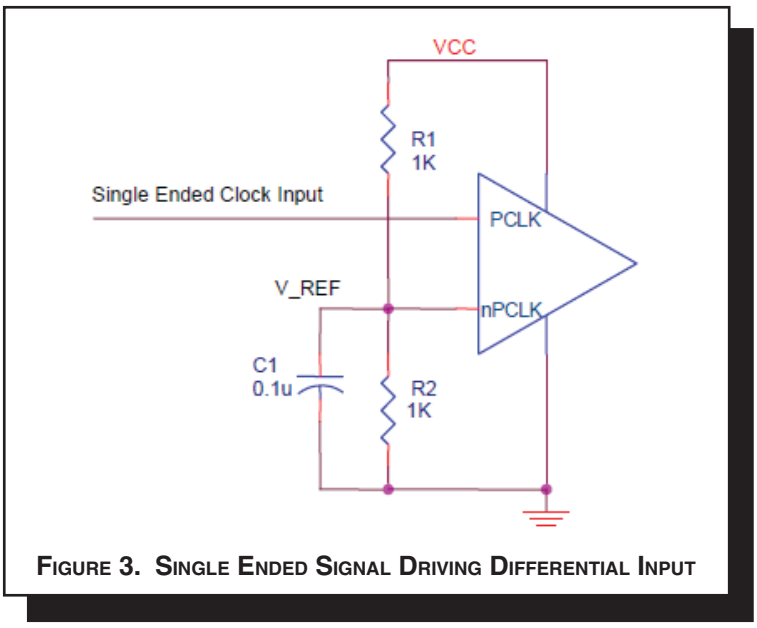



FIGURE 3. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

## TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

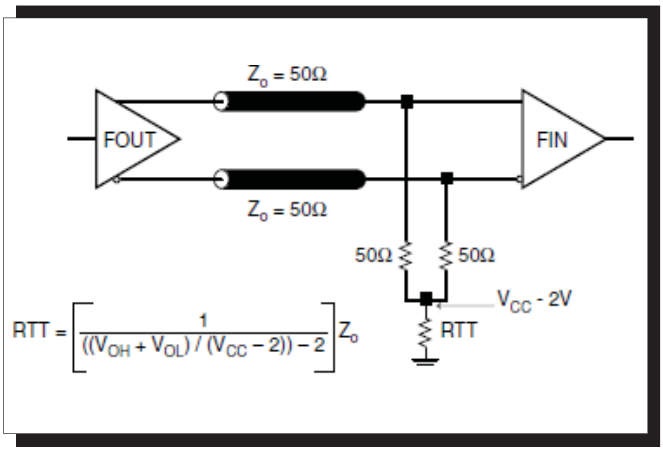



FIGURE 4A. LVPECL OUTPUT TERMINATION

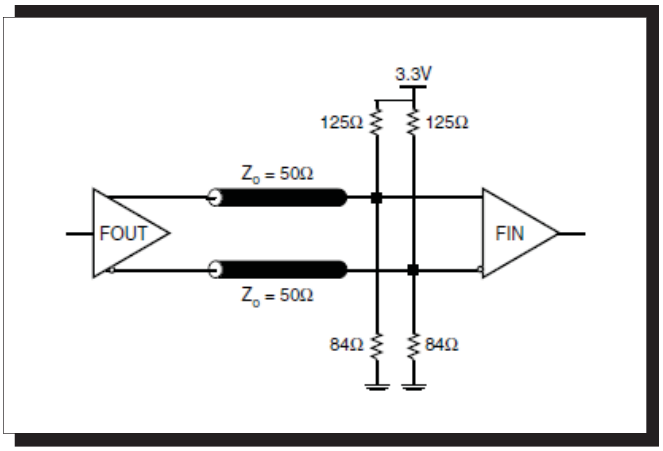



FIGURE 4B. LVPECL OUTPUT TERMINATION

## LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both $V_{SWING}$ and $V_{OH}$ must meet the $V_{PP}$ and $V_{CMR}$ input requirements. *Figures 5A to 5D* show interface examples for the PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

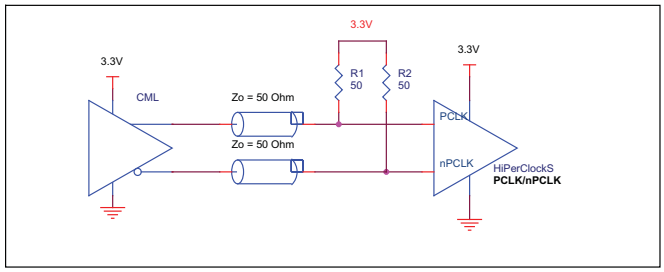



**Figure 5A. PCLK/nPCLK Input Driven by a CML Driver**

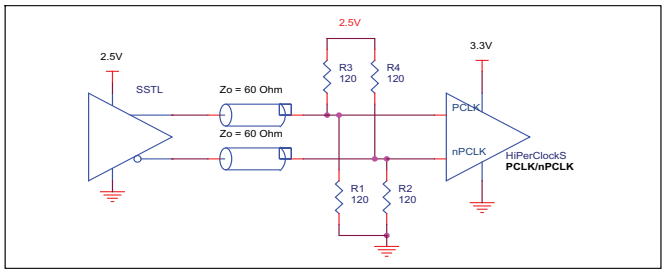



**Figure 5B. PCLK/nPCLK Input Driven by an SSTL Driver**

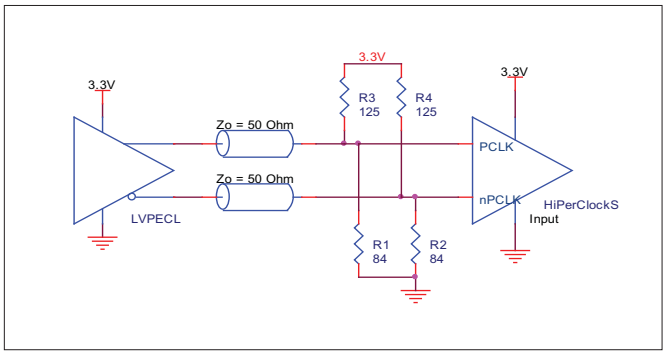



**Figure 5C. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver**

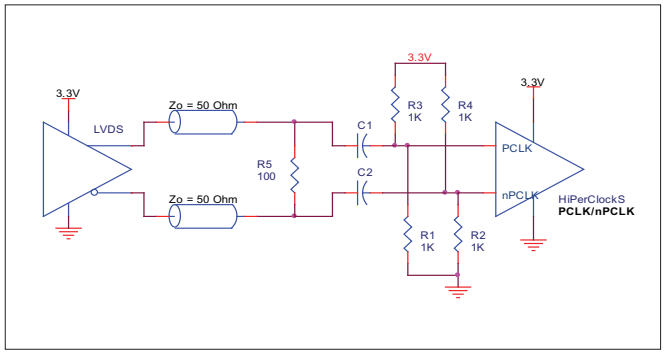



**Figure 5D. PCLK/nPCLK Input Driven by a 3.3V LVDS Driver**

# POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 873991.
Equations and example calculations are also provided.

*1. Power Dissipation.*
The total power dissipation for the 873991 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for $V_{CC}$ = 3.3V + 5% = 3.465V, which gives worst case results.
**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = $V_{CC\_MAX}$ * $I_{EE\_MAX}$ = 3.465V * 165mA = **571.7mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 14 * 30mW = **420mW**

**Total Power$_{_MAX}$** (3.465V, with all outputs switching) = 571.7mW + 420mW = **991.7mW**

*2. Junction Temperature.*
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for the devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

$\theta_{JA}$ = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)
$T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 47.1°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.992W * 47.1°C/W = 116.7°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**TABLE 7. THERMAL RESISTANCE $\theta_{JA}$ FOR 52-PIN LQFP, FORCED CONVECTION**

| $\theta_{JA}$ by Velocity (Linear Feet per Minute) | 0 | 200 | 500 |
|---|---|---|---|
| Single-Layer PCB, JEDEC Standard Test Boards | 58.0°C/W | 47.1°C/W | 42.0°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 42.3°C/W | 36.4°C/W | 34.0°C/W |

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

*3. Calculations and Equations.*

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 6.*

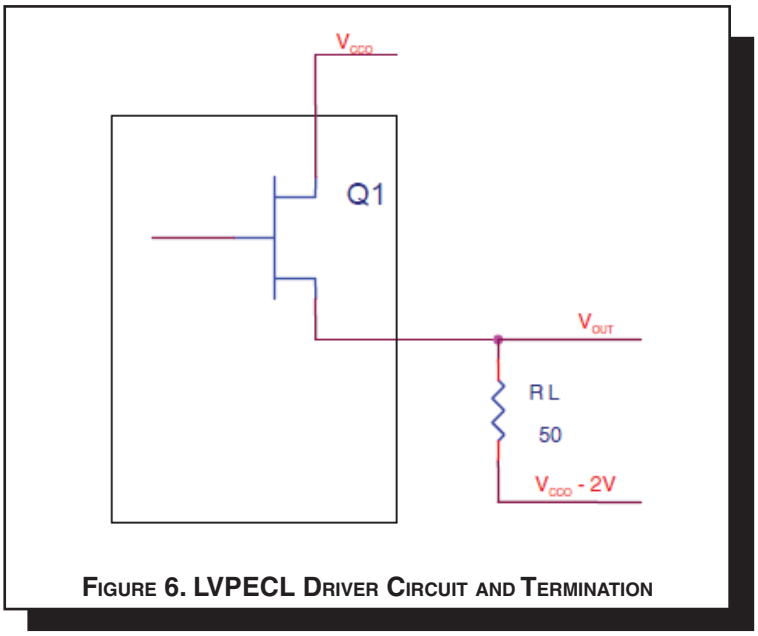



**FIGURE 6. LVPECL DRIVER CIRCUIT AND TERMINATION**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CCO}$ - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 0.9V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} - 1.7V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

# RELIABILITY INFORMATION

**TABLE 8. $\theta_{JA}$ VS. AIR FLOW TABLE FOR 52 LEAD LQFP**

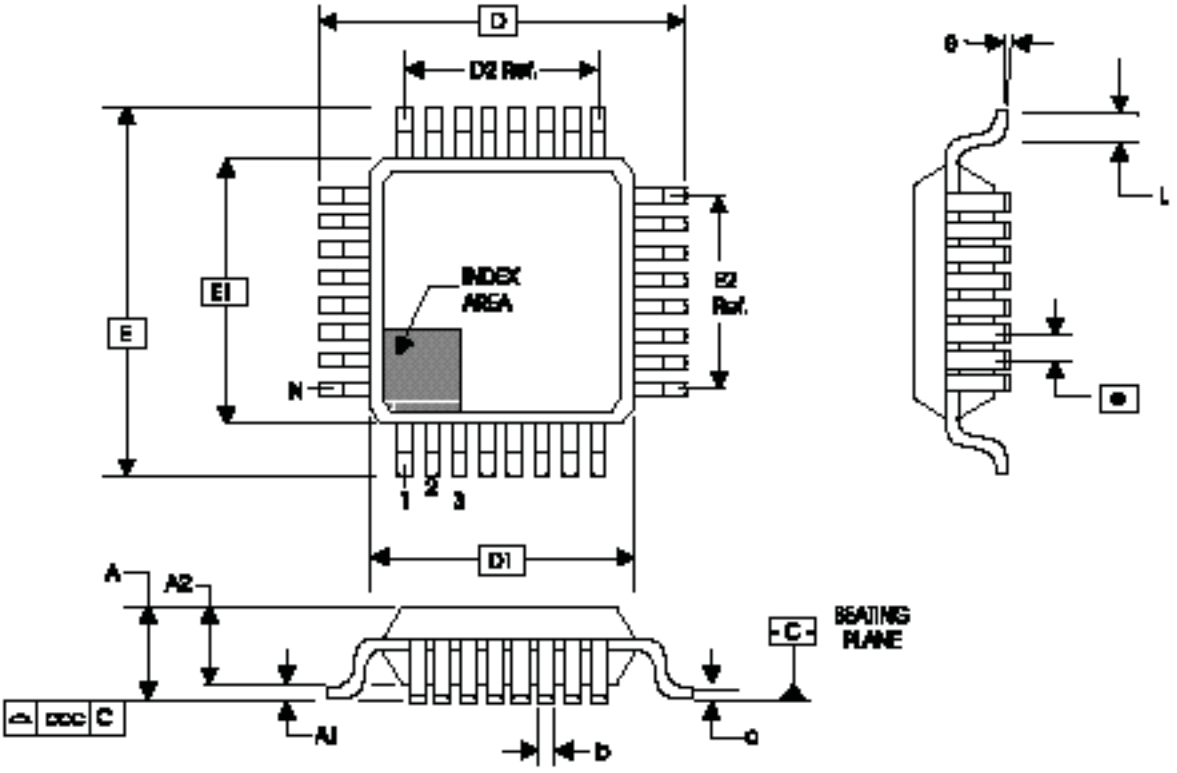
| $\theta_{JA}$ by Velocity (Linear Feet per Minute) | | | |
|---|---|---|---|
| | **0** | **200** | **500** |
| Single-Layer PCB, JEDEC Standard Test Boards | 58.0°C/W | 47.1°C/W | 42.0°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 42.3°C/W | 36.4°C/W | 34.0°C/W |

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

**TRANSISTOR COUNT**

The transistor count for 873991 is: 5788

## Package Outline - Y Suffix for 52 Lead LQFP




### Table 9. Package Dimensions

| JEDEC VARIATION<br>ALL DIMENSIONS IN MILLIMETERS | | | |
|---|---|---|---|
| SYMBOL | BCC | | |
| | MINIMUM | NOMINAL | MAXIMUM |
| N | | 52 | |
| A | -- | -- | 1.60 |
| A1 | 0.05 | -- | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| b | 0.22 | 0.32 | 0.38 |
| c | 0.09 | -- | 0.20 |
| D | | 12.00 BASIC | |
| D1 | | 10.00 BASIC | |
| E | | 12.00 BASIC | |
| E1 | | 10.00 BASIC | |
| e | | 0.65 BASIC | |
| L | 0.45 | -- | 0.75 |
| θ | 0° | -- | 7° |
| ccc | -- | -- | 0.08 |

Reference Document: JEDEC Publication 95, MS-026

**TABLE 10. ORDERING INFORMATION**

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|---|---|---|---|---|
| 873991AYLF | ICS873991AYLF | 52 Lead “Lead-Free” LQFP | tray | 0°C to 70°C |
| 873991AYLFT | ICS873991AYLF | 52 Lead “Lead-Free” LQFP | tape & reel | 0°C to 70°C |

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

| REVISION HISTORY SHEET | | | | |
|---|---|---|---|---|
| **Rev** | **Table** | **Page** | **Description of Change** | **Date** |
| A | T10 | 1<br>16 | Features Section - added Lead-Free bullet.<br>Ordering Information Table - added Lead-Free part number and note. | 6/13/05 |
| A | T10 | 16<br>18 | Updated datasheet's header/footer with IDT from ICS.<br>Removed ICS prefix from Part/Order Number column. Added LF marking.<br>Added Contact Page. | 7/25/10 |
| A | | | Product Discontinuation Notice - Last time buy expires August 14, 2016.<br>PDN CQ-15-04 | 8/25/15 |
| | | | | |

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