PRODUCT DISCONTINUATION NOTICE - LAST TIME BUY EXPIRES SEPTEMBER 7, 2016

DATA SHEET

General Description

The 874003DI-02 is a high performance Dif-ferential-to-LVDS Jitter Attenuator designed for use in PCI Express™ systems. In some PCI Express systems, such as those found in desktop PCs, the PCI Express clocks are generated from a low bandwidth, high phase noise PLL frequency synthesizer. In these systems, a jitter attenuator may be required to attenuate high frequency random and deterministic jitter components from the PLL synthesizer and from the system board. The 874003DI-02 has a bandwidth of 3MHz. The 3MHz provides an intermediate bandwidth that can easily track triangular spread profiles, while providing good jitter attenuation. The 874003DI-02 uses IDT's 3rd Generation FemtoClock™ PLL technology to achieve the lowest possible phase noise. The device is packaged in a 20 Lead TSSOP package, making it ideal for use in space constrained applications such as PCI Express add-in cards.

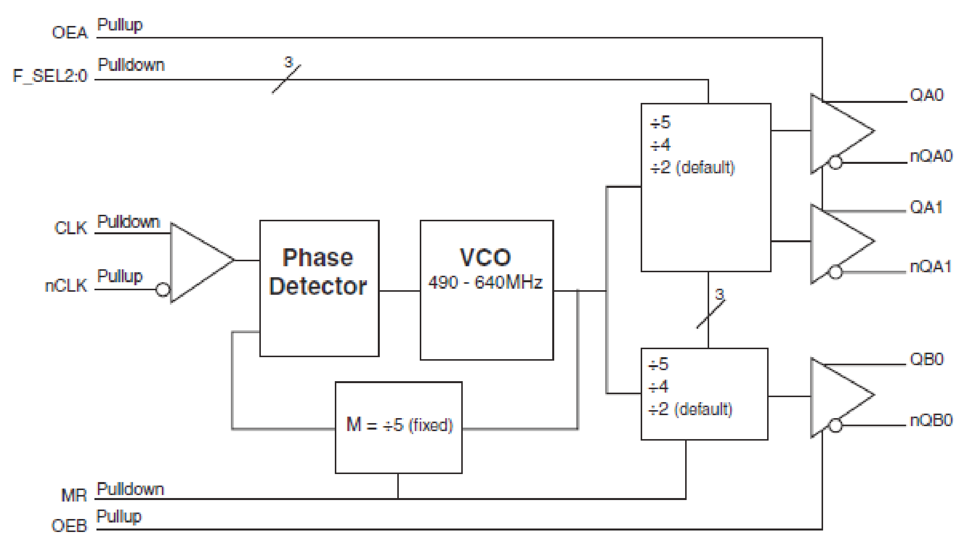
Features

- Three differential LVDS output pairs
- One differential clock input
- CLK and nCLK supports the following input types: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Output frequency range: 98MHz - 320MHz
- Input frequency range: 98MHz - 128MHz
- VCO range: 490MHz - 640MHz
- Cycle-to-cycle jitter: 30ps (maximum)
- Supports PCI-Express Spread-Spectrum Clocking
- 3MHz PLL loop bandwidth
- 3.3V operating supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

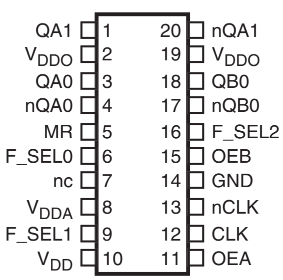
F_SEL[2:0] Function Table

Inputs			Outputs	
F_SEL2	F_SEL1	F_SEL0	QA0, nQA0:QA1, nQA1	QB0, nQB0
0	0	0	÷2 (default)	÷2 (default)
1	0	0	÷5	÷2
0	1	0	÷4	÷2
1	1	0	÷2	÷4
0	0	1	÷2	÷5
1	0	1	÷5	÷4
0	1	1	÷4	÷5
1	1	1	÷4	÷4

Block Diagram



Pin Assignment



874003DI-02
20-Lead TSSOP
6.5mm x 4.4mm x 0.92mm package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 20	QA1, nQA1	Output		Differential output pair. LVDS interface levels.
2, 19	V_{DDO}	Power		Output supply pins.
3, 4	QA0, nQA0	Output		Differential output pair. LVDS interface levels.
5	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs (Qx) to go low and the inverted outputs (nQx) to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
6, 9, 16	F_SEL0, F_SEL1, F_SEL2	Input	Pulldown	Frequency select pin for QAx/nQAx and QB0/nQB0 outputs. LVCMOS/LVTTL interface levels.
7	nc	Unused		No connect.
8	V_{DDA}	Power		Analog supply pin.
10	V_{DD}	Power		Core supply pin.
11	OEA	Input	Pullup	Output enable pin for QA pins. When HIGH, the QAx/nQAx outputs are active. When LOW, the QAx/nQAx outputs are in a high impedance state. LVCMOS/LVTTL interface levels.
12	CLK	Input	Pulldown	Non-inverting differential clock input.
13	nCLK	Input	Pullup	Inverting differential clock input.
14	GND	Power		Power supply ground.
15	OEB	Input	Pullup	Output enable pin for QB0 pins. When HIGH, the QB0/nQB0 outputs are active. When LOW, the QB0/nQB0 outputs are in a high impedance state. LVCMOS/LVTTL interface levels.
17, 18	nQB0, QB0	Output		Differential output pair. LVDS interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Table 3A. OEA Output Enable Function Table

Inputs	Outputs
OEA	**QA0/nQA0, QA1/nQA1**
0	High Impedance
1	Enabled

Table 3B. OEB Output Enable Function Table

Inputs	Outputs
OEB	**QB0/nQB0**
0	High Impedance
1	Enabled

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	73.2°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO}$ = 3.3V±5%, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.15	3.3	V_{DD}	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				80	mA
I_{DDA}	Analog Supply Current				15	mA
I_{DDO}	Output Supply Current				75	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{DD} = V_{DDO}$ = 3.3V±5%, TA = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	OEA, OEB	$V_{DD} = V_{IN}$ = 3.465V			5	µA
		F_SEL0, F_SEL1 F_SEL2, MR	$V_{DD} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	OEA, OEB	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
		F_SEL0, F_SEL1 F_SEL2, MR	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA

Table 4C. Differential DC Characteristics, $V_{DD} = V_{DDO}$ = 3.3V±5%, TA = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		nCLK	$V_{DD} = V_{IN}$ = 3.465V	5			µA
I_{IL}	Input Low Current	CLK	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		nCLK	$V_{DD} = V_{IN}$ = 3.465V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 4D. LVDS DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40°C$ TO $85°C$

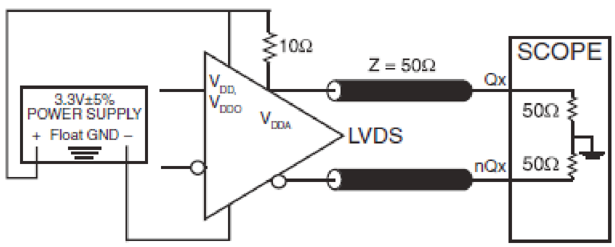
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		275	375	485	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.2	1.35	1.5	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

TABLE 5. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40°C$ TO $85°C$

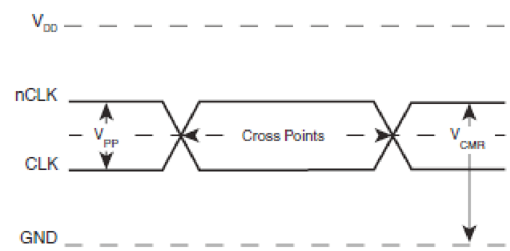
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency			98		320	MHz
*t*jit(cc)	Cycle-to-Cycle Jitter, NOTE 1, 3					30	ps
*t*sk(o)	Output Skew; NOTE 2					185	ps
*t*sk(b)	Bank Skew; NOTE 1, 4	Bank A				65	ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	250		700	ps
odc	Output Duty Cycle			47		53	%

T_A, Ambient Temperature applied using forced air flow.
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 2: These parameters are guaranteed by characterization. Not tested in production.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at the differential cross points.
NOTE 4: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.

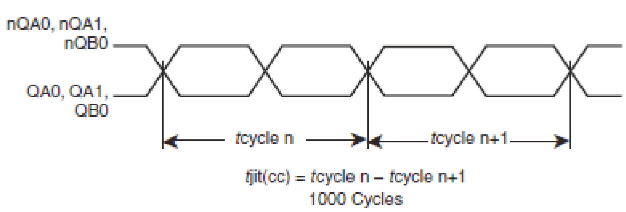
Parameter Measurement Information



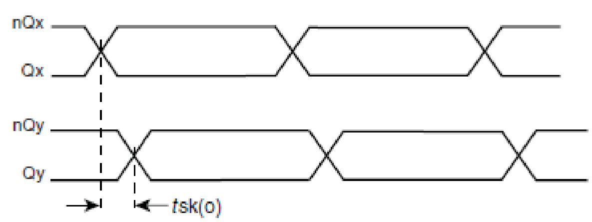
3.3V LVDS Output Load AC Test Circuit



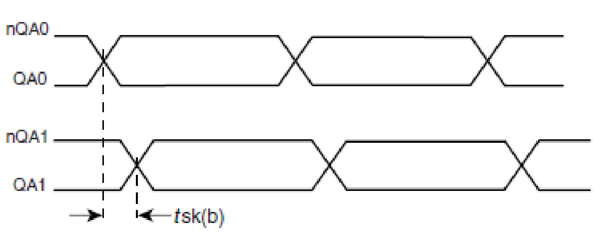
Differential Input Level



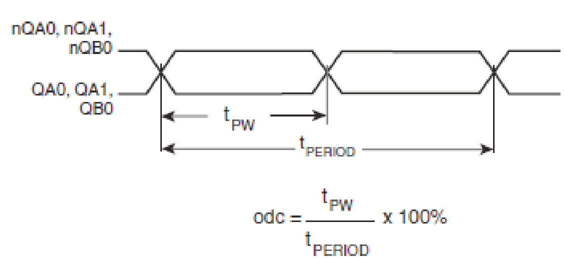
Cycle-to-Cycle Jitter



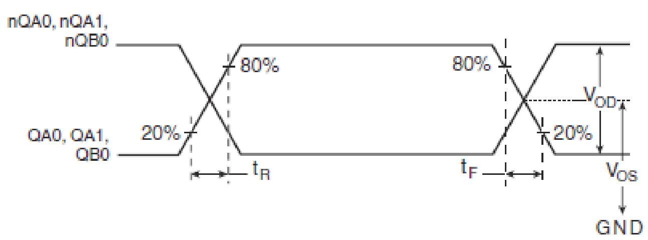
Output Skew



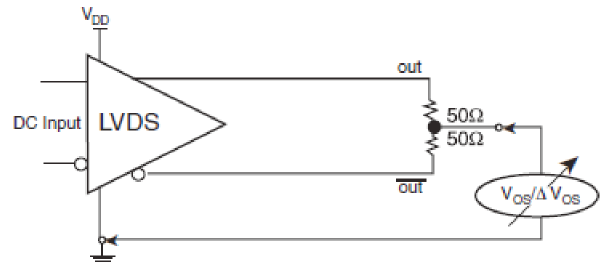
Bank Skew



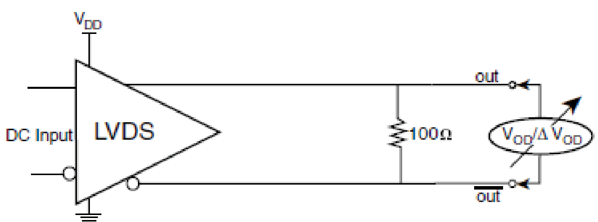
Output Duty Cycle/Pulse Width/Period



OUTPUT RISE/FALL TIME



OFFSET VOLTAGE SETUP



DIFFERENTIAL OUTPUT VOLTAGE SETUP

Application Information

Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 874003DI-02 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, and V_{DDO} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

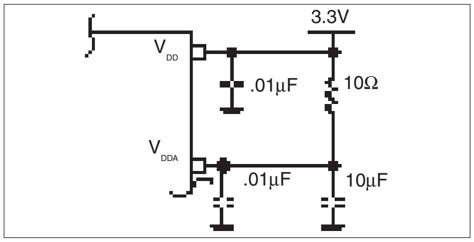


Figure 1. Power Supply Filtering

Wiring the Differential Input to Accept Single Ended Levels

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

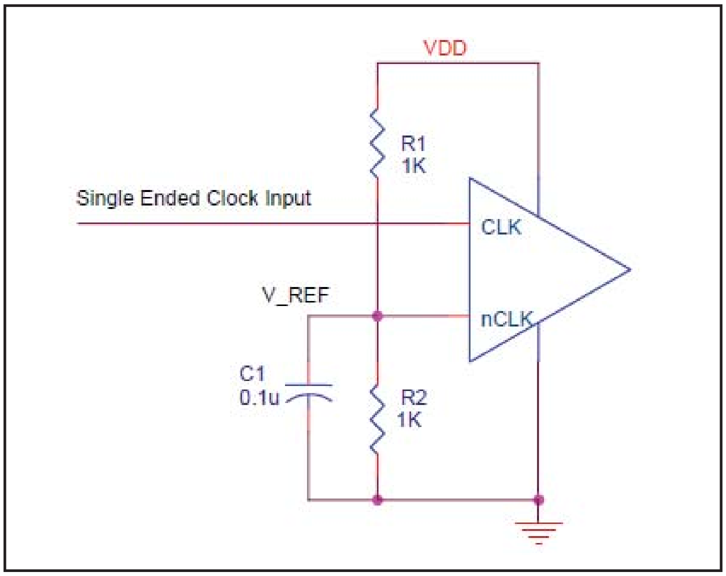


Figure 2. Single Ended Signal Driving Differential Input

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3F* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in Figure 3A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

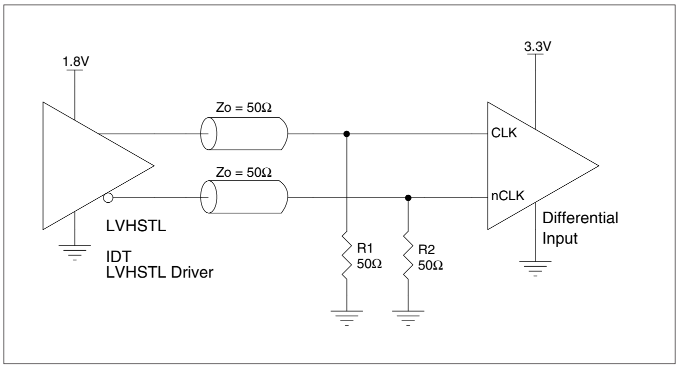


Figure 3A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

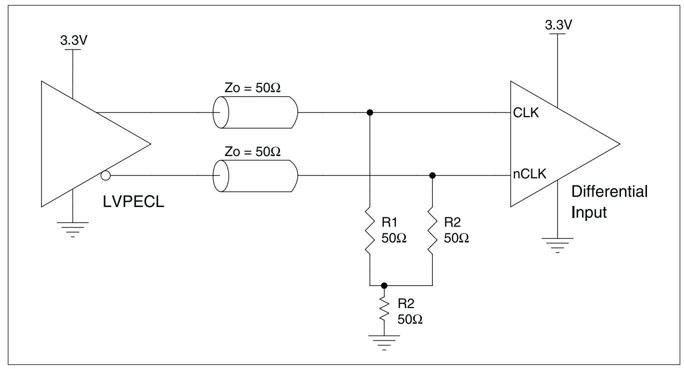


Figure 3B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

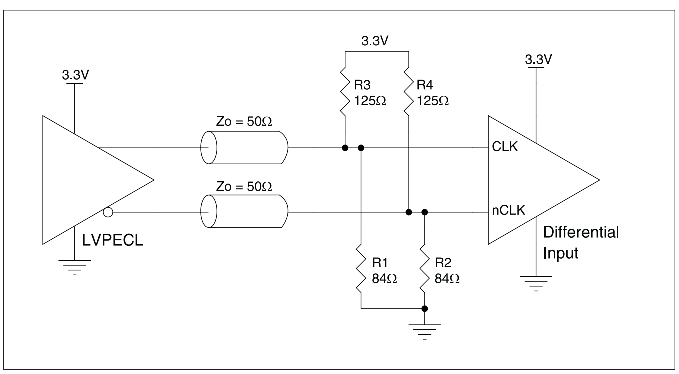


Figure 3C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

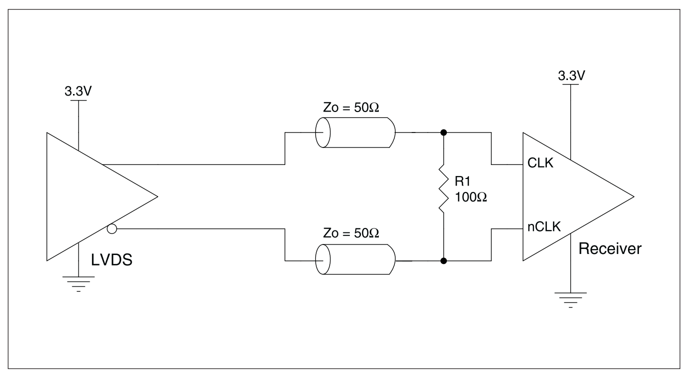


Figure 3D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

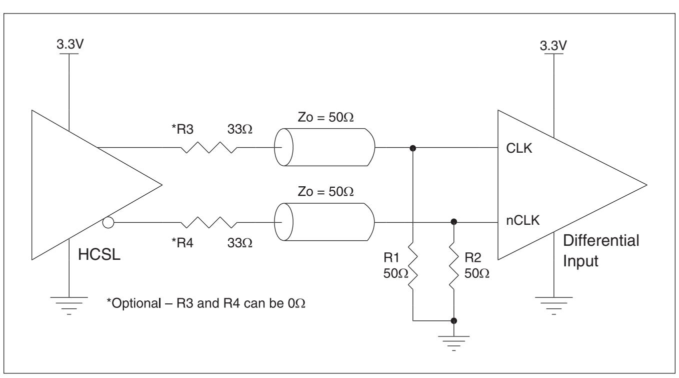


Figure 3E. CLK/nCLK Input Driven by a 3.3V HCSL Driver

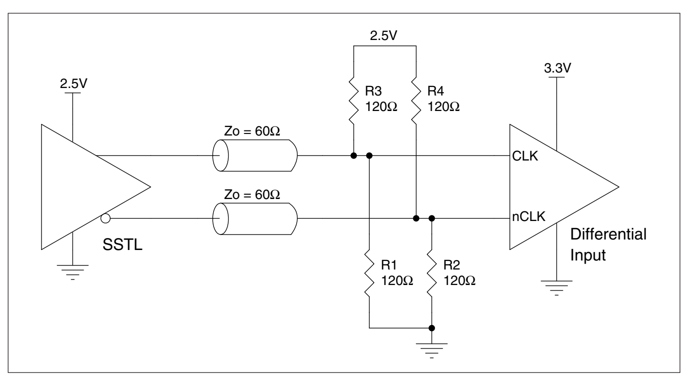


Figure 3F. CLK/nCLK Input Driven by a 2.5V SSTL Driver

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

LVDS Driver Termination

A general LVDS inteface is shown in *Figure 4.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

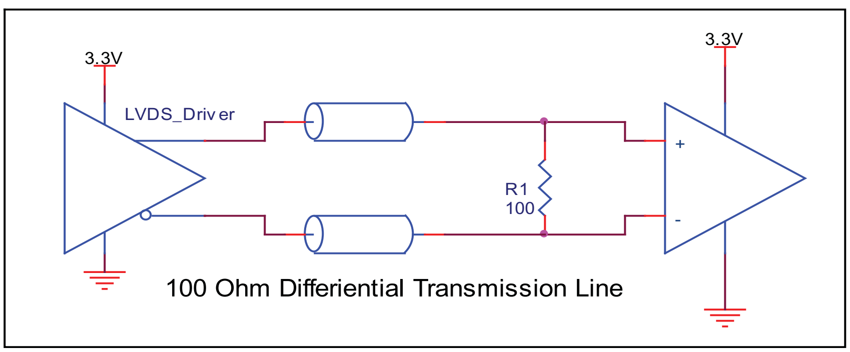


Figure 4. Typical LVDS Driver Termination

Schematic Example

Figure 5 shows an example of 874003DI-02 application schematic. In this example, the device is operated at $V_{DD} = V_{DDO} = 3.3V$. The decoupling capacitors should be located as close as possible to the power pin. The input is driven by a 3.3V LVPECL driver. Two examples of LVDS terminations are shown in this schematic.

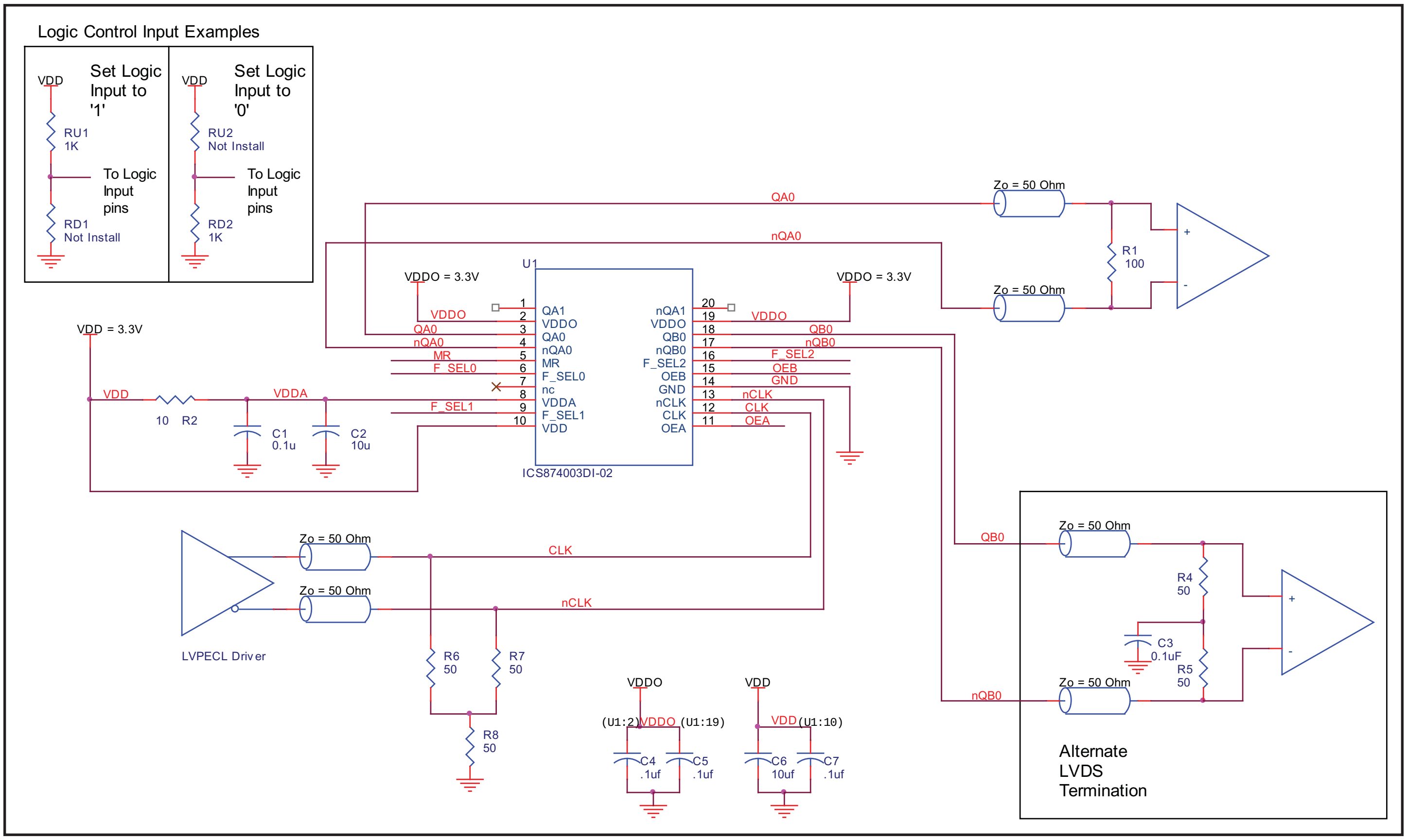


Figure 5. 874003DI-02 Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the 874003DI-02.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 874003DI-02 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power (core)$_{MAX}$ = V_{DD_MAX} * (I_{DD_MAX} + I_{DDA_MAX}) = 3.465V * (80mA + 15mA) = **329.175mW**
- Power (outputs)$_{MAX}$ = V_{DDO_MAX} * I_{DDO_MAX} = 3.465V * 75mA = **259.87mW**

Total Power $_{\_MAX}$ = 329.2mW + 259.9mW = **589.1mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.589W * 66.6°C/W = 124.2°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

Table 6. Thermal Resistance θ_{JA} for 20-Lead TSSOP, Forced Convection

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 20 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for 874003DI-02 is: 1408

Package Outline - G Suffix for 20 Lead TSSOP

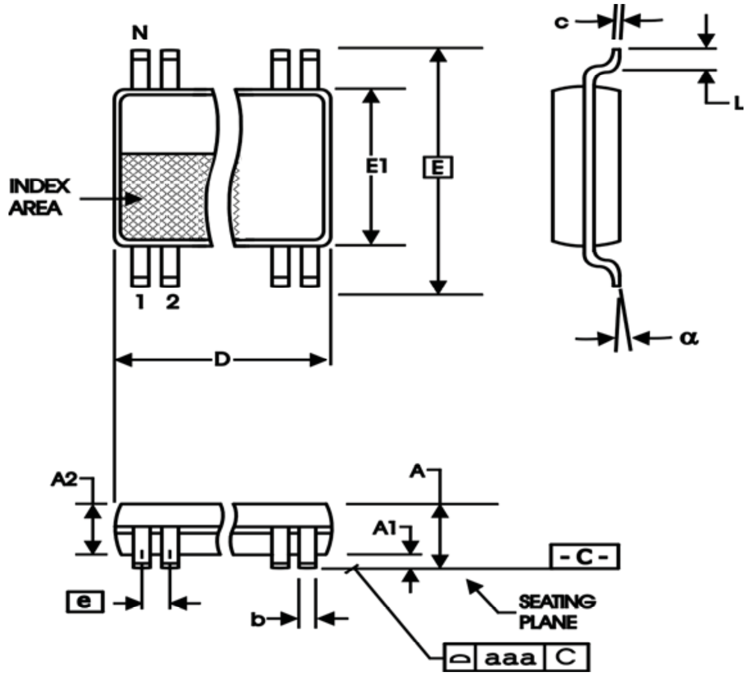


Table 7. Package Dimensions

SYMBOL	Millimeters	
	MIN	MAX
N	20	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
874003DGI-02LF	ICS4003DI02L	20 Lead “Lead-Free” TSSOP	tube	-40°C to 85°C
874003DGI-02LFT	ICS4003DI02L	20 Lead “Lead-Free” TSSOP	tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS complaint.

Revision History

Rev	Table	Page	Description of Change	Date
A	Funtion T	1 1 8	Corrected typo ‘QA0, nQA0:QA1, nQA1’. Removed HiPerClockS logo. Removed HiPerClockS references from drawings.	5/1/13
A	T8	14	Ordering Information - removed leaded devices. Updated data sheet format.	7/17/15
A		1	Product Discontinuation Notice - Last time buy expires September 7, 2016. PDN N-16-02.	3/11/16

Corporate Headquarters

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Contact Information

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