

**PRODUCT DISCONTINUATION NOTICE - LAST TIME BUY EXPIRES MAY 6, 2017**

**General Description**

The 87946I-01 is a low skew, ÷1, ÷2 Fanout Buffer. The 87946I-01 has one LVPECL clock input pair. The PCLK/nPCLK pair can accept LVPECL, CML, or SSTL input levels. The low impedance LVCMOS/LVTTL outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 10 to 20 by utilizing the ability of the outputs to drive two series terminated lines.

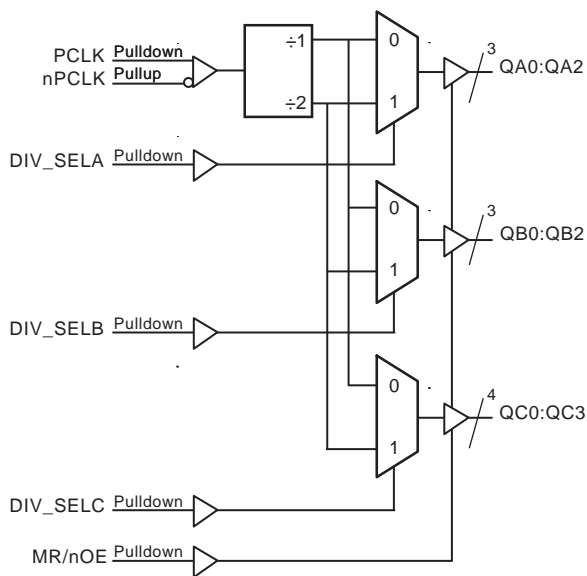
The divide select inputs, DIV\_SELx, control the output frequency of each bank. The outputs can be utilized in the ÷1, ÷2 or a combination of ÷1 and ÷2 modes. The master reset input, MR/nOE, resets the internal frequency dividers and also controls the active and high impedance states of all outputs.

The 87946I-01 is characterized at 3.3V core/3.3V output and 3.3V core/2.5V output. Guaranteed bank, output and part-to-part skew characteristics make the 87946I-01 ideal for those clock distribution applications demanding well defined performance and repeatability.

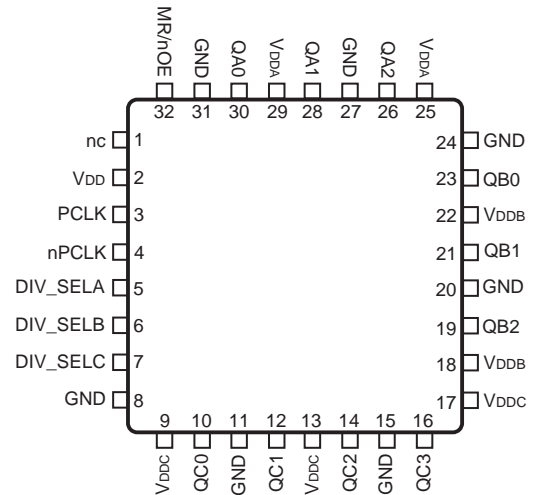
**Features**

- Ten single ended LVCMOS/LVTTL outputs, 7Ω typical output impedance
- LVPECL clock input pair
- PCLK/nPCLK supports the following input levels: LVPECL, CML, SSTL
- Maximum input frequency: 250MHz
- Output skew: 120ps (maximum)
- Part-to-part skew: 700ps (maximum)
- Multiple frequency skew: 320ps (maximum)
- Additive phase jitter, RMS: 0.19ps (typical)
- 3.3V core, 3.3V or 2.5V output supply modes -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package
- **For functional replacement use 87946i-147**

**Block Diagram**



**Pin Assignment**



**87946I-01**  
32-Lead LQFP  
7mm x 7mm x 1.45mm package body  
Y Package  
Top View

**Table 1. Pin Descriptions**

Number	Name	Type		Description
1	nc	Unused		No connect.
2	V <sub>DD</sub>	Power		Power supply pin.
3	PCLK	Input	Pulldown	Non-inverting differential LVPECL clock input.
4	nPCLK	Input	Pullup	Inverting differential LVPECL clock input.
5	DIV_SELA	Input	Pulldown	Controls frequency division for Bank A outputs. See Table 3 LVCMOS/LVTTL interface levels.
6	DIV_SELB	Input	Pulldown	Controls frequency division for Bank B outputs. See Table 3. LVCMOS/LVTTL interface levels.
7	DIV_SELC	Input	Pulldown	Controls frequency division for Bank C outputs. See Table 3. LVCMOS/LVTTL interface levels.
8, 11, 15, 20, 24, 27, 31	GND	Power		Power supply ground.
9, 13, 17	V <sub>DDB</sub>	Power		Output supply pins for Bank C outputs.
10, 12, 14, 16	QC0, QC1, QC2, QC3	Output		Single-ended Bank C clock outputs. LVCMOS/LVTTL interface levels. 7Ω typical output impedance.
18, 22	V <sub>DDA</sub>	Power		Output supply pins for Bank B outputs.
19, 21, 23	QB2, QB1, QB0	Output		Single-ended Bank B clock outputs. LVCMOS/LVTTL interface levels. 7Ω typical output impedance.
25, 29	V <sub>DDC</sub>	Power		Output supply pins for Bank A outputs.
26, 28, 30	QA2, QA1, QA0	Output		Single-ended Bank A clock outputs. LVCMOS/LVTTL interface levels. 7Ω typical output impedance.
32	MR/nOE	Input	Pulldown	Active HIGH Master Reset. Active LOW Output Enable. When logic HIGH, the internal dividers are reset and the outputs are High-Impedance (Hi-Z). When logic LOW, the internal dividers and the outputs are enabled. See Table 3. LVCMOS/LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
C <sub>PD</sub>	Power Dissipation Capacitance	V <sub>DD</sub> = V <sub>DDA</sub> = V <sub>DDB</sub> = V <sub>DDB</sub> = 3.465V			23	pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ
R <sub>OUT</sub>	Output Impedance		5	7	12	Ω

## Function Tables

Table 3. Clock Input Function Table

Inputs				Outputs		
MR/nOE	DIV_SELA	DIV_SELB	DIV_SELC	QA0:QA2	QB0:QB2	QC0:QC3
1	X	X	X	High-Impedance	High-Impedance	High-Impedance
0	0	X	X	fIN/1	Active	Active
0	1	X	X	fIN/2	Active	Active
0	X	0	X	Active	fIN/1	Active
0	X	1	X	Active	fIN/2	Active
0	X	X	0	Active	Active	fIN/1
0	X	X	1	Active	Active	fIN/2

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5V$
Outputs, $V_O$	-0.5V to $V_{DDx} + 0.5V$
Package Thermal Impedance, $\theta_{JA}$	47.9°C/W (0 lfp/m)
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics,  $V_{DD} = V_{DDA} = V_{DDB} = V_{DDC} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Positive Supply Voltage		3.135	3.3	3.465	V
$V_{DDA}, V_{DDB}, V_{DDC}$	Output Supply Voltage		3.135	3.3	3.465	V
$I_{DD}$	Power Supply Current				54	mA
$I_{DDA}, I_{DDB}, I_{DDC}$	Output Supply Current				23	mA

**Table 4B. Power Supply DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDA} = V_{DDB} = V_{DDC} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Positive Supply Voltage		3.135	3.3	3.465	V
$V_{DDA}$ , $V_{DDB}$ , $V_{DDC}$	Output Supply Voltage		2.375	2.5	2.625	V
$I_{DD}$	Power Supply Current				54	mA
$I_{DDA}$ , $I_{DDB}$ , $I_{DDC}$	Output Supply Current				22	mA

**Table 4C. LVCMOS/LVTTL DC Characteristics,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	$V_{DD} = 3.465V$	2		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage	$V_{DD} = 3.465V$	-0.3		0.8	V
$I_{IH}$	Input High Current	$V_{DD} = V_{IN} = 3.465V$			150	$\mu\text{A}$
$I_{IL}$	Input Low Current	$V_{DD} = 3.465V$ , $V_{IN} = 0V$	-5			$\mu\text{A}$
$V_{OH}$	Output High Voltage; NOTE 1	$V_{DDA} = V_{DDB} = V_{DDC} = 3.465V$	2.6			V
$V_{OL}$	Output Low Voltage; NOTE 1	$V_{DDA} = V_{DDB} = V_{DDC} = 3.465V$ or $2.525V$			0.5	V
$I_{OZL}$	Output Hi-Z Current Low		-5			$\mu\text{A}$
$I_{OZH}$	Output Hi-Z Current High				5	$\mu\text{A}$

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{DDX}/2$ . See Parameter Measurement Information section. *Load Test Circuit diagrams.*

**Table 4D. LVPECL DC Characteristics,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	PCLK	$V_{DD} = V_{IN} = 3.465V$		150	$\mu\text{A}$
		nPCLK	$V_{DD} = V_{IN} = 3.465V$		5	$\mu\text{A}$
$I_{IL}$	Input Low Current	PCLK	$V_{DD} = 3.465V$ , $V_{IN} = 0V$	-5		$\mu\text{A}$
		nPCLK	$V_{DD} = 3.465V$ , $V_{IN} = 0V$	-150		$\mu\text{A}$
$V_{PP}$	Peak-to-Peak Voltage		0.3		1.0	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1		GND + 1.5		$V_{DD}$	V

NOTE 1: Common mode input voltage is defined as  $V_{IH}$ .

## AC Electrical Characteristics

**Table 5A. AC Characteristics,  $V_{DD} = V_{DDA} = V_{DDB} = V_{DDC} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				250	MHz
$t_{PD}$	Propagation Delay; NOTE 1	$f \leq 250\text{MHz}$	2.3	3.1	3.8	ns
$t_{sk}(b)$	Bank Skew; NOTE 2, 7	Measured on rising edge at $V_{DDX}/2$			30	ps
$t_{sk}(o)$	Output Skew; NOTE 3, 7	Measured on rising edge at $V_{DDX}/2$			130	ps
$t_{sk}(w)$	Multiple Frequency Skew; NOTE 4, 7	Measured on rising edge at $V_{DDX}/2$			320	ps
$t_{sk}(pp)$	Part-to-Part Skew; NOTE 5, 7	Measured on rising edge at $V_{DDX}/2$			700	ps
$f_{jit}$	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	125MHz, 12kHz – 20MHz		0.19		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	400		950	ps
odc	Output Duty Cycle		40	50	60	%
$t_{EN}$	Output Enable Time; NOTE 6	$f = 10\text{MHz}$			3	ns
$t_{DIS}$	Output Disable Time; NOTE 6	$f = 10\text{MHz}$			3	ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Measured from the differential input crossing point to  $V_{DDX}/2$  of the output.

NOTE 2: Defined as skew within a bank of outputs at the same supply voltages and with equal load conditions.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDX}/2$ .

NOTE 4: Defined as skew across banks of outputs operating at different frequencies with the same supply voltage and equal load conditions.

NOTE 5: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at  $V_{DDX}/2$ .

NOTE 6: These parameters are guaranteed by characterization. Not tested in production.

NOTE 7: This parameter is defined in accordance with JEDEC Standard 65.

**Table 5B. AC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDA} = V_{DDB} = V_{DDC} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

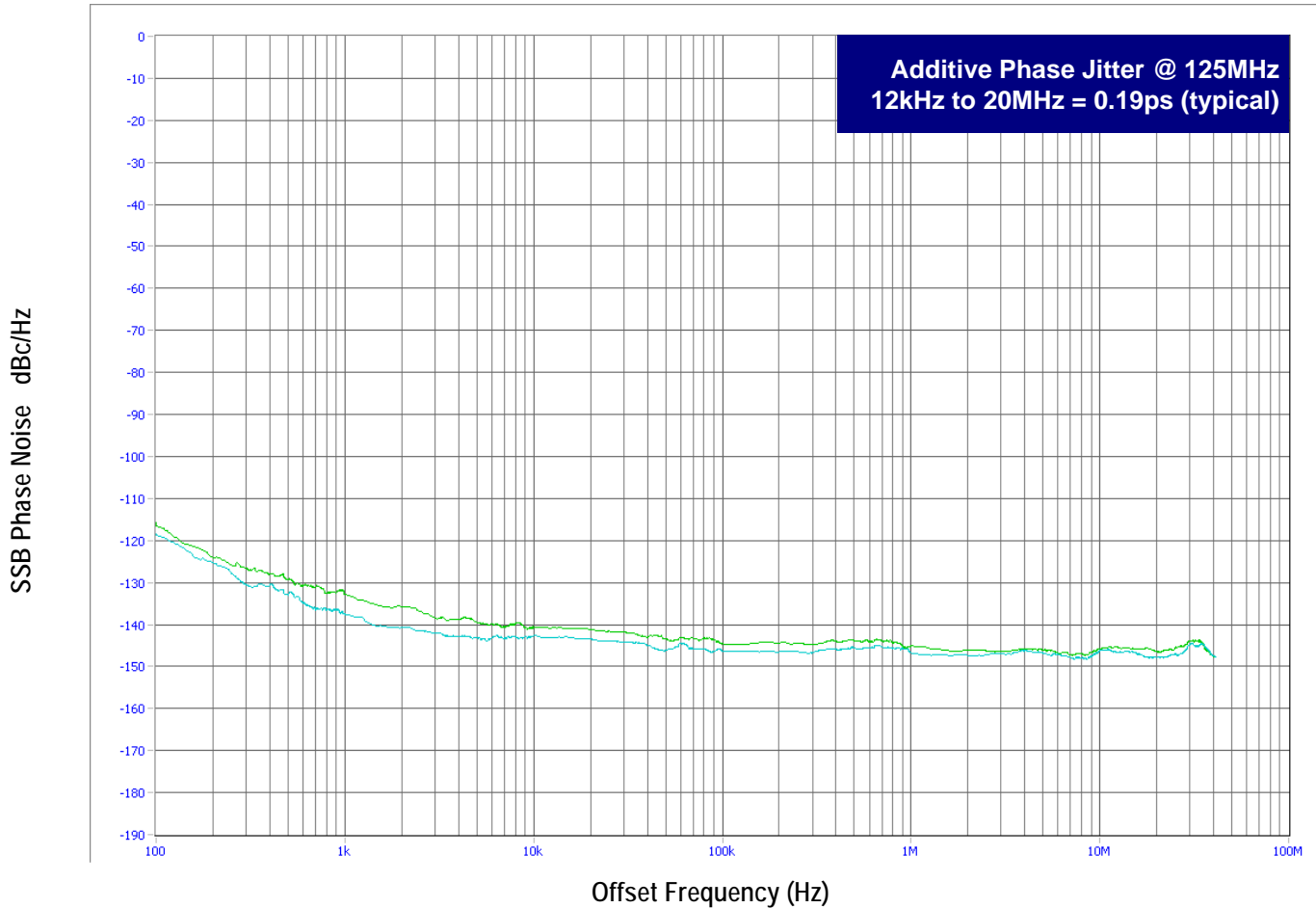
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				250	MHz
$t_{PD}$	Propagation Delay; NOTE 1	$f \leq 250\text{MHz}$	2.5	3.2	3.8	ns
$t_{sk}(b)$	Bank Skew; NOTE 2, 7	Measured on rising edge at $V_{DDX}/2$			35	ps
$t_{sk}(o)$	Output Skew; NOTE 3, 7	Measured on rising edge at $V_{DDX}/2$			120	ps
$t_{sk}(w)$	Multiple Frequency Skew; NOTE 4, 7	Measured on rising edge at $V_{DDX}/2$			325	ps
$t_{sk}(pp)$	Part-to-Part Skew; NOTE 5, 7	Measured on rising edge at $V_{DDX}/2$			700	ps
$f_{jit}$	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	125MHz, 12kHz – 20MHz		0.19		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	350		800	ps
odc	Output Duty Cycle		40	50	57	%
$t_{EN}$	Output Enable Time; NOTE 6	$f = 10\text{MHz}$			3	ns
$t_{DIS}$	Output Disable Time; NOTE 6	$f = 10\text{MHz}$			3	ns

For NOTES, please see Table 5A above.

## Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the *dBc Phase Noise*. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the

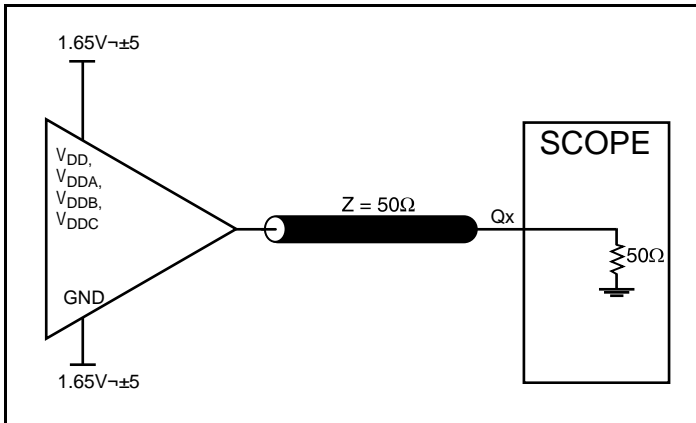
fundamental. When the required offset is specified, the phase noise is called a *dBc* value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



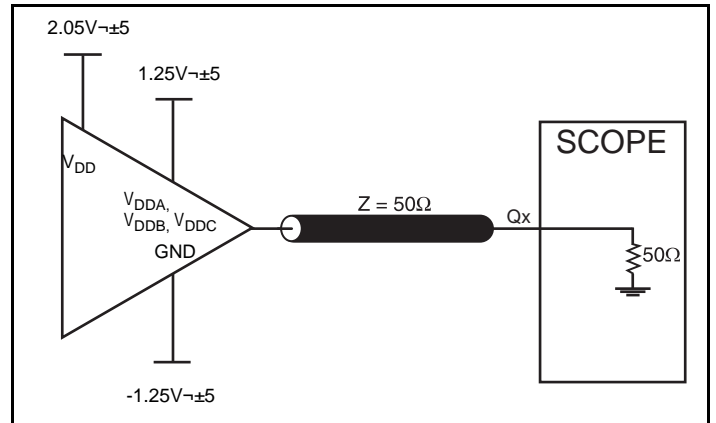
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device.

This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

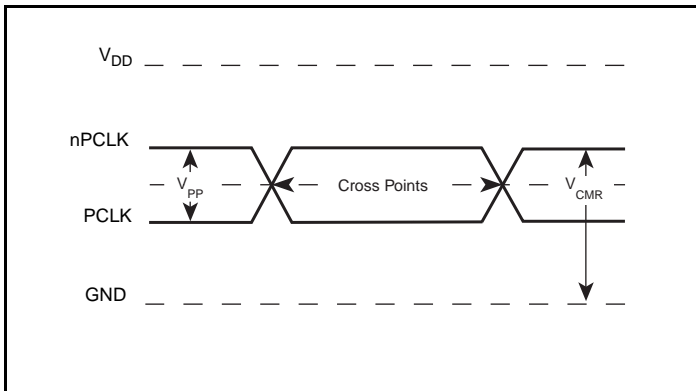
## Parameter Measurement Information



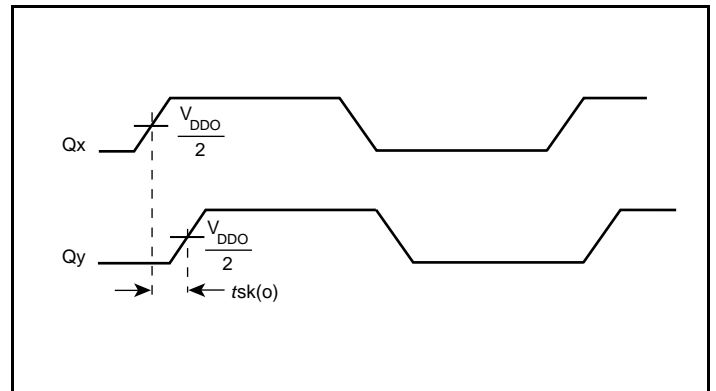
3.3V Output Load AC Test Circuit



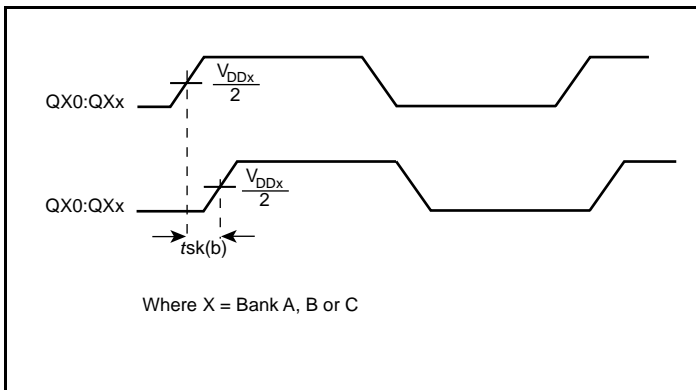
3.3V/2.5V Output Load AC Test Circuit



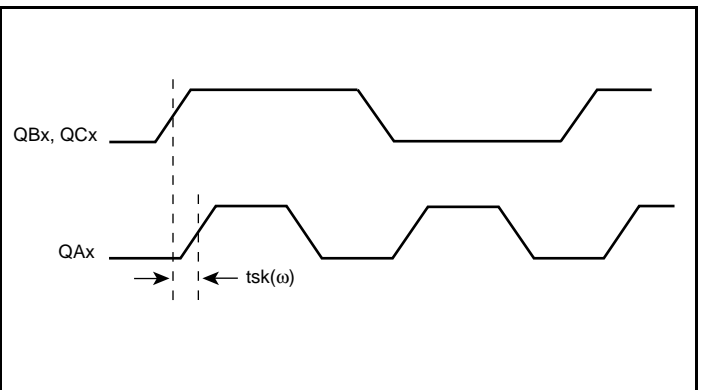
Differential Input Level



Output Skew

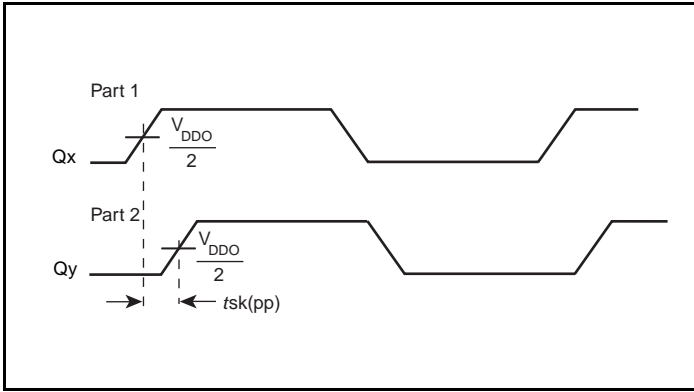


Bank Skew

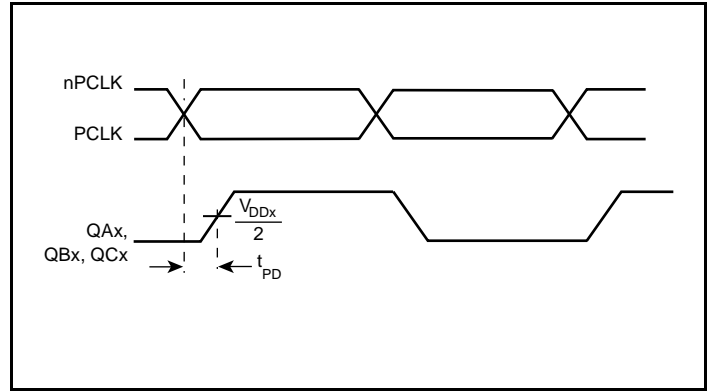


Multiple Frequency Skew

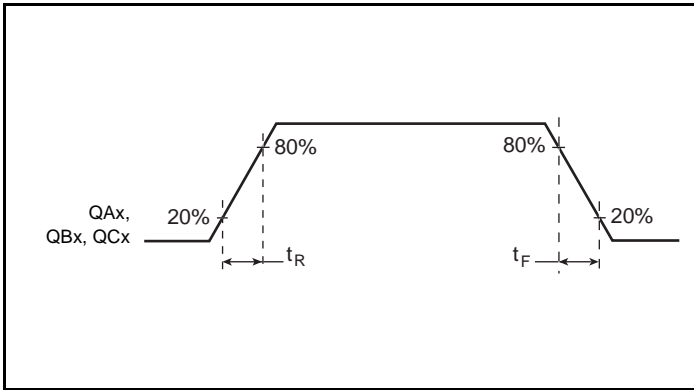
Parameter Measurement Information, continued



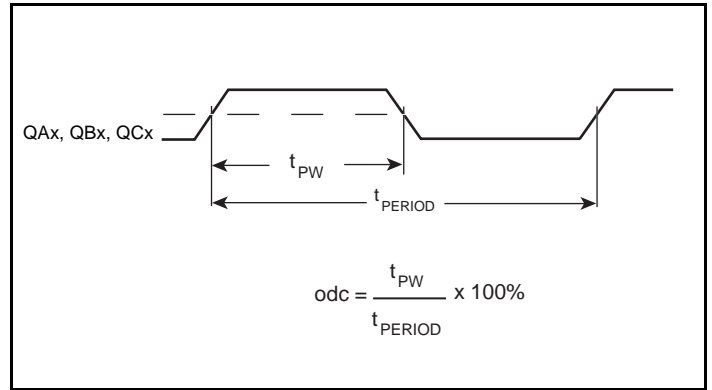
Part-to-Part Skew



Propagation Delay



Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period



## Application Information

### Recommendations for Unused Input and Output Pins

#### Inputs:

##### LVC MOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

#### Outputs:

##### LVC MOS Outputs

All unused LVC MOS output can be left floating. There should be no trace attached.

### Wiring the Differential Input to Accept Single Ended Levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{DD}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{DD} = 3.3V$ ,  $V_{REF}$  should be 1.25V and  $R2/R1 = 0.609$ .

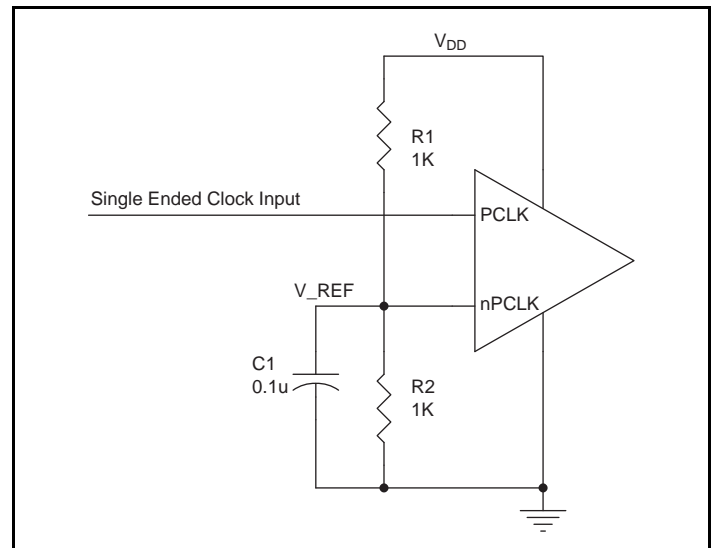
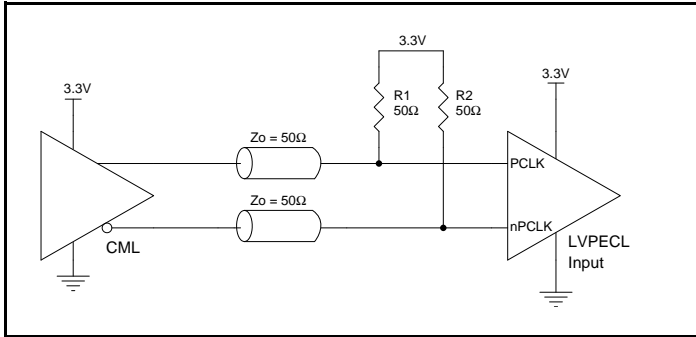


Figure 1. Single-Ended Signal Driving Differential Input

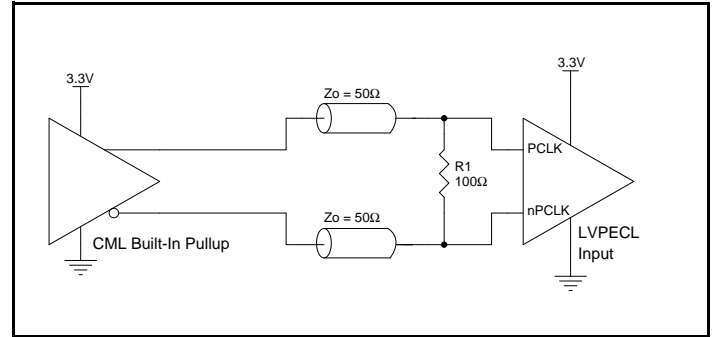
## LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. The differential signal must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 2A to 2E show interface examples for the PCLK/nPCLK input driven by the most common driver types.

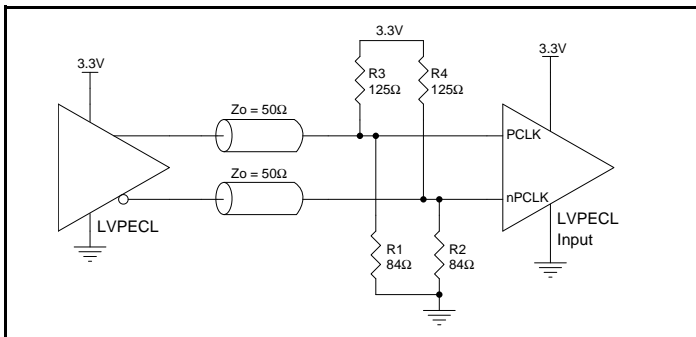
The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.



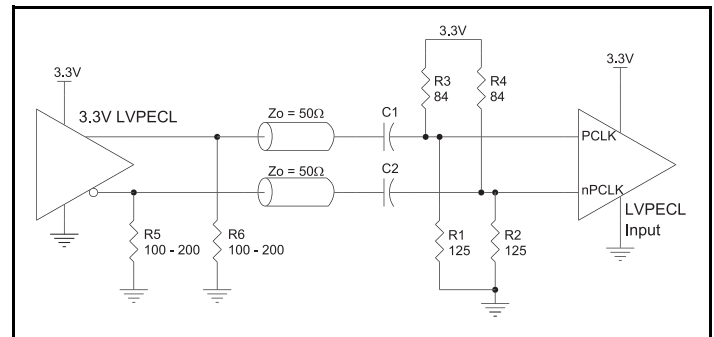
**Figure 2A. PCLK/nPCLK Input Driven by a CML Driver**



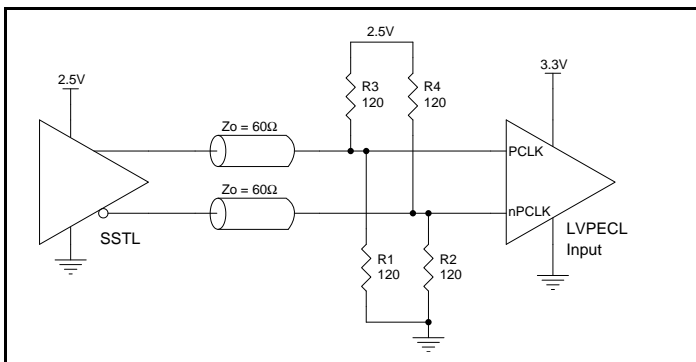
**Figure 2B. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver**



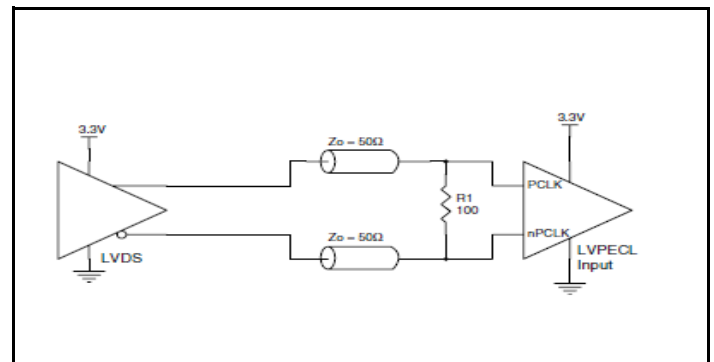
**Figure 2C. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver**



**Figure 2D. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple**



**Figure 2E. PCLK/nPCLK Input Driven by an SSTL Driver**



**Figure 2F. PCLK/nPCLK Input Driven by a 3.3V LVDS Driver**

## Reliability Information

**Table 6.  $\theta_{JA}$  vs. Air Flow Table for a 32 Lead LQFP**

$\theta_{JA}$ vs. Air Flow			
Linear Feet per Minute	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

## Transistor Count

The transistor count for 87946I-01 is: 1204

## Package Outline and Package Dimension

### Package Outline - Y Suffix for 32 Lead LQFP

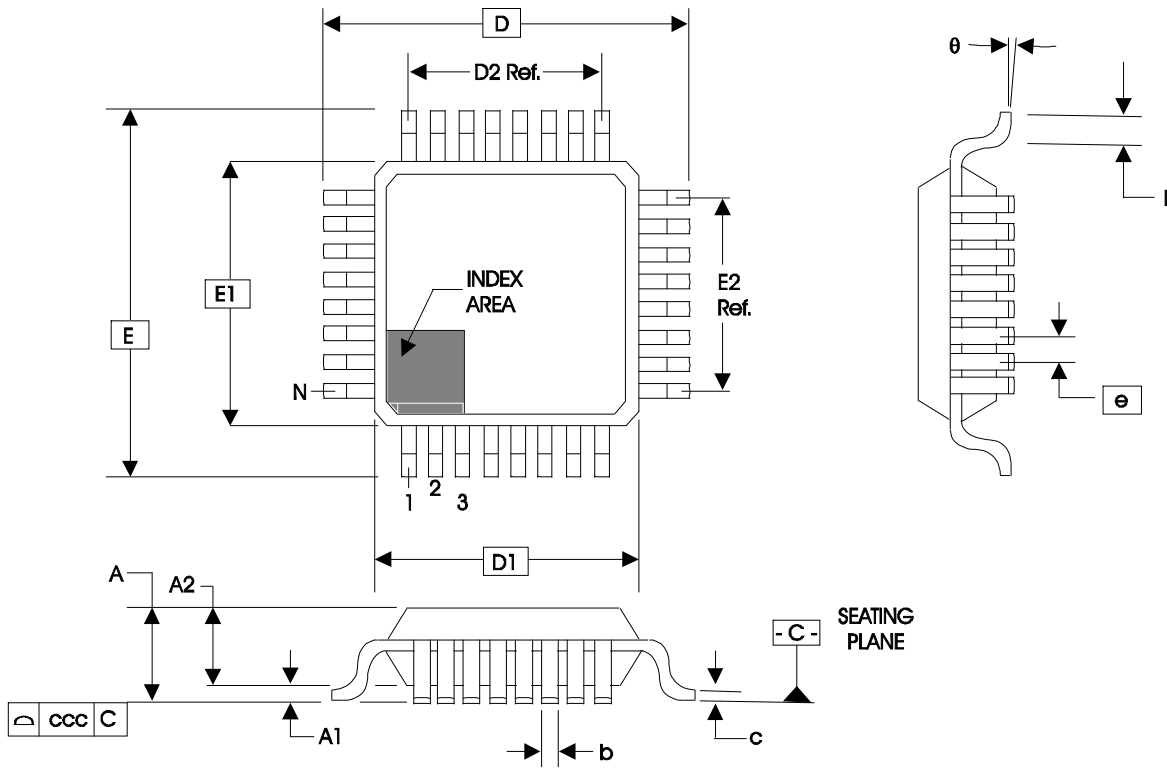


Table 7. Package Dimensions for 32 Lead LQFP

JEDEC Variation: BBC - HD			
All Dimensions in Millimeters			
Symbol	Minimum	Nominal	Maximum
<b>N</b>	32		
<b>A</b>			1.60
<b>A1</b>	0.05	0.10	0.15
<b>A2</b>	1.35	1.40	1.45
<b>b</b>	0.30	0.37	0.45
<b>c</b>	0.09		0.20
<b>D &amp; E</b>	9.00 Basic		
<b>D1 &amp; E1</b>	7.00 Basic		
<b>D2 &amp; E2</b>	5.60 Ref.		
<b>e</b>	0.80 Basic		
<b>L</b>	0.45	0.60	0.75
<b>θ</b>	0°		7°
<b>ccc</b>			0.10

Reference Document: JEDEC Publication 95, MS-026

## Ordering Information

**Table 8. Ordering Information**

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
87946AYI-01LF	ICS7946AI01L	"Lead-Free" 32 Lead LQFP	Tray	-40°C to 85°C
87946AYI-01LFT	ICS7946AI01L	"Lead-Free" 32 Lead LQFP	Tape & Reel	-40°C to 85°C

## Revision History Sheet

Rev	Table	Page	Description of Change	Date
B	T5A & T5B  13	1 5 6 9	Features section added <i>Additive Phase Jitter</i> and <i>Lead-Free</i> bullets AC Characteristics Tables - added Additive Phase Jitter row. Added <i>Additive Phase Jitter</i> section. Application Section - added <i>Recommendations for Unused Input and Output Pins</i> . Ordering Information Table - added lead-free Part/Order Number and Note. Updated format throughout the datasheet.	5/4/07
B	T8	13	Ordering Information Table - added lead-free marking. Updated header/footer of datasheet.	11/10/09
B	T8	13	Ordering Information - removed leaded devices. Updated data sheet format.	7/21/15
B	T8	13	Ordering Information - Deleted LF note below table. Product Discontinuation Notice - Last time buy expires May 6, 2017. PDN CQ-16-01 Updated header and footer.	6/28/16
C		1	Corrected datasheet title. Corrected <i>General Description</i> , first sentence from <i>Clock Generator</i> to <i>Fanout Buffer</i> .	9/20/16



## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit [www.renesas.com/contact-us/](http://www.renesas.com/contact-us/).