Device Overview

The 89HPES12T3G2 is a member of IDT's PRECISE™ family of PCI Express® switching solutions. The PES12T3G2 is a 12-lane, 3-port Gen2 peripheral chip that performs PCI Express Base switching with a feature set optimized for high performance applications such as servers, storage, and communications/networking. It provides connectivity and switching functions between a PCI Express upstream port and two downstream ports and supports switching between downstream ports.

Features

◆ High Performance PCI Express Switch
  – Twelve 5 Gbps Gen2 PCI Express lanes
  – Three switch ports
    • One x4 upstream port
    • Two x4 downstream ports
  – Low latency cut-through switch architecture
  – Support for Max Payload Size up to 2048 bytes
  – One virtual channel
  – Eight traffic classes
  – PCI Express Base Specification Revision 2.0 compliant
◆ Flexible Architecture with Numerous Configuration Options
  – Automatic per port link width negotiation to x4, x2 or x1
  – Automatic lane reversal on all ports
  – Automatic polarity inversion
  – Ability to load device configuration from serial EEPROM

◆ Legacy Support
  – PCI compatible INTx emulation
  – Bus locking
◆ Highly Integrated Solution
  – Incorporates on-chip internal memory for packet buffering and queueing
  – Integrates twelve 5 Gbps embedded SerDes with 8b/10b encoder/decoder (no separate transceivers needed)
    • Receive equalization (RxEQ)
◆ Reliability, Availability, and Serviceability (RAS) Features
  – Internal end-to-end parity protection on all TLPs ensures data integrity even in systems that do not implement end-to-end CRC (ECRC)
  – Supports ECRC and Advanced Error Reporting
  – Supports PCI Express Native Hot-Plug, Hot-Swap capable I/O
  – Compatible with Hot-Plug I/O expanders used on PC motherboards
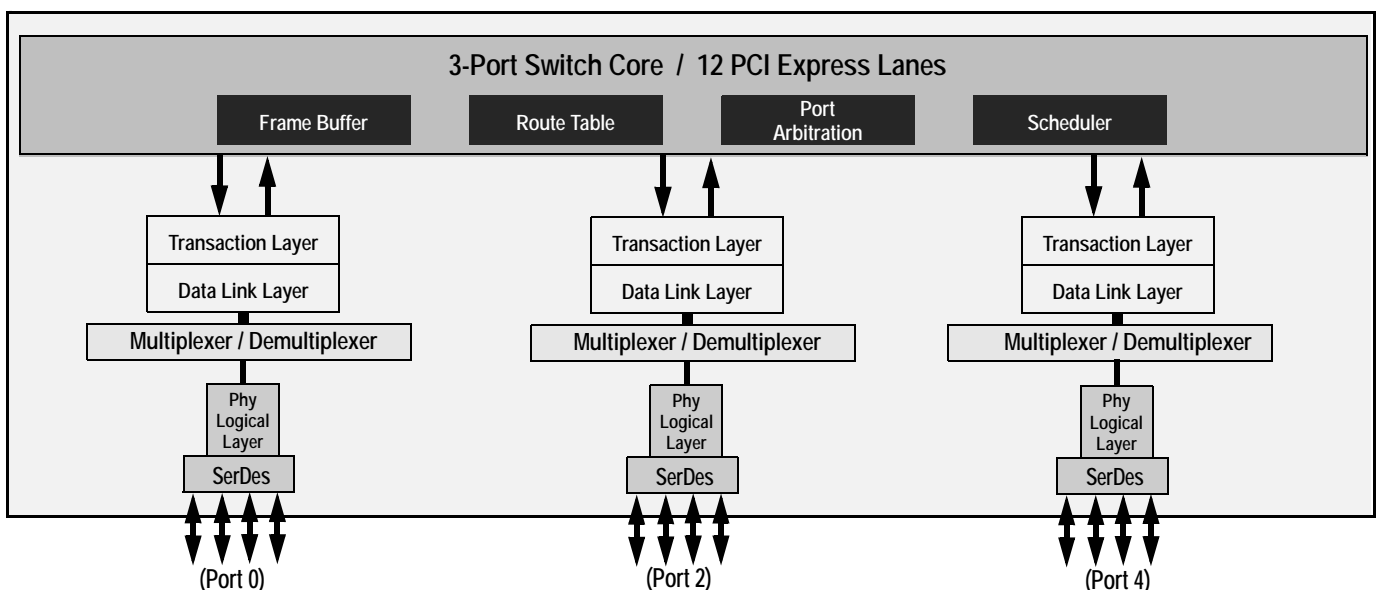 – Supports Hot-Swap

Block Diagram

Figure 1 Internal Block Diagram

DSC 6930

- Power Management
  - *Utilizes advanced low-power design techniques to achieve low typical power consumption*
  - *Support PCI Express Power Management Interface specification (PCI-PM 1.2)*
  - *Supports PCI Express Active State Power Management (ASPM) link state*
  - *Supports PCI Express Power Budgeting Capability*
  - *Supports the optional PCI Express SerDes Transmit Low-Swing Voltage Mode*
  - *Unused SerDes are disabled and can be powered-off.*
- Testability and Debug Features
  - *Built in Pseudo-Random Bit Stream (PRBS) generator*
  - *Numerous SerDes test modes*
  - *Ability to read and write any internal register via the SMBus*
  - *Ability to bypass link training and force any link into any mode*
  - *Provides statistics and performance counters*
- Nine General Purpose Input/Output Pins
  - *Each pin may be individually configured as an input or output*
  - *Each pin may be individually configured as an interrupt input*
  - *Some pins have selectable alternate functions*
- Packaged in a 19mm x 19mm 324-ball BGA with 1mm ball spacing

Product Description

Utilizing standard PCI Express interconnect, the PES12T3G2 provides the most efficient fan-out solution for applications requiring high throughput, low latency, and simple board layout with a minimum number of board layers. It provides 12 GBps (96 Gbps) of aggregated, full-duplex switching capacity through 12 integrated serial lanes, using proven and robust IDT technology. Each lane provides 5 Gbps of bandwidth in both directions and is fully compliant with PCI Express Base Specification, Revision 2.0.

The PES12T3G2 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers in compliance with PCI Express Base specification Revision 2.0. The PES12T3G2 can operate either as a store and forward or cut-through switch and is designed to switch memory and I/O transactions. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management to enable efficient switching and I/O connectivity for servers, storage, and embedded processors with limited connectivity.
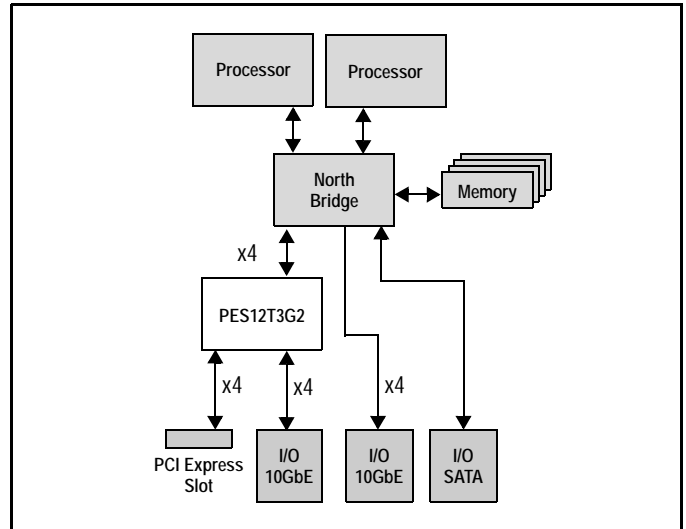

Figure 2 I/O Expansion Application

SMBus Interface

The PES12T3G2 contains two SMBus interfaces. The slave interface provides full access to the configuration registers in the PES12T3G2, allowing every configuration register in the device to be read or written by an external agent. The master interface allows the default configuration register values of the PES12T3G2 to be overridden following a reset with values programmed in an external serial EEPROM. The master interface is also used by an external Hot-Plug I/O expander.

Six pins make up each of the two SMBus interfaces. These pins consist of an SMBus clock pin, an SMBus data pin, and 4 SMBus address pins. In the slave interface, these address pins allow the SMBus address to which the device responds to be configured. In the master interface, these address pins allow the SMBus address of the serial configuration EEPROM from which data is loaded to be configured. The SMBus address is set up on negation of PERSTN by sampling the corresponding address pins. When the pins are sampled, the resulting address is assigned as shown in Table 1.

Bit	Slave SMBus Address	Master SMBus Address
1	SSMBADDR[1]	MSMBADDR[1]
2	SSMBADDR[2]	MSMBADDR[2]
3	SSMBADDR[3]	MSMBADDR[3]
4	0	MSMBADDR[4]
5	SSMBADDR[5]	1
6	1	0
7	1	1

Table 1 Master and Slave SMBus Address Assignment

As shown in Figure 3, the master and slave SMBuses may be used in a unified or split configuration. In the unified configuration, shown in Figure 3(a), the master and slave SMBuses are tied together and the PES12T3G2 acts both as a SMBus master as well as a SMBus slave on this bus. This requires that the SMBus master or processor that has access to PES12T3G2 registers supports SMBus arbitration. In some systems, this SMBus master interface may be implemented using general purpose I/O pins on a processor or micro controller, and may not support SMBus arbitration. To support these systems, the PES12T3G2 may be configured to operate in a split configuration as shown in Figure 3(b).

In the split configuration, the master and slave SMBuses operate as two independent buses and thus multi-master arbitration is never required. The PES12T3G2 supports reading and writing of the serial EEPROM on the master SMBus via the slave SMBus, allowing in system programming of the serial EEPROM.
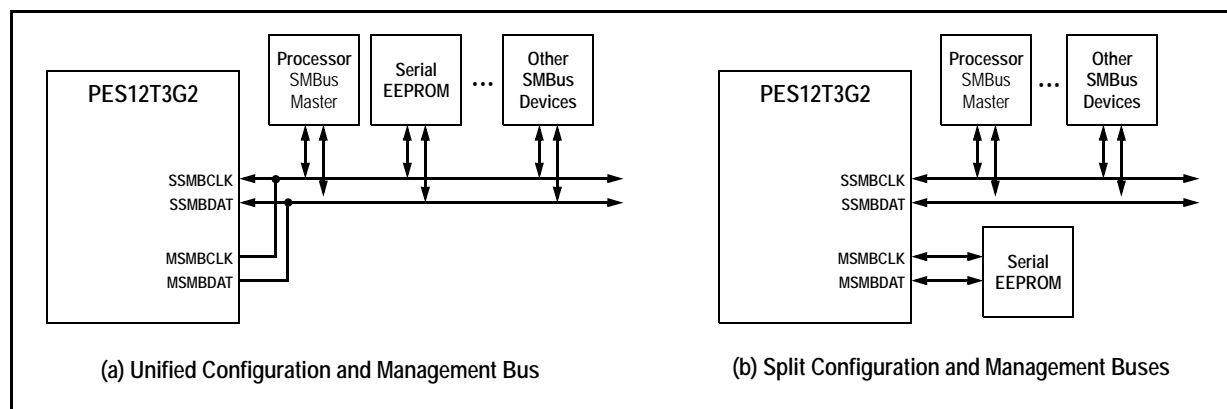
Figure 3 SMBus Interface Configuration Examples

Hot-Plug Interface

The PES12T3G2 supports PCI Express Hot-Plug on each downstream port. To reduce the number of pins required on the device, the PES12T3G2 utilizes an external I/O expander, such as that used on PC motherboards, connected to the SMBus master interface. Following reset and configuration, whenever the state of a Hot-Plug output needs to be modified, the PES12T3G2 generates an SMBus transaction to the I/O expander with the new value of all of the outputs. Whenever a Hot-Plug input changes, the I/O expander generates an interrupt which is received on the IOEXPINTN input pin (alternate function of GPIO) of the PES12T3G2. In response to an I/O expander interrupt, the PES12T3G2 generates an SMBus transaction to read the state of all of the Hot-Plug inputs from the I/O expander.

General Purpose Input/Output

The PES12T3G2 provides 9 General Purpose Input/Output (GPIO) pins that may be used by the system designer as bit I/O ports. Each GPIO pin may be configured independently as an input or output through software control. Some GPIO pins are shared with other on-chip functions. These alternate functions may be enabled via software, SMBus slave interface, or serial configuration EEPROM.

Pin Description

The following tables list the functions of the pins provided on the PES12T3G2. Some of the functions listed may be multiplexed onto the same pin. The active polarity of a signal is defined using a suffix. Signals ending with an "N" are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level.

> **Note:** In the PES12T3G2, the two downstream ports are labeled port 2 and port 4.

Signal	Type	Name/Description
PE0RP[3:0] PE0RN[3:0]	I	**PCI Express Port 0 Serial Data Receive.** Differential PCI Express receive pairs for port 0. Port 0 is the upstream port.
PE0TP[3:0] PE0TN[3:0]	O	**PCI Express Port 0 Serial Data Transmit.** Differential PCI Express transmit pairs for port 0. Port 0 is the upstream port.
PE2RP[3:0] PE2RN[3:0]	I	**PCI Express Port 2 Serial Data Receive.** Differential PCI Express receive pairs for port 2.
PE2TP[3:0] PE2TN[3:0]	O	**PCI Express Port 2 Serial Data Transmit.** Differential PCI Express transmit pairs for port 2.
PE4RP[3:0] PE4RN[3:0]	I	**PCI Express Port 4 Serial Data Receive.** Differential PCI Express receive pairs for port 4.
PE4TP[3:0] PE4TN[3:0]	O	**PCI Express Port 4 Serial Data Transmit.** Differential PCI Express transmit pairs for port 4.
PEREFCLKP[0] PEREFCLKN[0]	I	**PCI Express Reference Clock.** Differential reference clock pair input. This clock is used as the reference clock by on-chip PLLs to generate the clocks required for the system logic and on-chip SerDes. The frequency of the differential reference clock is determined by the REFCLKM signal.
REFCLKM	I	**PCI Express Reference Clock Mode Select.** This signal selects the frequency of the reference clock input. 0x0 - 100 MHz 0x1 - 125 MHz This pin should be static and not change following the negation of PERSTN.

Table 2 PCI Express Interface Pins

Signal	Type	Name/Description
MSMBADDR[4:1]	I	**Master SMBus Address.** These pins determine the SMBus address of the serial EEPROM from which configuration information is loaded.
MSMBCLK	I/O	**Master SMBus Clock.** This bidirectional signal is used to synchronize transfers on the master SMBus.
MSMBDAT	I/O	**Master SMBus Data.** This bidirectional signal is used for data on the master SMBus.
SSMBADDR[5,3:1]	I	**Slave SMBus Address.** These pins determine the SMBus address to which the slave SMBus interface responds.
SSMBCLK	I/O	**Slave SMBus Clock.** This bidirectional signal is used to synchronize transfers on the slave SMBus.
SSMBDAT	I/O	**Slave SMBus Data.** This bidirectional signal is used for data on the slave SMBus.

Table 3 SMBus Interface Pins

Signal	Type	Name/Description
GPIO[0]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P2RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 2.
GPIO[1]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P4RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 4.
GPIO[2]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN0 Alternate function pin type: Input Alternate function: I/O expander interrupt 0 input.
GPIO[3]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[4]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN2 Alternate function pin type: Input Alternate function: I/O Expander interrupt 2 input
GPIO[5]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[6]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[7]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: GPEN Alternate function pin type: Output Alternate function: General Purpose Event (GPE) output
GPIO[11]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.

Table 4 General Purpose I/O Pins

Signal	Type	Name/Description
CCLKDS	I	**Common Clock Downstream.** The assertion of this pin indicates that all downstream ports are using the same clock source as that provided to downstream devices.This bit is used as the initial value of the Slot Clock Configuration bit in all of the Link Status Registers for downstream ports. The value may be overridden by modifying the SCLK bit in each downstream port's PCIELSTS register.
CCLKUS	I	**Common Clock Upstream.** The assertion of this pin indicates that the upstream port is using the same clock source as the upstream device. This bit is used as the initial value of the Slot Clock Configuration bit in the Link Status Register for the upstream port. The value may be overridden by modifying the SCLK bit in the P0_PCIELSTS register.
MSMBSMODE	I	**Master SMBus Slow Mode.** The assertion of this pin indicates that the master SMBus should operate at 100 KHz instead of 400 KHz. This value may not be overridden.
PERSTN	I	**Fundamental Reset.** Assertion of this signal resets all logic inside PES12T3G2 and initiates a PCI Express fundamental reset.
RSTHALT	I	**Reset Halt.** When this signal is asserted during a PCI Express fundamental reset, PES12T3G2 executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the SWCTL register by an SMBus master.
SWMODE[2:0]	I	**Switch Mode.** These configuration pins determine the PES12T3G2 switch operating mode. 0x0 - Normal switch mode 0x1 - Normal switch mode with Serial EEPROM initialization 0x2 - through 0x7 Reserved These pins should be static and not change following the negation of PERSTN.

Table 5 System Pins

Signal	Type	Name/Description
JTAG_TCK	I	**JTAG Clock**. This is an input test clock used to clock the shifting of data into or out of the boundary scan logic or JTAG Controller. JTAG_TCK is independent of the system clock with a nominal 50% duty cycle.
JTAG_TDI	I	**JTAG Data Input**. This is the serial data input to the boundary scan logic or JTAG Controller.

Table 6 Test Pins (Part 1 of 2)

Signal	Type	Name/Description
JTAG_TDO	O	**JTAG Data Output**. This is the serial data shifted out from the boundary scan logic or JTAG Controller. When no data is being shifted out, this signal is tri-stated.
JTAG_TMS	I	**JTAG Mode**. The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller.

JTAG_TRST_N	I	**JTAG Reset**. This active low signal asynchronously resets the boundary scan logic and JTAG TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur:
		    1) actively drive this signal low with control logic
		    2) statically drive this signal low with an external pull-down on the board

Table 6 Test Pins (Part 2 of 2)

Signal	Type	Name/Description
REFRES0	I/O	**Port 0 External Reference Resistor.** Provides a reference for the Port 0 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES2	I/O	**Port 2 External Reference Resistor.** Provides a reference for the Port 2 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES4	I/O	**Port 4 External Reference Resistor.** Provides a reference for the Port 4 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
$V_{DD}CORE$	I	**Core V_{DD}.** Power supply for core logic.
$V_{DD}I/O$	I	**I/O V_{DD}.** LVTTL I/O buffer power supply.
$V_{DD}PEA$	I	**PCI Express Analog Power.** Serdes analog power supply (1.0V).
$V_{DD}PEHA$	I	**PCI Express Analog High Power.** Serdes analog power supply (2.5V).
$V_{DD}PETA$	I	**PCI Express Transmitter Analog Voltage.** Serdes transmitter analog power supply (1.0V).
V_{SS}	I	**Ground.**

Table 7 Power, Ground, and SerDes Resistor Pins

Pin Characteristics

Note: Some input pads of the PES12T3G2 do not contain internal pull-ups or pull-downs. Unused inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs which, if left floating, could adversely affect operation. Also, any input pin left floating can cause a slight increase in power consumption.

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor[1]	Notes
PCI Express Interface	PE0RN[3:0]	I	PCIe differential[2]	Serial Link		
	PE0RP[3:0]	I				
	PE0TN[3:0]	O				
	PE0TP[3:0]	O				
	PE2RN[3:0]	I				
	PE2RP[3:0]	I				
	PE2TN[3:0]	O				
	PE2TP[3:0]	O				
	PE4RN[3:0]	I				
	PE4RP[3:0]	I				
	PE4TN[3:0]	O				
	PE4TP[3:0]	O				
	PEREFCLKN[0]	I	HCSL	Diff. Clock Input		Refer to Table 9
	PEREFCLKP[0]	I				
	REFCLKM	I	LVTTL	Input	pull-down	
SMBus	MSMBADDR[4:1]	I	LVTTL	Input	pull-up	
	MSMBCLK	I/O		STI[3]		pull-up on board
	MSMBDAT	I/O		STI		pull-up on board
	SSMBADDR[5,3:1]	I		Input	pull-up	
	SSMBCLK	I/O		STI		pull-up on board
	SSMBDAT	I/O		STI		pull-up on board
General Purpose I/O	GPIO[11,7:0]	I/O	LVTTL	STI, High Drive	pull-up	
System Pins	CCLKDS	I	LVTTL	Input	pull-up	
	CCLKUS	I		Input	pull-up	
	MSMBSMODE	I		Input	pull-down	
	PERSTN	I		STI		
	RSTHALT	I		Input	pull-down	
	SWMODE[2:0]	I		Input	pull-down	
EJTAG / JTAG	JTAG_TCK	I	LVTTL	STI	pull-up	
	JTAG_TDI	I		STI	pull-up	
	JTAG_TDO	O				
	JTAG_TMS	I		STI	pull-up	
	JTAG_TRST_N	I		STI	pull-up	

Table 8 Pin Characteristics (Part 1 of 2)

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor[1]	Notes
SerDes Reference Resistors	REFRES0	I/O	Analog			
	REFRES2	I/O				
	REFRES4	I/O				

Table 8 Pin Characteristics (Part 2 of 2)

[1.] Internal resistor values under typical operating conditions are 92K Ω for pull-up and 90K Ω for pull-down.

[2.] All receiver pins set the DC common mode voltage to ground. All transmitters must be AC coupled to the media.

[3.] Schmitt Trigger Input (STI).
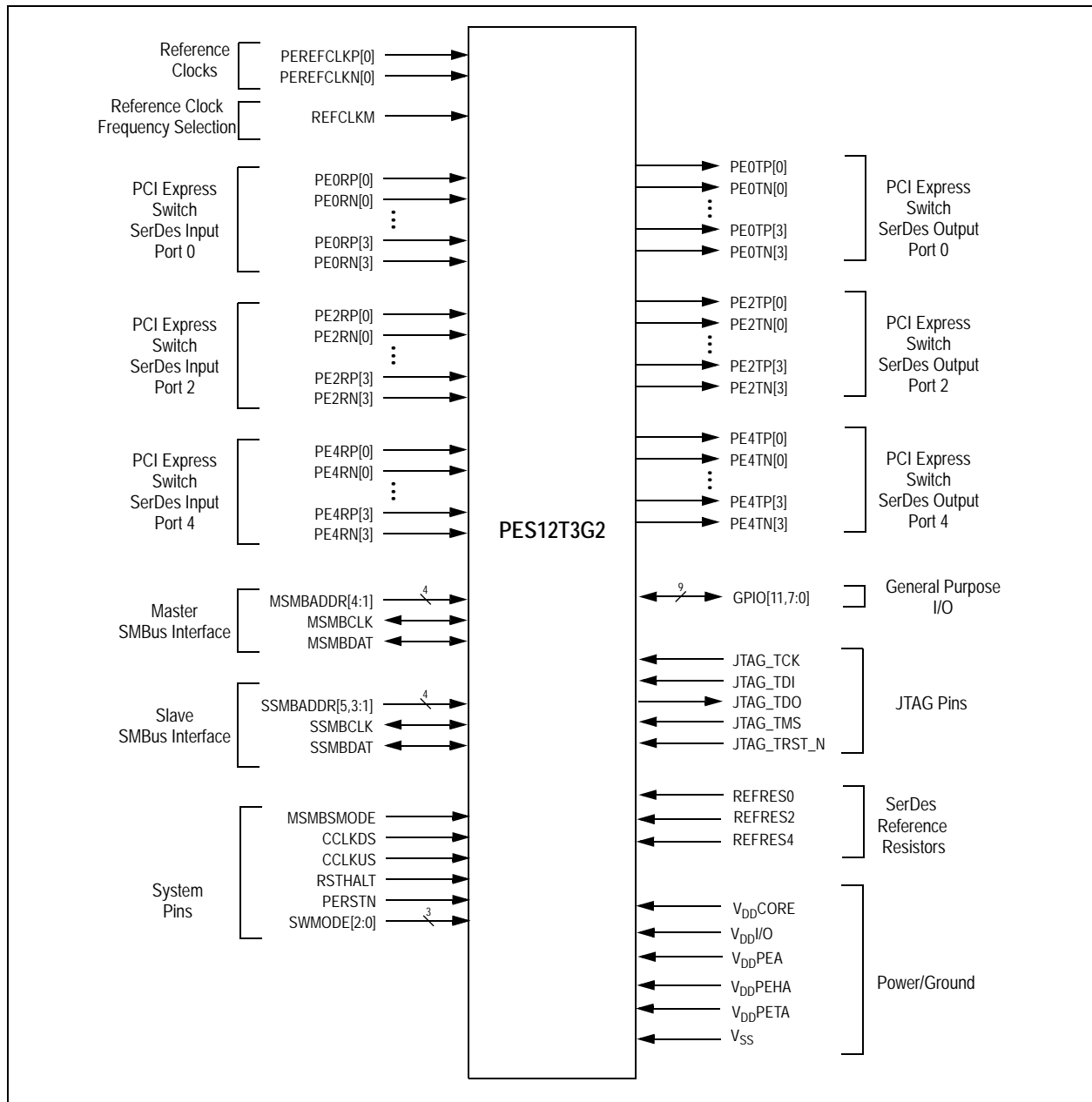
Logic Diagram — PES12T3G2

Figure 4 PES12T3G2 Logic Diagram

System Clock Parameters

Values based on systems running at recommended supply voltages and operating temperatures, as shown in Tables 13 and 15.

Parameter	Description	Condition	Min	Typical	Max	Unit
Refclk$_{FREQ}$	Input reference clock frequency range		100		125[1]	MHz
T$_{C-RISE}$	Rising edge rate	Differential	0.6		4	V/ns
T$_{C-FALL}$	Falling edge rate	Differential	0.6		4	V/ns
V$_{IH}$	Differential input high voltage	Differential	+150			mV
V$_{IL}$	Differential input low voltage	Differential			-150	mV
V$_{CROSS}$	Absolute single-ended crossing point voltage	Single-ended	+250		+550	mV
V$_{CROSS-DELTA}$	Variation of V$_{CROSS}$ over all rising clock edges	Single-ended			+140	mV
V$_{RB}$	Ring back voltage margin	Differential	-100		+100	mV
T$_{STABLE}$	Time before V$_{RB}$ is allowed	Differential	500			ps
T$_{PERIOD-AVG}$	Average clock period accuracy		-300		2800	ppm
T$_{PERIOD-ABS}$	Absolute period, including spread-spectrum and jitter		9.847		10.203	ns
T$_{CC-JITTER}$	Cycle to cycle jitter				150	ps
V$_{MAX}$	Absolute maximum input voltage				+1.15	V
V$_{MIN}$	Absolute minimum input voltage		-0.3			V
Duty Cycle	Duty cycle		40		60	%
Rise/Fall Matching	Single ended rising Refclk edge rate versus falling Refclk edge rate			20		%
Z$_{C-DC}$	Clock source output DC impedance		40		60	Ω

Table 9 Input Clock Requirements

[1.] The input clock frequency will be either 100 or 125 MHz depending on signal REFCLKM.

AC Timing Characteristics

Parameter	Description	Gen 1			Gen 2			Units
		Min[1]	Typ[1]	Max[1]	Min[1]	Typ[1]	Max[1]	
PCIe Transmit								
UI	Unit Interval	399.88	400	400.12	199.94	200	200.06	ps
T$_{TX-EYE}$	Minimum Tx Eye Width	0.75			0.75			UI
T$_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median			0.125				UI
T$_{TX-RISE}$, T$_{TX-FALL}$	TX Rise/Fall Time: 20% - 80%	0.125			0.15			UI
T$_{TX-IDLE-MIN}$	Minimum time in idle	20			20			UI

Table 10 PCIe AC Timing Characteristics (Part 1 of 2)

Parameter	Description	Gen 1			Gen 2			Units
		Min[1]	Typ[1]	Max[1]	Min[1]	Typ[1]	Max[1]	
T$_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Idle after sending an Idle ordered set			8			8	ns
T$_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition from valid idle to diff data			8			8	ns
T$_{TX-SKEW}$	Transmitter data skew between any 2 lanes			1.3			1.3	ns
T$_{MIN-PULSED}$	Minimum Instantaneous Lone Pulse Width		NA		0.9			UI
T$_{TX-HF-DJ-DD}$	Transmitter Deterministic Jitter > 1.5MHz Bandwidth		NA				0.15	UI
T$_{RF-MISMATCH}$	Rise/Fall Time Differential Mismatch		NA				0.1	UI
PCIe Receive								
UI	Unit Interval	399.88	400	400.12	199.94		200.06	ps
T$_{RX-EYE (with jitter)}$	Minimum Receiver Eye Width (jitter tolerance)	0.4			0.4			UI
T$_{RX-EYE-MEDIUM TO MAX JITTER}$	Max time between jitter median & max deviation			0.3				UI
T$_{RX-SKEW}$	Lane to lane input skew			20			8	ns
T$_{RX-HF-RMS}$	1.5 — 100 MHz RMS jitter (common clock)		NA				3.4	ps
T$_{RX-HF-DJ-DD}$	Maximum tolerable DJ by the receiver (common clock)		NA				88	ps
T$_{RX-LF-RMS}$	10 KHz to 1.5 MHz RMS jitter (common clock)		NA				4.2	ps
T$_{RX-MIN-PULSE}$	Minimum receiver instantaneous eye width		NA		0.6			UI

Table 10 PCIe AC Timing Characteristics (Part 2 of 2)

[1] Minimum, Typical, and Maximum values meet the requirements under PCI Specification 2.0

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
GPIO						
GPIO[11,7:0][1]	Tpw[2]	None	50	—	ns	

Table 11 GPIO AC Timing Characteristics

[1] GPIO signals must meet the setup and hold times if they are synchronous or the minimum pulse width if they are asynchronous.

[2] The values for this symbol were determined by calculation, not by testing.

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
JTAG						
JTAG_TCK	Tper_16a	none	50.0	—	ns	See Figure 5.
	Thigh_16a, Tlow_16a		10.0	25.0	ns	
JTAG_TMS[1], JTAG_TDI	Tsu_16b	JTAG_TCK rising	2.4	—	ns	
	Thld_16b		1.0	—	ns	
JTAG_TDO	Tdo_16c	JTAG_TCK falling	—	20	ns	
	Tdz_16c[2]		—	20	ns	
JTAG_TRST_N	Tpw_16d[2]	none	25.0	—	ns	

Table 12 JTAG AC Timing Characteristics

[1] The JTAG specification, IEEE 1149.1, recommends that JTAG_TMS should be held at 1 while the signal applied at JTAG_TRST_N changes from 0 to 1. Otherwise, a race may occur if JTAG_TRST_N is deasserted (going from low to high) on a rising edge of JTAG_TCK when JTAG_TMS is low, because the TAP controller might go to either the Run-Test/Idle state or stay in the Test-Logic-Reset state.

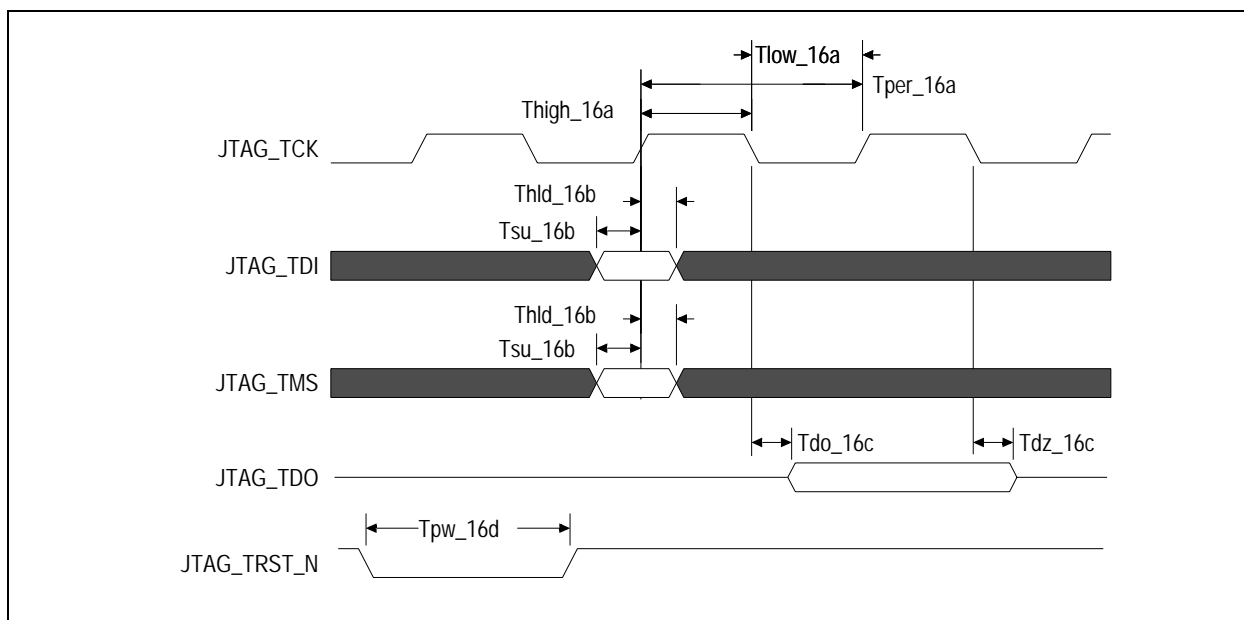[2] The values for this symbol were determined by calculation, not by testing.

Figure 5 JTAG AC Timing Waveform

Recommended Operating Supply Voltages

Symbol	Parameter	Minimum	Typical	Maximum	Unit
$V_{DD}CORE$	Internal logic supply	0.9	1.0	1.1	V
$V_{DD}I/O$	I/O supply except for SerDes LVPECL/CML	3.135	3.3	3.465	V
$V_{DD}PEA^1$	PCI Express Analog Power	0.95	1.0	1.1	V
$V_{DD}PEHA^2$	PCI Express Analog High Power	2.25	2.5	2.75	V
$V_{DD}PETA^1$	PCI Express Transmitter Analog Voltage	0.95	1.0	1.1	V
V_{SS}	Common ground	0	0	0	V

Table 13 PES12T3G2 Operating Voltages

[1.] $V_{DD}PEA$ and $V_{DD}PETA$ should have no more than $25mV_{peak-peak}$ AC power supply noise superimposed on the 1.0V nominal DC value.

[2.] $V_{DD}PEHA$ should have no more than $50mV_{peak-peak}$ AC power supply noise superimposed on the 2.5V nominal DC value.

Absolute Maximum Voltage Rating

Core Supply	PCIe Analog Supply	PCIe Analog High Supply	PCIe Transmitter Supply	I/O Supply
1.5V	1.5V	4.6V	1.5V	4.6V

Table 14 PES12T3G2 Absolute Maximum Voltage Rating

Warning: For proper and reliable operation in adherence with this data sheet, the device should not exceed the recommended operating voltages in Table 13. The absolute maximum operating voltages in Table 14 are offered to provide guidelines for voltage excursions outside the recommended voltage ranges. Device functionality is not guaranteed at these conditions and sustained operation at these values or any exposure to voltages outside the maximum range may adversely affect device functionality and reliability.

Power-Up/Power-Down Sequence

During power supply ramp-up, $V_{DD}CORE$ must remain at least 1.0V below $V_{DD}I/O$ at all times. There are no other power-up sequence requirements for the various operating supply voltages.

The power-down sequence can occur in any order.

Recommended Operating Temperature

Grade	Temperature
Commercial	0°C to +70°C Ambient
Industrial	-40°C to +85°C Ambient

Table 15 PES12T3G2 Operating Temperatures

Power Consumption

Typical power is measured under the following conditions: 25°C Ambient, 35% total link usage on all ports, typical voltages defined in Table 13 (and also listed below).

Maximum power is measured under the following conditions: 70°C Ambient, 85% total link usage on all ports, maximum voltages defined in Table 13 (and also listed below).

Number of active Lanes per Port		Core Supply		PCIe Analog Supply		PCIe Analog High Supply		PCIe Termin- ation Supply		I/O Supply		Total	
		Typ 1.0V	Max 1.1V	Typ 1.0V	Max 1.1V	Typ 2.5V	Max 2.75V	Typ 1.0V	Max 1.1V	Typ 3.3V	Max 3.465V	Typ Power	Max Power
4/4/4 (Full swing)	mA	531	781	402	484	155	220	230	264	3	4		
	Watts	0.53	0.86	0.40	0.53	0.39	0.61	0.23	0.29	0.01	0.02	1.56	2.3
4/1/1 (Full swing)	mA	440	550	320	352	110	132	120	130	3	4		
	Watts	0.44	0.61	0.32	0.39	0.28	0.36	0.12	0.14	.01	.02	1.16	1.51

Table 16 PES12T3G2 Power Consumption

Thermal Considerations

This section describes thermal considerations for the PES12T3G2 (19mm^2 CABGA324 package). The data in Table 17 below contains information that is relevant to the thermal performance of the PES12T3G2 switch.

> **Note:** It is important for the reliability of this device in any user environment that the junction temperature not exceed the $T_{J(max)}$ value

Symbol	Parameter	Value	Units	Conditions
$T_{J(max)}$	Junction Temperature	125	°C	Maximum
$T_{A(max)}$	Ambient Temperature	70	°C	Maximum
$\theta_{JA(effective)}$	Effective Thermal Resistance, Junction-to-Ambient	23.6	°C/W	Zero air flow
		16.8	°C/W	1 m/S air flow
		15.4	°C/W	2 m/S air flow
θ_{JB}	Thermal Resistance, Junction-to-Board	14.5	°C/W	
θ_{JC}	Thermal Resistance, Junction-to-Case	7.6	°C/W	
P	Power Dissipation of the Device	2.3	Watts	Maximum

Table 17 Thermal Specifications for PES12T3G2, 19x19 mm CABGA324 Package

specified in Table 17. Consequently, the effective junction to ambient thermal resistance (θ_{JA}) for the worst case scenario must be maintained below the value determined by the formula:

$$\theta_{JA} = (T_{J(max)} - T_{A(max)})/P$$

Given that the values of $T_{J(max)}$, $T_{A(max)}$, and P are known, the value of desired θ_{JA} becomes a known entity to the system designer. How to achieve the desired θ_{JA} is left up to the board or system designer, but in general, it can be achieved by adding the effects of θ_{JC} (value provided in Table 17), thermal resistance of the chosen adhesive (θ_{CS}), that of the heat sink (θ_{SA}), amount of airflow, and properties of the circuit board (number of layers and size of the board). As a general guideline, this device will not need a heat sink if the board has 8 or more layers AND the board size is larger than 4"x12" AND airflow in excess of 0.5 m/s is available. It is strongly recommended that users perform their own thermal analysis for their own board and system design scenarios.

DC Electrical Characteristics

Values based on systems running at recommended supply voltages, as shown in Table 13.

Note: See Table 8, Pin Characteristics, for a complete I/O listing.

I/O Type	Parameter	Description	Gen1			Gen2			Unit	Conditions
			Min[1]	Typ[1]	Max[1]	Min[1]	Typ[1]	Max[1]		
Serial Link	PCIe Transmit									
	$V_{TX-DIFFp-p}$	Differential peak-to-peak output voltage	800		1200	800		1200	mV	
	$V_{TX-DIFFp-p-LOW}$	Low-Drive Differential Peak to Peak Output Voltage	400		1200	400		1200	mV	
	$V_{TX-DE-RATIO-3.5dB}$	De-emphasized differential output voltage	-3		-4	-3.0	-3.5	-4.0	dB	
	$V_{TX-DE-RATIO-6.0dB}$	De-emphasized differential output voltage	NA			-5.5	-6.0	-6.5	dB	
	$V_{TX-DC-CM}$	DC Common mode voltage	0		3.6	0		3.6	V	
	$V_{TX-CM-ACP}$	RMS AC peak common mode output voltage			20				mV	
	$V_{TX-CM-DC-active-idle-delta}$	Abs delta of DC common mode voltage between L0 and idle			100			100	mV	
	$V_{TX-CM-DC-line-delta}$	Abs delta of DC common mode voltage between D+ and D-			25			25	mV	
	$V_{TX-Idle-DiffP}$	Electrical idle diff peak output			20			20	mV	
	$RL_{TX-DIFF}$	Transmitter Differential Return loss	10					10	dB	0.05 - 1.25GHz
								8	dB	1.25 - 2.5GHz
	RL_{TX-CM}	Transmitter Common Mode Return loss	6					6	dB	
	$Z_{TX-DIFF-DC}$	DC Differential TX impedance	80	100	120			120	Ω	
	VTX-CM-ACpp	Peak-Peak AC Common	NA					100	mV	
	$V_{TX-DC-CM}$	Transmit Driver DC Common Mode Voltage	0		3.6	0		3.6	V	
	$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during Receiver Detection			600			600	mV	
	$I_{TX-SHORT}$	Transmitter Short Circuit Current Limit	0		90			90		mA

Table 18 DC Electrical Characteristics (Part 1 of 2)

I/O Type	Parameter	Description	Gen1			Gen2			Unit	Conditions
			Min[1]	Typ[1]	Max[1]	Min[1]	Typ[1]	Max[1]		
Serial Link (cont.)	PCIe Receive									
	$V_{RX-DIFFp-p}$	Differential input voltage (peak-to-peak)	175		1200	120		1200	mV	
	$RL_{RX-DIFF}$	Receiver Differential Return Loss	10					10	dB	0.05 - 1.25GHz
								8		1.25 - 2.5GHz
	RL_{RX-CM}	Receiver Common Mode Return Loss	6					6	dB	
	$Z_{RX-DIFF-DC}$	Differential input impedance (DC)	80	100	120	Refer to return loss spec			Ω	
	Z_{RX--DC}	DC common mode impedance	40	50	60	40		60	Ω	
	$Z_{RX-COMM-DC}$	Powered down input common mode impedance (DC)	200k	350k				50k	Ω	
	$Z_{RX-HIGH-IMP-DC-POS}$	DC input CM input impedance for V>0 during reset or power down			50k			50k	Ω	
	$Z_{RX-HIGH-IMP-DC-NEG}$	DC input CM input impedance for V<0 during reset or power down			1.0k			1.0k	Ω	
	$V_{RX-IDLE-DET-DIFFp-p}$	Electrical idle detect threshold	65		175	65		175	mV	
	$V_{RX-CM-ACp}$	Receiver AC common-mode peak voltage			150			150	mV	$V_{RX-CM-ACp}$
PCIe REFCLK										
	C_{IN}	Input Capacitance	1.5	—		1.5	—		pF	
Other I/Os										
LOW Drive Output	I_{OL}		—	2.5	—	—	2.5	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-5.5	—	—	-5.5	—	mA	V_{OH} = 1.5V
High Drive Output	I_{OL}		—	12.0	—	—	12.0	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-20.0	—	—	-20.0	—	mA	V_{OH} = 1.5V
Schmitt Trigger Input (STI)	V_{IL}		-0.3	—	0.8	-0.3	—	0.8	V	—
	V_{IH}		2.0	—	V_{DD}I/O + 0.5	2.0	—	V_{DD}I/O + 0.5	V	—
Input	V_{IL}		-0.3	—	0.8	-0.3	—	0.8	V	—
	V_{IH}		2.0	—	V_{DD}I/O + 0.5	2.0	—	V_{DD}I/O + 0.5	V	—
Capacitance	C_{IN}		—	—	8.5	—	—	8.5	pF	—
Leakage	Inputs		—	—	± 10	—	—	± 10	µA	V_{DD}I/O (max)
	$I/O_{LEAK\ W/O}$ Pull-ups/downs		—	—	± 10	—	—	± 10	µA	V_{DD}I/O (max)
	$I/O_{LEAK\ WITH}$ Pull-ups/downs		—	—	± 80	—	—	± 80	µA	V_{DD}I/O (max)

Table 18 DC Electrical Characteristics (Part 2 of 2)

[1.] Minimum, Typical, and Maximum values meet the requirements under PCI Specification 2.0.

Package Pinout — 324-BGA Signal Pinout for PES12T3G2

The following table lists the pin numbers and signal names for the PES12T3G2 device.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
A1	V_{SS}		B17	SWMODE_1		D15	GPIO_01	1	F13	V_{SS}	
A2	V_{SS}		B18	SWMODE_2		D16	PE4TP00		F14	$V_{DD}CORE$	
A3	PE0RN00		C1	JTAG_TCK		D17	$V_{DD}PETA$		F15	$V_{DD}I/O$	
A4	PE0RP00		C2	PE0TP00		D18	GPIO_03		F16	V_{SS}	
A5	V_{SS}		C3	PE0TN00		E1	V_{SS}		F17	$V_{DD}PEA$	
A6	PE0RN01		C4	V_{SS}		E2	$V_{DD}PEA$		F18	PE4RP00	
A7	PE0RP01		C5	PE0TP01		E3	PE2TN03		G1	PE2RN03	
A8	V_{SS}		C6	PE0TN01		E4	JTAG_TMS		G2	$V_{DD}PEA$	
A9	PEREFCLKP0		C7	$V_{DD}PEA$		E5	$V_{DD}CORE$		G3	$V_{DD}PETA$	
A10	PEREFCLKN0		C8	$V_{DD}PETA$		E6	$V_{DD}I/O$		G4	V_{SS}	
A11	V_{SS}		C9	V_{SS}		E7	$V_{DD}PEHA$		G5	$V_{DD}CORE$	
A12	PE0RN02		C10	PE0TP02		E8	$V_{DD}PEHA$		G6	$V_{DD}I/O$	
A13	PE0RP02		C11	PE0TN02		E9	$V_{DD}PEHA$		G7	V_{SS}	
A14	V_{SS}		C12	$V_{DD}PETA$		E10	$V_{DD}CORE$		G8	V_{SS}	
A15	PE0RN03		C13	PE0TP03		E11	$V_{DD}PEHA$		G9	$V_{DD}CORE$	
A16	PE0RP03		C14	PE0TN03		E12	$V_{DD}I/O$		G10	V_{SS}	
A17	CCLKDS		C15	V_{SS}		E13	$V_{DD}CORE$		G11	V_{SS}	
A18	SWMODE_0		C16	CCLKUS		E14	$V_{DD}I/O$		G12	V_{SS}	
B1	JTAG_TDI		C17	PERSTN		E15	GPIO_00	1	G13	$V_{DD}I/O$	
B2	V_{SS}		C18	GPIO_02	1	E16	PE4TN00		G14	$V_{DD}PEHA$	
B3	V_{SS}		D1	V_{SS}		E17	V_{SS}		G15	V_{SS}	
B4	V_{SS}		D2	JTAG_TDO		E18	PE4RN00		G16	PE4TP01	
B5	V_{SS}		D3	$V_{DD}PETA$		F1	PE2RP03		G17	$V_{DD}PETA$	
B6	V_{SS}		D4	JTAG_TRST_N		F2	$V_{DD}PEHA$		G18	V_{SS}	
B7	V_{SS}		D5	$V_{DD}I/O$		F3	PE2TP03		H1	V_{SS}	
B8	V_{SS}		D6	$V_{DD}PEHA$		F4	$V_{DD}CORE$		H2	V_{SS}	
B9	$V_{DD}PEA$		D7	V_{SS}		F5	$V_{DD}I/O$		H3	PE2TN02	
B10	$V_{DD}PEA$		D8	$V_{DD}CORE$		F6	V_{SS}		H4	V_{SS}	
B11	$V_{DD}PETA$		D9	$V_{DD}CORE$		F7	$V_{DD}CORE$		H5	$V_{DD}PEHA$	
B12	V_{SS}		D10	REFRES0		F8	V_{SS}		H6	V_{SS}	
B13	V_{SS}		D11	$V_{DD}PEA$		F9	V_{SS}		H7	$V_{DD}CORE$	
B14	$V_{DD}CORE$		D12	$V_{DD}CORE$		F10	V_{SS}		H8	V_{SS}	
B15	V_{SS}		D13	V_{SS}		F11	V_{SS}		H9	V_{SS}	
B16	$V_{DD}PEA$		D14	RSTHALT		F12	$V_{DD}CORE$		H10	V_{SS}	

Table 19 PES12T3G2 324-pin Signal Pin-Out (Part 1 of 3)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
H11	$V_{DD}CORE$		K13	V_{SS}		M15	V_{SS}		P17	V_{SS}	
H12	V_{SS}		K14	$V_{DD}CORE$		M16	$V_{DD}PETA$		P18	PE4RN03	
H13	V_{SS}		K15	V_{SS}		M17	$V_{DD}PEA$		R1	PE2RP00	
H14	$V_{DD}PEHA$		K16	PE4TP02		M18	PE4RP02		R2	V_{SS}	
H15	$V_{DD}CORE$		K17	REFRES4		N1	PE2RN01		R3	PE2TP00	
H16	PE4TN01		K18	V_{SS}		N2	$V_{DD}PEA$		R4	SSMBADDR_2	
H17	V_{SS}		L1	V_{SS}		N3	V_{SS}		R5	$V_{DD}I/O$	
H18	PE4RN01		L2	$V_{DD}PEA$		N4	V_{SS}		R6	MSMBSMODE	
J1	PE2RP02		L3	PE2TN01		N5	$V_{DD}CORE$		R7	$V_{DD}CORE$	
J2	$V_{DD}PETA$		L4	$V_{DD}CORE$		N6	V_{SS}		R8	V_{SS}	
J3	PE2TP02		L5	$V_{DD}PEHA$		N7	$V_{DD}I/O$		R9	V_{SS}	
J4	REFRES2		L6	V_{SS}		N8	V_{SS}		R10	V_{SS}	
J5	$V_{DD}CORE$		L7	V_{SS}		N9	V_{SS}		R11	$V_{DD}CORE$	
J6	V_{SS}		L8	V_{SS}		N10	V_{SS}		R12	V_{SS}	
J7	V_{SS}		L9	V_{SS}		N11	V_{SS}		R13	$V_{DD}I/O$	
J8	V_{SS}		L10	V_{SS}		N12	$V_{DD}I/O$		R14	V_{SS}	
J9	$V_{DD}CORE$		L11	V_{SS}		N13	V_{SS}		R15	V_{SS}	
J10	V_{SS}		L12	$V_{DD}CORE$		N14	$V_{DD}CORE$		R16	GPIO_04	1
J11	V_{SS}		L13	V_{SS}		N15	$V_{DD}CORE$		R17	$V_{DD}PEA$	
J12	$V_{DD}CORE$		L14	$V_{DD}PEHA$		N16	PE4TP03		R18	PE4RP03	
J13	V_{SS}		L15	V_{SS}		N17	$V_{DD}PEHA$		T1	PE2RN00	
J14	$V_{DD}PEHA$		L16	PE4TN02		N18	V_{SS}		T2	$V_{DD}PETA$	
J15	V_{SS}		L17	$V_{DD}PETA$		P1	V_{SS}		T3	V_{SS}	
J16	$V_{DD}PEA$		L18	PE4RN02		P2	V_{SS}		T4	SSMBADDR_5	
J17	$V_{DD}PEA$		M1	PE2RP01		P3	PE2TN00		T5	V_{SS}	
J18	PE4RP01		M2	$V_{DD}PETA$		P4	SSMBADDR_1		T6	MSMBDAT	
K1	PE2RN02		M3	PE2TP01		P5	$V_{DD}CORE$		T7	MSMBADDR_3	
K2	$V_{DD}PEA$		M4	V_{SS}		P6	$V_{DD}I/O$		T8	$V_{DD}PEA$	
K3	V_{SS}		M5	$V_{DD}PEHA$		P7	$V_{DD}CORE$		T9	NC	
K4	V_{SS}		M6	$V_{DD}I/O$		P8	$V_{DD}PEHA$		T10	NC	
K5	$V_{DD}PEHA$		M7	$V_{DD}CORE$		P9	$V_{DD}PEHA$		T11	$V_{DD}PEA$	
K6	V_{SS}		M8	V_{SS}		P10	$V_{DD}CORE$		T12	NC	
K7	$V_{DD}CORE$		M9	$V_{DD}CORE$		P11	$V_{DD}PEHA$		T13	NC	
K8	V_{SS}		M10	V_{SS}		P12	$V_{DD}CORE$		T14	$V_{DD}PETA$	
K9	V_{SS}		M11	$V_{DD}CORE$		P13	$V_{DD}CORE$		T15	V_{SS}	
K10	$V_{DD}CORE$		M12	V_{SS}		P14	$V_{DD}I/O$		T16	GPIO_06	
K11	V_{SS}		M13	$V_{DD}I/O$		P15	V_{SS}		T17	GPIO_05	
K12	V_{SS}		M14	$V_{DD}CORE$		P16	PE4TN03		T18	V_{SS}	

Table 19 PES12T3G2 324-pin Signal Pin-Out (Part 2 of 3)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
U1	V_{SS}		U10	V_{DD}PETA		V1	V_{SS}		V10	V_{SS}	
U2	V_{SS}		U11	V_{SS}		V2	V_{SS}		V11	V_{SS}	
U3	SSMBCLK		U12	V_{SS}		V3	SSMBDAT		V12	V_{SS}	
U4	SSMBADDR_3		U13	V_{SS}		V4	V_{SS}		V13	V_{SS}	
U5	V_{SS}		U14	V_{SS}		V5	MSMBADDR_4		V14	V_{SS}	
U6	MSMBCLK		U15	REFCLKM		V6	MSMBADDR_2		V15	V_{SS}	
U7	MSMBADDR_1		U16	GPIO_07	1	V7	V_{SS}		V16	GPIO_11	
U8	V_{DD}PEA		U17	V_{SS}		V8	V_{SS}		V17	V_{SS}	
U9	V_{SS}		U18	V_{SS}		V9	V_{SS}		V18	V_{SS}	

Table 19 PES12T3G2 324-pin Signal Pin-Out (Part 3 of 3)

Alternate Signal Functions

Pin	GPIO	Alternate
E15	GPIO_00	P2RSTN
D15	GPIO_01	P4RSTN
C18	GPIO_02	IOEXPINTN0
R16	GPIO_04	IOEXPINTN2
U16	GPIO_07	GPEN

Table 20 PES12T3G2 Alternate Signal Functions

No Connection Pins

NC Pins
T9
T10
T12
T13

Table 21 PES12T3G2 No Connection Pins

Power Pins

V$_{DD}$Core	V$_{DD}$Core	V$_{DD}$I/O	V$_{DD}$PEA	V$_{DD}$PEHA	V$_{DD}$PETA
B14	K7	D5	B9	D6	B11
D8	K10	E6	B10	E7	C8
D9	K14	E12	B16	E8	C12
D12	L4	E14	C7	E9	D3
E5	L12	F5	D11	E11	D17
E10	M7	F15	E2	F2	G3
E13	M9	G6	F17	G14	G17
F4	M11	G13	G2	H5	J2
F7	M14	M6	J16	H14	L17
F12	N5	M13	J17	J14	M2
F14	N14	N7	K2	K5	M16
G5	N15	N12	L2	L5	T2
G9	P5	P6	M17	L14	T14
H7	P7	P14	N2	M5	U10
H11	P10	R5	R17	N17	
H15	P12	R13	T8	P8	
J5	P13		T11	P9	
J9	R7		U8	P11	
J12	R11				

Table 22 PES12T3G2 Power Pins

Ground Pins

V$_{ss}$	V$_{ss}$	V$_{ss}$	V$_{ss}$	V$_{ss}$	V$_{ss}$
A1	E1	H9	L1	N18	U13
A2	E17	H10	L6	P1	U14
A5	F6	H12	L7	P2	U17
A8	F8	H13	L8	P15	U18
A11	F9	H17	L9	P17	V1
A14	F10	J6	L10	R2	V2
B2	F11	J7	L11	R8	V4
B3	F13	J8	L13	R9	V7
B4	F16	J10	L15	R10	V8
B5	G4	J11	M4	R12	V9
B6	G7	J13	M8	R14	V10
B7	G8	J15	M10	R15	V11
B8	G10	K3	M12	T3	V12
B12	G11	K4	M15	T5	V13
B13	G12	K6	N3	T15	V14
B15	G15	K8	N4	T18	V15
C4	G18	K9	N6	U1	V17
C9	H1	K11	N8	U2	V18
C15	H2	K12	N9	U5	
D1	H4	K13	N10	U9	
D7	H6	K15	N11	U11	
D13	H8	K18	N13	U12	

Table 23 PES12T3G2 Ground Pins

Signals Listed Alphabetically

Signal Name	I/O Type	Location	Signal Category
CCLKDS	I	A17	System
CCLKUS	I	C16	
GPIO_00	I/O	E15	General Purpose Input/Output
GPIO_01	I/O	D15	
GPIO_02	I/O	C18	
GPIO_03	I/O	D18	
GPIO_04	I/O	R16	
GPIO_05	I/O	T17	
GPIO_06	I/O	T16	
GPIO_07	I/O	U16	
GPIO_11	I/O	V16	
JTAG_TCK	I	C1	JTAG
JTAG_TDI	I	B1	
JTAG_TDO	O	D2	
JTAG_TMS	I	E4	
JTAG_TRST_N	I	D4	
MSMBADDR_1	I	U7	SMBus
MSMBADDR_2	I	V6	
MSMBADDR_3	I	T7	
MSMBADDR_4	I	V5	
MSMBCLK	I/O	U6	
MSMBDAT	I/O	T6	
MSMBSMODE	I	R6	System
No Connection	See Table 21 for a list of NC pins		
PE0RN00	I	A3	PCI Express
PE0RN01	I	A6	
PE0RN02	I	A12	

Table 24 89PES12T3G2 Alphabetical Signal List (Part 1 of 3)

Signal Name	I/O Type	Location	Signal Category
PE0RN03	I	A15	PCI Express (Cont.)
PE0RP00	I	A4	
PE0RP01	I	A7	
PE0RP02	I	A13	
PE0RP03	I	A16	
PE0TN00	O	C3	
PE0TN01	O	C6	
PE0TN02	O	C11	
PE0TN03	O	C14	
PE0TP00	O	C2	
PE0TP01	O	C5	
PE0TP02	O	C10	
PE0TP03	O	C13	
PE2RN00	I	T1	
PE2RN01	I	N1	
PE2RN02	I	K1	
PE2RN03	I	G1	
PE2RP00	I	R1	
PE2RP01	I	M1	
PE2RP02	I	J1	
PE2RP03	I	F1	
PE2TN00	O	P3	
PE2TN01	O	L3	
PE2TN02	O	H3	
PE2TN03	O	E3	
PE2TP00	O	R3	
PE2TP01	O	M3	
PE2TP02	O	J3	
PE2TP03	O	F3	
PE4RN00	I	E18	
PE4RN01	I	H18	
PE4RN02	I	L18	
PE4RN03	I	P18	
PE4RP00	I	F18	
PE4RP01	I	J18	
PE4RP02	I	M18	

Table 24 89PES12T3G2 Alphabetical Signal List (Part 2 of 3)

Signal Name	I/O Type	Location	Signal Category
PE4RP03	I	R18	PCI Express (Cont.)
PE4TN00	O	E16	
PE4TN01	O	H16	
PE4TN02	O	L16	
PE4TN03	O	P16	
PE4TP00	O	D16	
PE4TP01	O	G16	
PE4TP02	O	K16	
PE4TP03	O	N16	
PEREFCLKN0	I	A10	
PEREFCLKP0	I	A9	
PERSTN	I	C17	System
REFCLKM	I	U15	PCI Express
REFRES0	I/O	D10	SerDes Reference Resistors
REFRES2	I/O	J4	
REFRES4	I/O	K17	
RSTHALT	I	D14	System
SSMBADDR_1	I	P4	SMBus
SSMBADDR_2	I	R4	
SSMBADDR_3	I	U4	
SSMBADDR_5	I	T4	
SSMBCLK	I/O	U3	SMBus
SSMBDAT	I/O	V3	
SWMODE_0	I	A18	System
SWMODE_1	I	B17	
SWMODE_2	I	B18	
$V_{DD}CORE$, $V_{DD}I/O$, $V_{DD}PEA$, $V_{DD}PEHA$, $V_{DD}PETA$	See Table 22 for a listing of power pins.		
V_{SS}	See Table 23 for a listing of ground pins.		

Table 24 89PES12T3G2 Alphabetical Signal List (Part 3 of 3)

PES12T3G2 Pinout — Top View

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PES12T3G2 Package Drawing — 324-Pin BC324/BCG324

PES12T3G2 Package Drawing — Page Two

BOTTOM VIEW

324 SOLDER BALLS

A1 BALL PAD CORNER

1.00 REF

1.00

1.00

1.00 REF

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M—1994.

2. THE BASIC SOLDER BALL GRID PITCH IS 1.00mm.

3. THE MAXIMUM SOLDER BALL MATRIX SIZE IS 18 X 18.

4. THE MAXIMUM ALLOWABLE NUMBER OF SOLDER BALLS IS 324.

5. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.

6. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

7. "A1" ID CORNER MUST BE IDENTIFIED. IDENTIFICATION MAY BE BY MEANS OF CHAMFER, METALLIZED OR INK MARK, INDENTATION OR OTHER FEATURE OF THE PACKAGE BODY.

8. THIS DRAWING CONFORMS TO THE JEDEC REGISTERED OUTLINE MS—034/A, VARIATION AAG—1 EXCEPT FOR A1, b, AND aaa DIMENSIONS.

Revision History

March 27, 2008: Initial publication of final data sheet.

April 17, 2008: In Table 16, Thermal Specifications, revised values for θ_{JA}, θ_{JB}, and θ_{JC}.

October 28, 2008: Added ZB silicon to Ordering Information section.

February 24, 2009: Revised AC Timing Characteristics table and DC Electrical Characteristics table to correct typos.

January 18, 2010: Revised Power Management list in Features section.
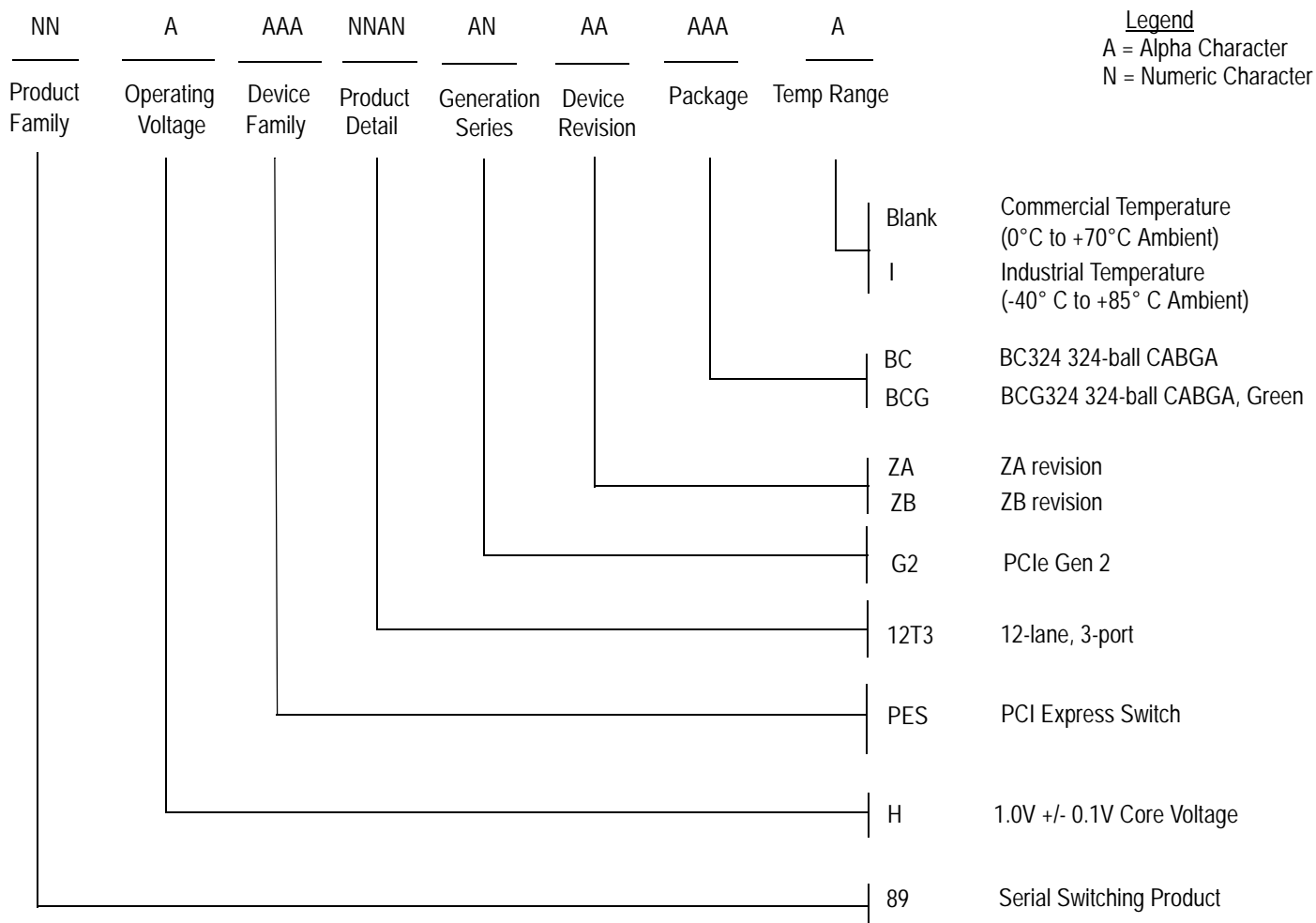
February 2, 2010: Added new section Absolute Maximum Voltage Rating with table.

September 13, 2010: In Table 8, changed Buffer type for PCI Express from CML to PCIe differential and changed reference clocks to HCSL.

March 30, 2011: In Table 13, added VddPETA to footnote #1.

August 10, 2011: Added Industrial temperature to Table 15 and to Order page.

Ordering Information

NN	A	AAA	NNAN	AN	AA	AAA	A
Product Family	Operating Voltage	Device Family	Product Detail	Generation Series	Device Revision	Package	Temp Range

Blank — Commercial Temperature (0°C to +70°C Ambient)

I — Industrial Temperature (-40° C to +85° C Ambient)

BC — BC324 324-ball CABGA

BCG — BCG324 324-ball CABGA, Green

ZA — ZA revision

ZB — ZB revision

G2 — PCIe Gen 2

12T3 — 12-lane, 3-port

PES — PCI Express Switch

H — 1.0V +/- 0.1V Core Voltage

89 — Serial Switching Product

Valid Combinations

89HPES12T3G2ZABC	324-ball BGA package, Commercial Temp.
89HPES12T3G2ZABCG	324-ball Green BGA package, Commercial Temp.
89HPES12T3G2ZBBC	324-ball BGA package, Commercial Temp.
89HPES12T3G2ZBBCG	324-ball Green BGA package, Commercial Temp.
89HPES12T3G2ZABCI	324-ball BGA package, Industrial Temp.
89HPES12T3G2ZABCGI	324-ball Green BGA package, Industrial Temp.
89HPES12T3G2ZBBCI	324-ball BGA package, Industrial Temp.
89HPES12T3G2ZBBCGI	324-ball Green BGA package, Industrial Temp.

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