Low Skew, ÷2, ÷4, ÷8 Differential-to-LVPECL Clock Divider

ICS8S73034I

DATA SHEET

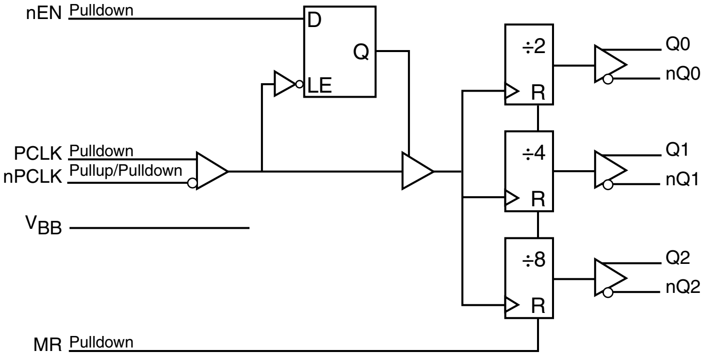
General Description

The ICS8S73034I is a high-speed, differential-to- LVPECL clock divider designed for high-performance telecommunication, computing and networking applications. High clock frequency capability and the differential design make the ICS8S73034I an ideal choice for performance clock distribution networks. The device frequency-divides the input clock by ÷2, ÷4 and ÷8. Each frequency-divided clock signal is output at a separate LVPECL output. The differential input pair can be driven by LVPECL, LVDS, CML and SSTL signals. Single-ended input signals are supported by using the integrated bias voltage generator (V_{BB}). The ICS8S73034I is optimized for 3.3V and 2.5V power supply voltages and the temperature range of -40 to +85°C. The device is available in space-saving 16-lead TSSOP and SOIC packages.

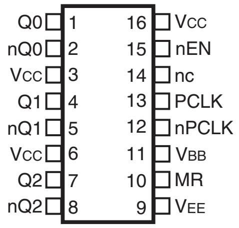
Features

- ÷2, ÷4 and ÷8 clock frequency divider
- Three differential LVPECL output pairs
- One differential PCLK, nPCLK input pair
- PCLK, nPCLK pair can accept the following differential input levels: LVPECL, LVDS, CML
- V_{BB} bias voltage generator supports single-ended LVPECL clock input signals
- LVCMOS control inputs
- Maximum input frequency: 3.2GHz
- Translates any single-ended input signal to 3.3V LVPECL levels with bias resistors on nPCLK input
- LVPECL mode operating voltage supply range: V_{CC} = 2.375V to 3.8V, V_{EE} = 0V
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



ICS8S73034I

16-Lead SOIC, 150 Mil
3.9mm x 9.9mm x 1.375mm package body
M Package
Top View

16-Lead TSSOP
4.4mm x 5.0mm x 0.925mm package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	Q0, nQ0	Output		Differential output pair. LVPECL interface levels.
3, 6, 16	V_{CC}	Power		Power supply pins.
4, 5	Q1, nQ1	Output		Differential output pair. LVPECL interface levels.
7, 8	Q2, nQ2	Output		Differential output pair. LVPECL interface levels.
9	V_{EE}	Power		Negative supply pin.
10	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
11	V_{BB}	Output		Bias voltage.
12	nPCLK	Input	Pullup/ Pulldown	Inverting differential clock input. Defaults to $^{2}/_{3} * V_{CC}$ when left open. LVPECL interface levels.
13	PCLK	Input	Pulldown	Non-inverting differential clock input. LVPECL interface levels.
14	nc	Unused		No connect.
15	nEN	Input	Pulldown	Synchronous clock enable. When logic LOW, the clock is enabled and frequency-divided. When logic HIGH, the clock is disabled and the outputs remain stopped in the same logic state (hold). LVTTL / LVCMOS interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$R_{PULLDOWN}$	Input Pulldown Resistor			75		kΩ
R_{PULLUP}	Input Pullup Resistor			37.5		kΩ

Function Table

Table 3. Truth Table

Inputs			Function
PCLK	nEN	MR	
↓	L	L	Divide
↑	H	L	Hold Q[0:2]
X	X	H	Reset Q[0:2]

↑ = Rising edge transition
↓ = Falling edge transition
X = Don’t care

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	**Rating**
Supply Voltage, V_{CC}	4.6V (LVPECL mode, V_{EE} = 0V)
Inputs, V_I (LVPECL mode)	-0.5V to V_{CC} + 0.5V
Outputs, I_O Continuos Current Surge Current	 50mA 100mA
V_{BB} Sink/Source, I_{BB}	±0.5mA
Operating Temperature Range, T_A	-40°C to +85°C
Package Thermal Impedance, θ_{JA} 16 Lead SOIC, Junction-to-Ambient 16 Lead TSSOP, Junction-to-Ambient	 70.2°C/W (0 mps) 100°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = 2.375V to 3.8V; V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	**Parameter**	**Test Conditions**	**Minimum**	**Typical**	**Maximum**	**Units**
V_{CC}	Power Supply Voltage		2.375	3.3	3.8	V
I_{EE}	Power Supply Current				45	mA

Table 4B. DC Characteristics, V_{CC} = 2.375V to 3.8V, V_{EE} = 0V; T_A = -40°C to 85°C

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1		V_{CC}-1.070	V_{CC}-0.867	V_{CC}-0.635	V_{CC}-1.070	V_{CC}-0.867	V_{CC}-0.635	V_{CC}-1.070	V_{CC}-0.867	V_{CC}-0.635	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC}-1.960	V_{CC}-1.780	V_{CC}-1.590	V_{CC}-1.960	V_{CC}-1.780	V_{CC}-1.590	V_{CC}-1.960	V_{CC}-1.780	V_{CC}-1.590	V
V_{IH}	Input High Voltage (Single-ended)		0.7V_{CC}		V_{CC} + 0.3	0.7V_{CC}		V_{CC} + 0.3	0.7V_{CC}		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage (Single-ended)		-0.3		0.3V_{CC}	-0.3		0.3V_{CC}	-0.3		0.3V_{CC}	V
V_{BB}	Output Voltage Reference		V_{CC} - 1.44		V_{CC} - 1.32	V_{CC} - 1.44		V_{CC} - 1.32	V_{CC} - 1.44		V_{CC} - 1.32	V
V_{PP}	Peak-to-Peak Input Voltage		0.15	0.8	1.3	0.15	0.8	1.3	0.15	0.8	1.3	V
V_{CMR}	Input High Voltage Common Mode Range; NOTE 2		1.2		V_{CC}	1.2		V_{CC}	1.2		V_{CC}	V
I_{IH}	Input High Current	PCLK/ nPCLK, MR, nEN			150			150			150	µA
I_{IL}	Input Low Current	PCLK, MR, nEN	-10			-10			-10			µA
		nPCLK	-150			-150			-150			µA

NOTE Input and output parameters vary 1:1 with V_{CC}.
NOTE 1: Outputs terminated with 50Ω to V_{CC} – 2V.
NOTE 2: Common mode voltage is defined as V_{IH}.

AC Electrical Characteristics

Table 5. AC Characteristics, V_{CC} = 2.375V to 3.8V, V_{EE} = 0V; T_A = -40°C to 85°C

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	
f_{IN}	Input Frequency				3.2			3.2			3.2	GHz
f_{OUT}	Output Frequency	Q0, nQ0			1.6			1.6			1.6	GHz
		Q1, nQ1			800			800			800	MHz
		Q2, nQ2			400			400			400	MHz
t_{PD}	Propagation Delay; NOTE 1		270	370	470	310	410	510	330	450	565	ps
tsk(o)	Output Skew; NOTE 2				50			50			50	ps
t_{RR}	Set/Reset Recovery			320	500		320	500		320	500	ps
t_S	Setup Time	nEN			400			400			400	ps
t_H	Hold Time	nEN			200			200			200	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	80	145	210	85	150	215	100	165	230	ps
odc	Output Duty Cycle		48		52	48		52	48		52	%

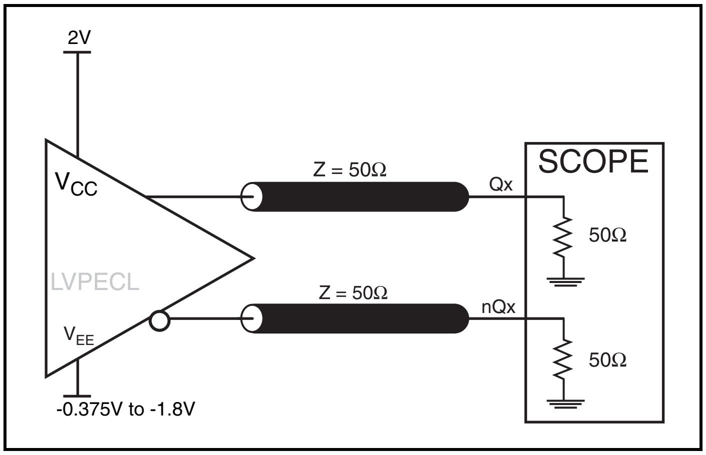
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

All parameters are measured at $f_{IN} \leq 1.5$GHz, unless otherwise noted.

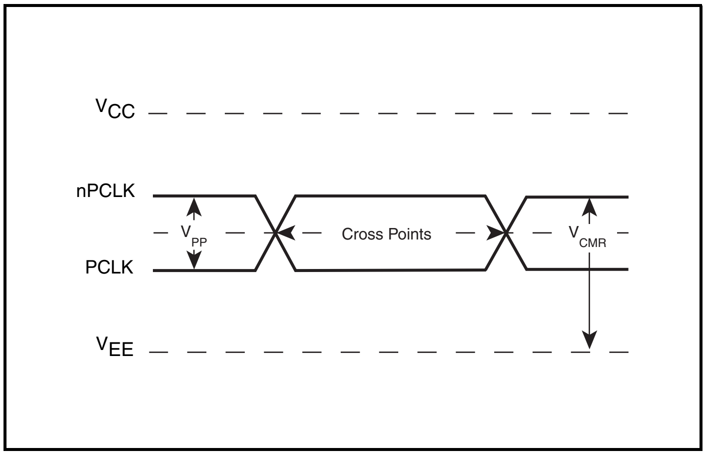
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Output skew at coincident rising edges.

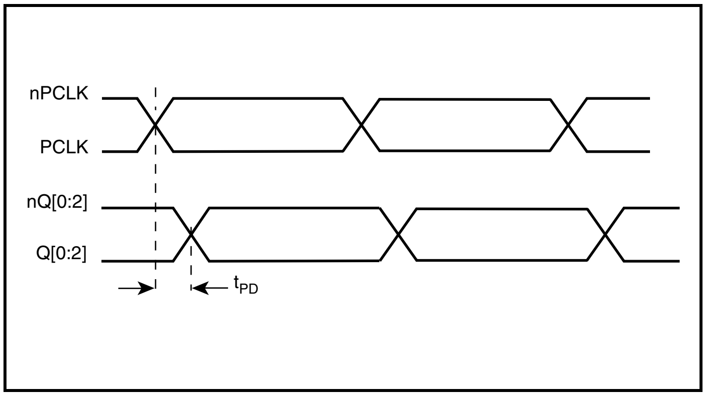
Parameter Measurement Information



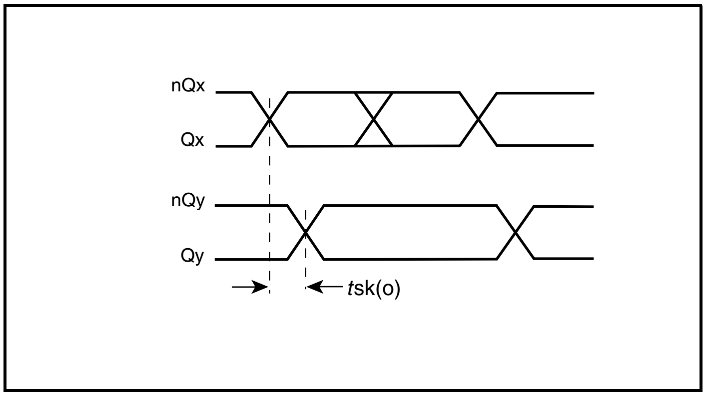
LVPECL Output Load AC Test Circuit



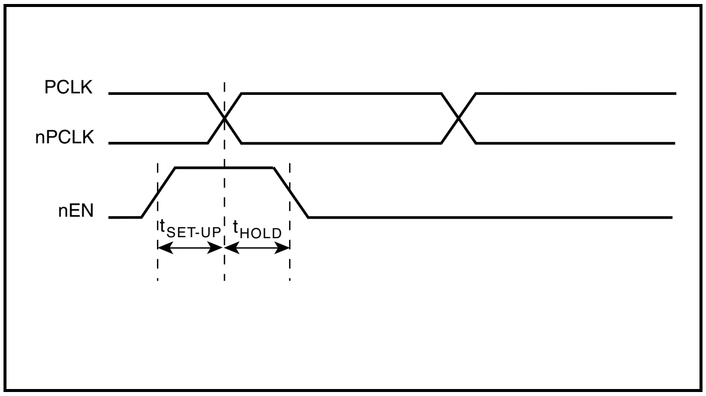
Differential Input Level



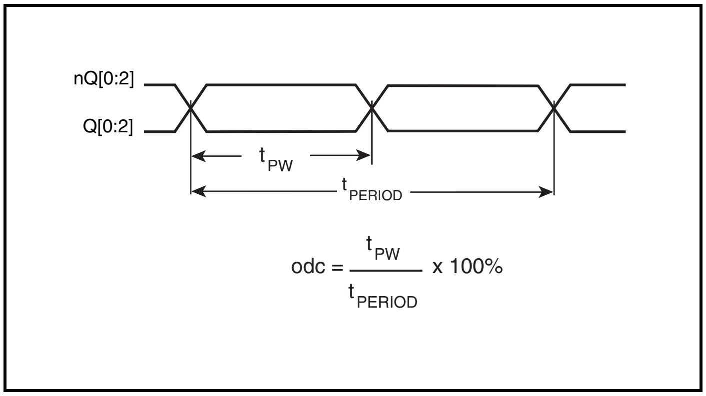
Propagation Delay



Output Skew



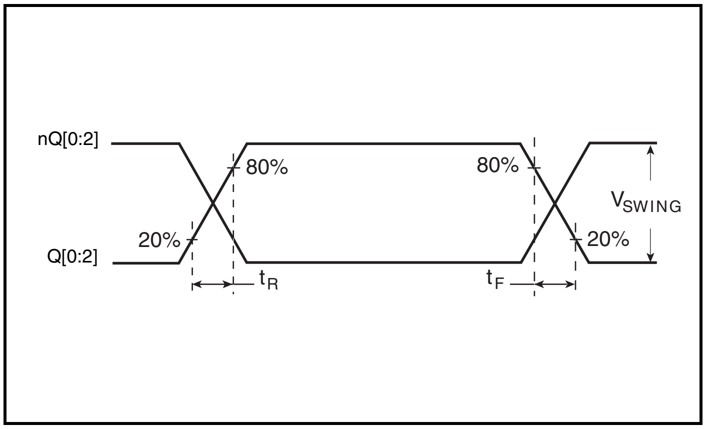
Setup and Hold Time



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

Output Duty Cycle

Parameter Measurement Information, continued



Output Rise/Fall Time

Application Information

Recommendations for Unused Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

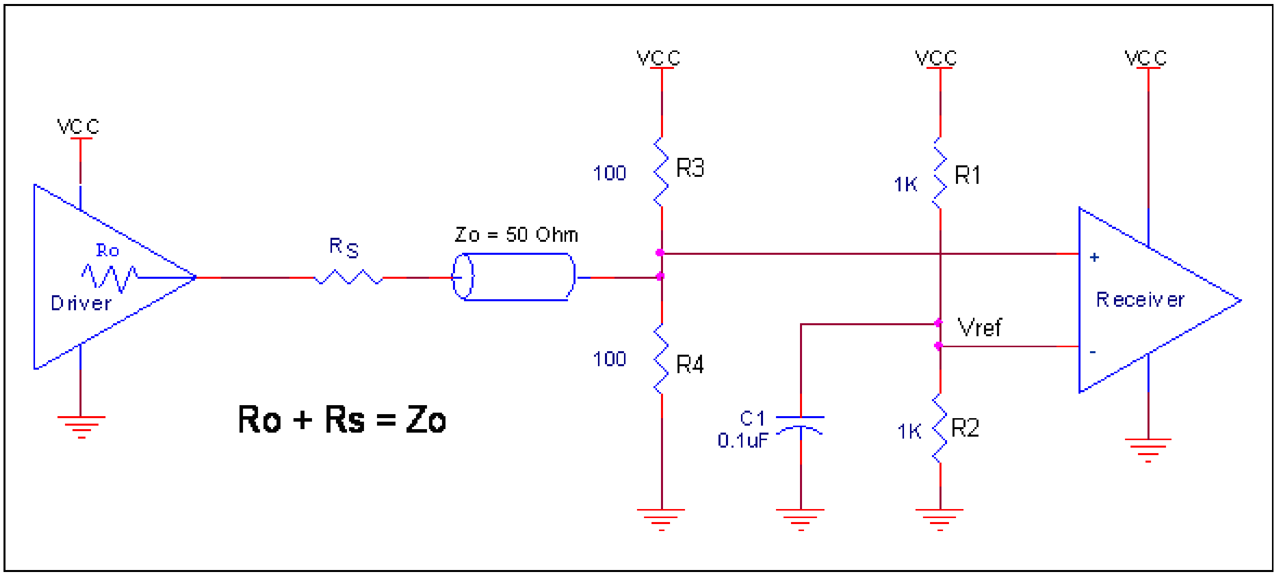


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

3.3V LVPECL Clock Input Interface

The PCLK/nPCLK accepts LVPECL, LVDS, CML and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2E* show interface examples for the PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

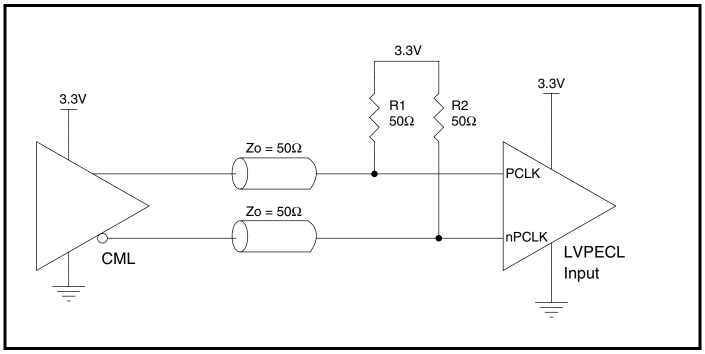


Figure 2A. PCLK/nPCLK Input Driven by a CML Driver

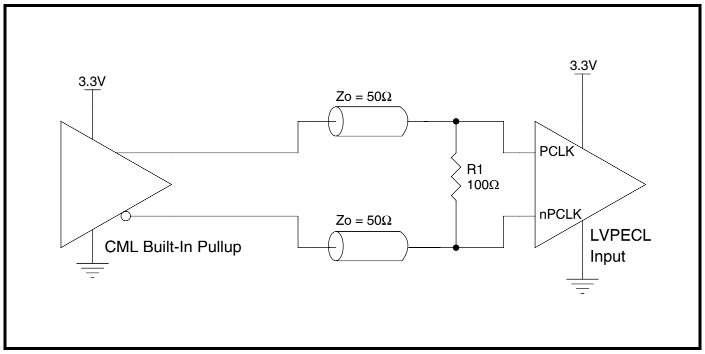


Figure 2B. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

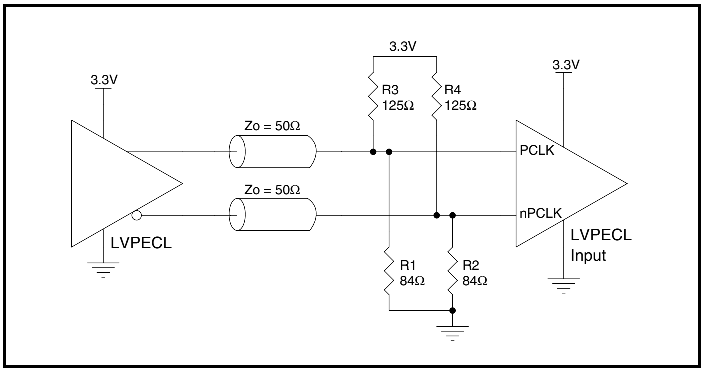


Figure 2C. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

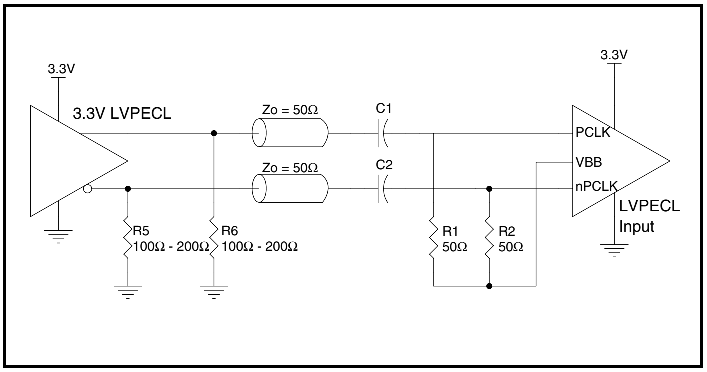


Figure 2D. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

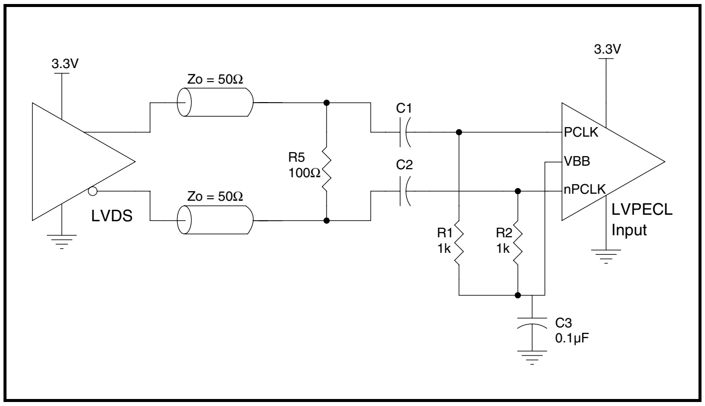


Figure 2E. PCLK/nPCLK Input Driven by a 3.3V LVDS Driver

2.5V LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, LVDS, CML and other differential signals. The differential signal must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3E* show interface examples for the PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

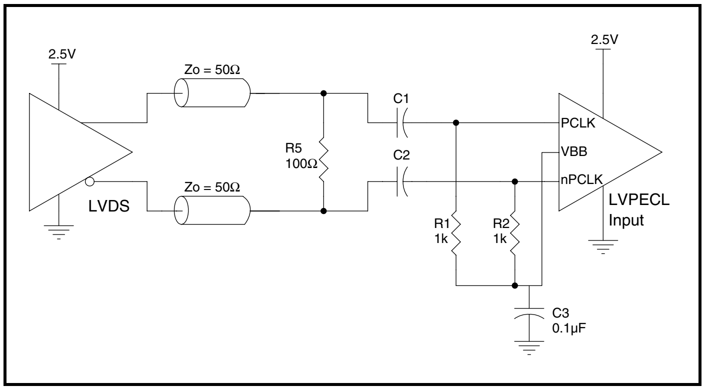


Figure 3A. PCLK/nPCLK Input Driven by a 2.5V LVDS Driver

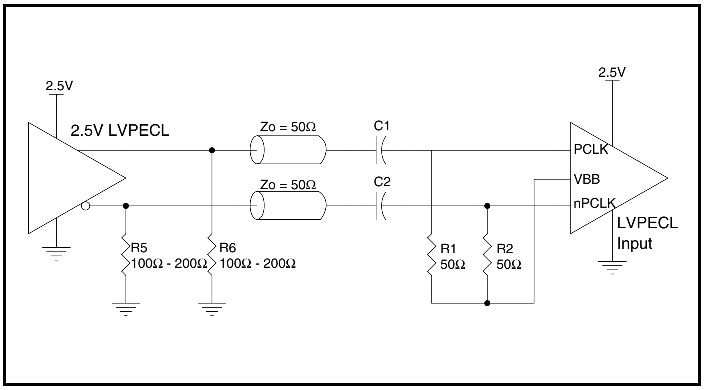


Figure 3B. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

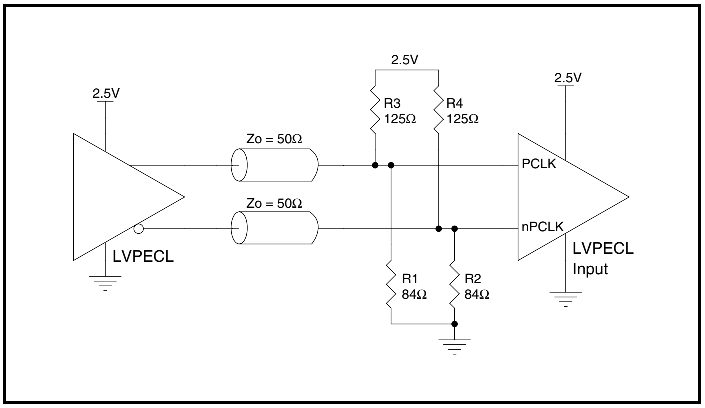


Figure 3C. PCLK/nPCLK Input Driven by a 2.5V LVPECL Driver

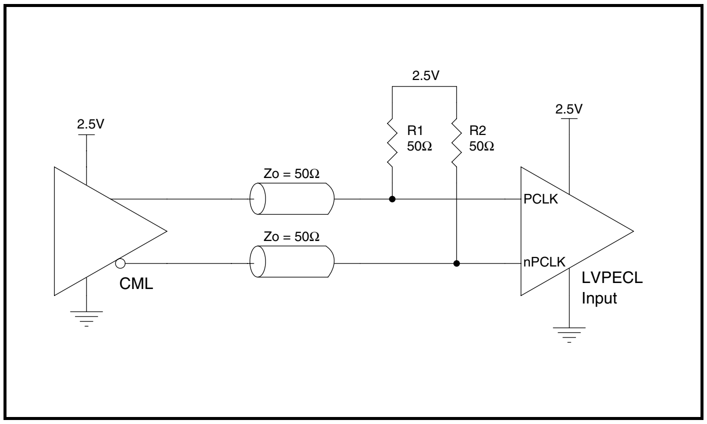


Figure 3D. PCLK/nPCLK Input Driven by a CML Driver

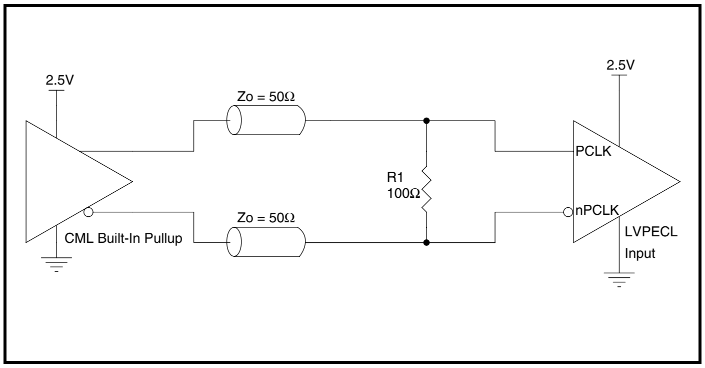
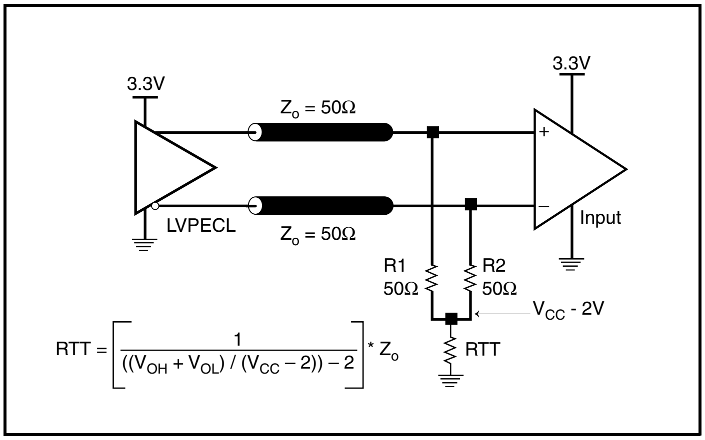


Figure 3E. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.



$$RTT = \left[\frac{1}{((V_{OH} + V_{OL}) / (V_{CC} - 2)) - 2}\right] * Z_o$$

Figure 4A. 3.3V LVPECL Output Termination

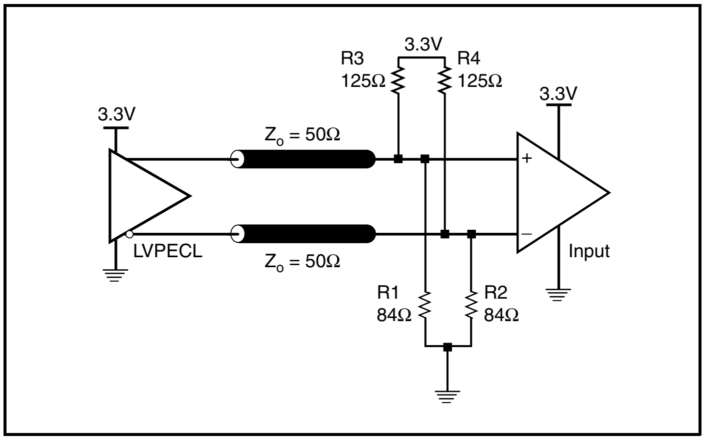


Figure 4B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 5A and *Figure 5B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CC} = 2.5V, the V_{CC} – 2V is very close to ground level. The R3 in Figure 5B can be eliminated and the termination is shown in *Figure 5C.*

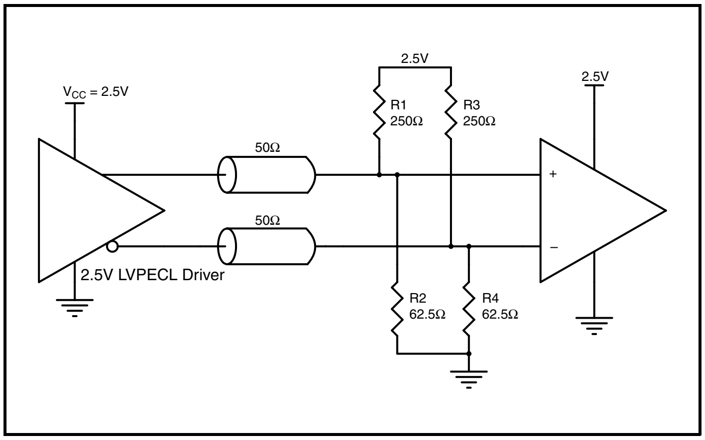


Figure 5A. 2.5V LVPECL Driver Termination Example

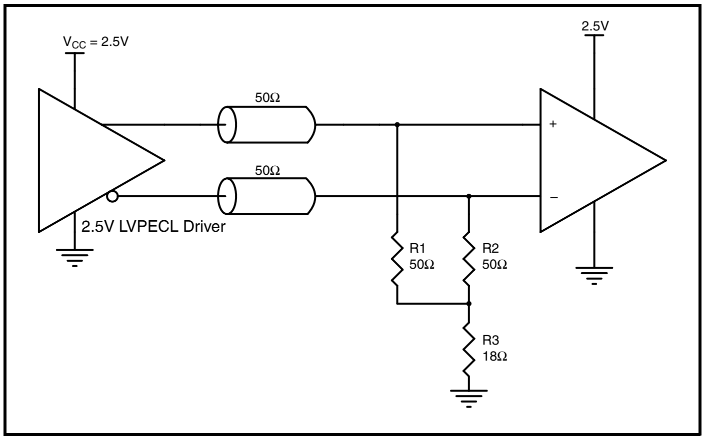


Figure 5B. 2.5V LVPECL Driver Termination Example

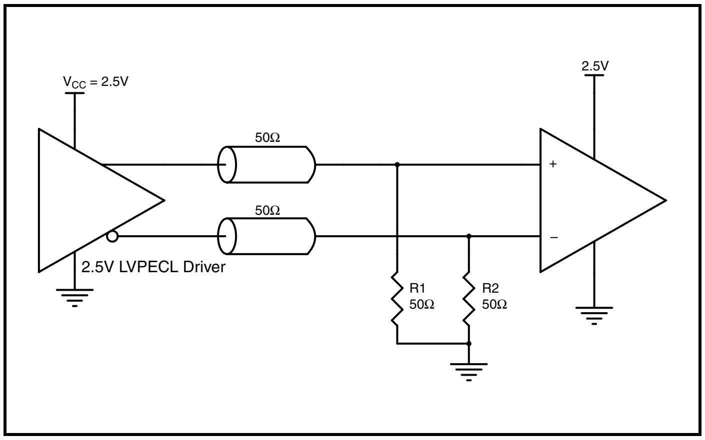


Figure 5C. 2.5V LVPECL Driver Termination Example

Application Schematic Example

Figure 6 shows an example of ICS8S73034I application schematic. In this example, the device is operated at V_{CC}= 3.3V. The decoupling capacitor should be located as close as possible to the power pin. The input is driven by a 3.3V LVPECL driver. For the LVPECL output drivers, only two terminations examples are shown in this schematic. More termination approaches are shown in the LVPECL Termination Application Note.

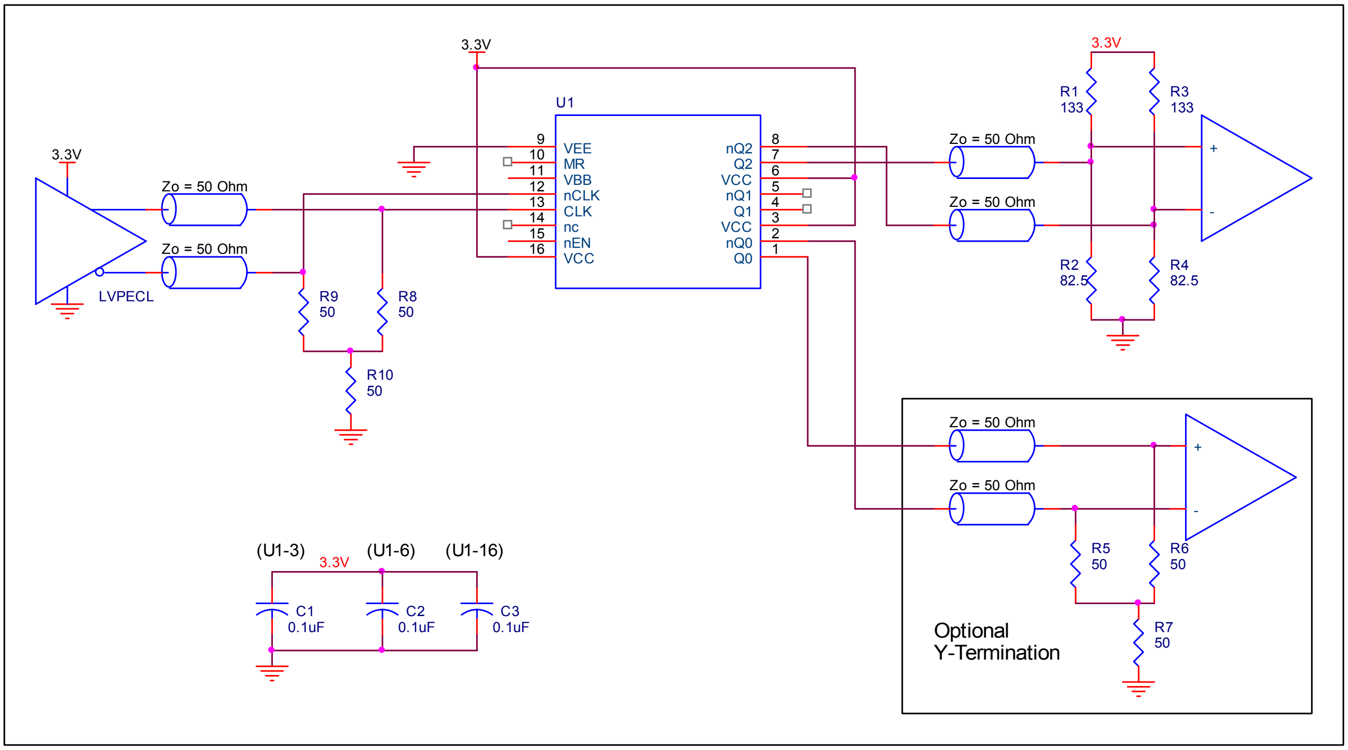


Figure 6. ICS8S73034I Application Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8S73034I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS8S73034I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.8V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.8V * 45mA = **171mW**
- Power $(outputs)_{MAX}$ = **30.3mW/Loaded Output pair**
  If all outputs are loaded, the total power is 3 * 30.3mW = **90.9mW**

Total Power$_{\_MAX}$ (3.8V, with all outputs switching) = 171mW + 90.9mW = **261.9mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 100°C/W per Table 6B below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.262W * 100°C/W = 111.2°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6A. Thermal Resistance θ_{JA} for 16 Lead SOIC Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70.2°C/W	64.7°C/W	61.6°C/W

Table 6B. Thermal Resistance θ_{JA} for 16 Lead TSSOP Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	100.0°C/W	94.2°C/W	90.2°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 7.*

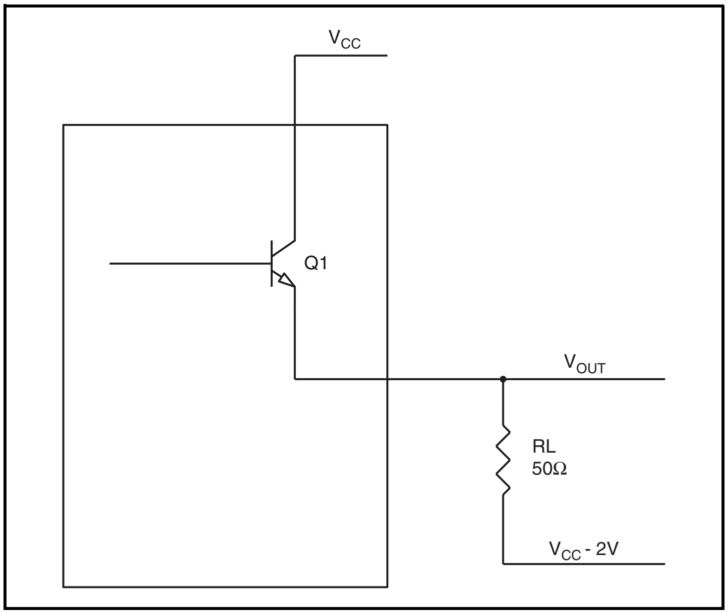


Figure 7. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC} - 2V$.

- For logic high, $V_{OUT} = V_{OH\_MAX} = V_{CC\_MAX} - 0.635V$
  $(V_{CC\_MAX} - V_{OH\_MAX}) = 0.635V$
- For logic low, $V_{OUT} = V_{OL\_MAX} = V_{CC\_MAX} - 1.59V$
  $(V_{CC\_MAX} - V_{OL\_MAX}) = 1.59V$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.635V)/50\Omega] * 0.635V = \mathbf{17.3mW}$

$Pd\_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.59V)/50\Omega] * 1.59V = \mathbf{13mW}$

Total Power Dissipation per output pair = Pd_H + Pd_L = **30.3mW**

Reliability Information

Table 7A. θ_{JA} vs. Air Flow Table for an 16 Lead SOIC

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70.2°C/W	64.7°C/W	61.6°C/W

Table 7B. θ_{JA} vs. Air Flow Table for an 16 Lead TSSOP Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	100.0°C/W	94.2°C/W	90.2°C/W

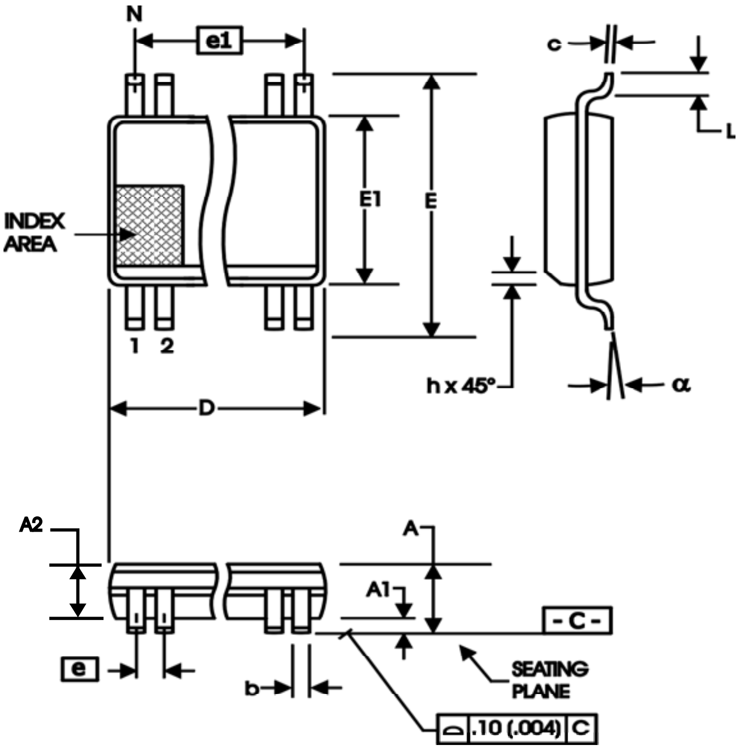
Transistor Count

The transistor count for ICS8S73034I is: 375

This device is pin and function compatible and a suggested replacement for ICS873034.

Package Outlines and Package Dimensions

Package Outline - G Suffix for 16 Lead TSSOP



Package Outline - M Suffix for 16 Lead SOIC

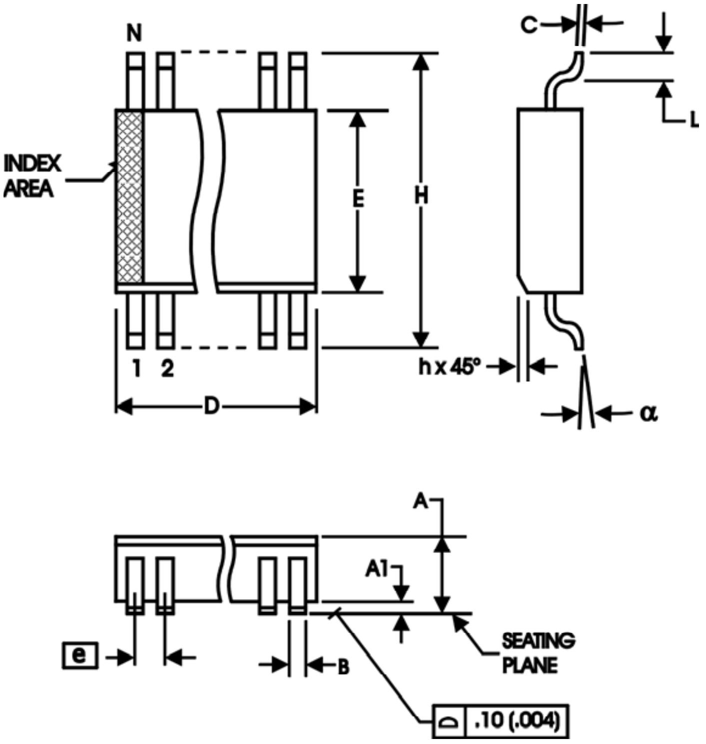


Table 8A. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	16	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Table 8B. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	16	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	9.80	10.00
E	3.80	4.00
e	1.27 Basic	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8S73034AMILF	8S73034AMIL	“Lead-Free” 16 Lead SOIC	Tube	-40°C to 85°C
8S73034AMILFT	8S73034AMIL	“Lead-Free” 16 Lead SOIC	1000 Tape & Reel	-40°C to 85°C
8S73034AGILF	73034AIL	“Lead-Free” 16 Lead TSSOP	Tube	-40°C to 85°C
8S73034AGILFT	73034AIL	“Lead-Free” 16 Lead TSSOP	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	1	2 8 9-10	Pin Description Table - corrected pin 1 as Q0 and pin 2 as nQ0. Updated *Wiring the Differential Input to Accept Single-ended Levels* section. Updated *LVPECL Clock Input Interface* sections.	11/8/10
A		1	Features Section - corrected Maximum input frequency bullet, from 2.8MHz to 3.2MHz.	6/8/11

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