DATASHEET

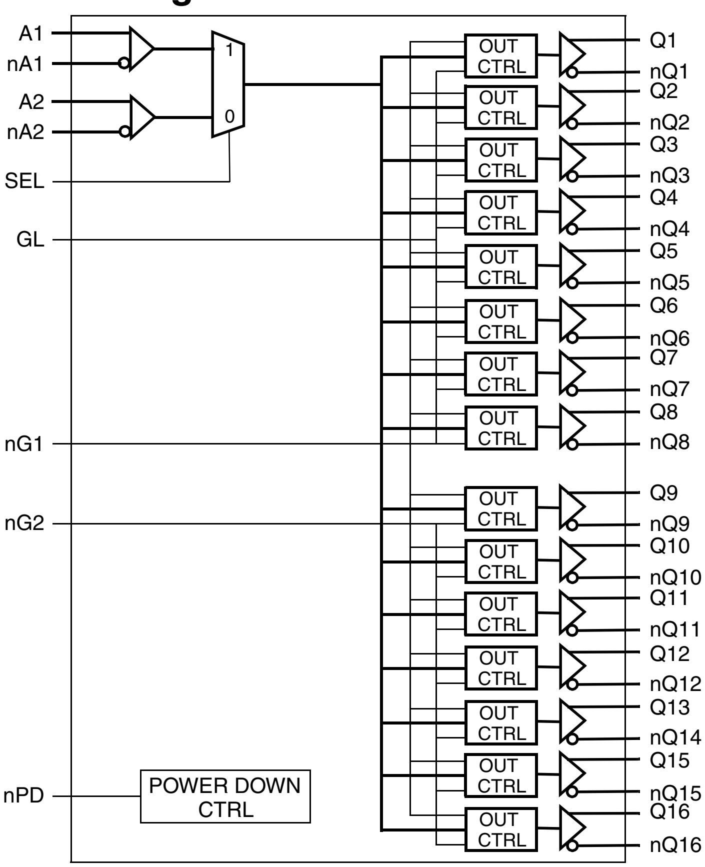
General Description

The 8T349316 is a 2.5V differential clock buffer with sixteen LVDS outputs. The fanout from a differential input to the sixteen LVDS outputs reduces loading on the preceding driver and provides an efficient clock distribution network. The 8T349316 can act as a translator from a differential HSTL, LVPECL, CML or LVDS input to LVDS output signals. A single-ended 3.3V, 2.5V LVCMOS/LVTTL input can also be used to translate to LVDS outputs. The redundant input capability allows for an asynchronous change-over from a primary clock source to a secondary clock source. Selectable reference inputs are controlled by SEL. The 8T349316 outputs can be asynchronously enabled/disabled. When disabled, the outputs will drive to the value selected by the GL pin. Multiple power and grounds reduce noise.The extended temperature range supports wireless infrastructure, telecommunication and networking end equipment requirements. The device is a member of the high-performance clock family from IDT.

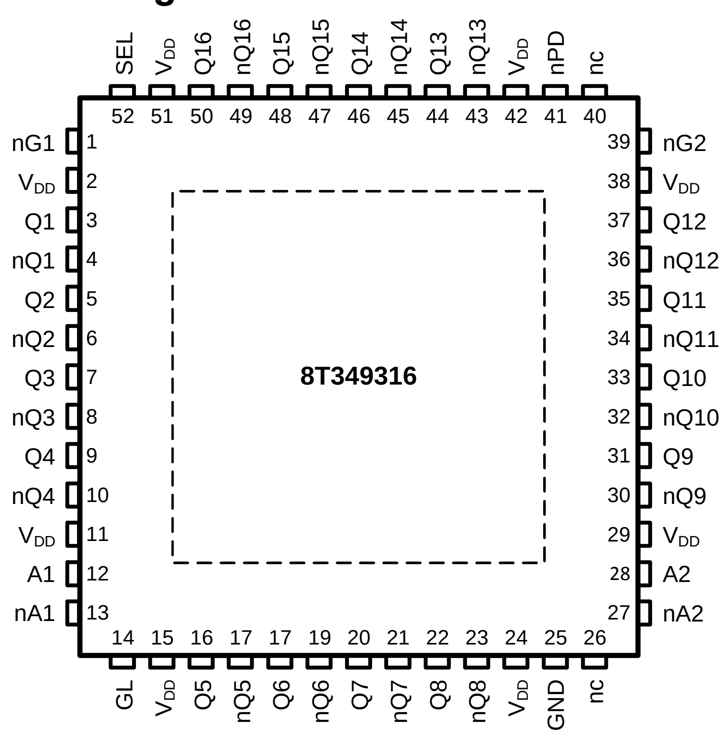
Features

- Clock signal selection and fanout to 16 LVDS outputs
- Guaranteed Low Skew < 50ps (max)
- Low output pulse skew < 125ps (max)
- Propagation delay < 1.75ns (max)
- Up to 1GHz clock signal operation
- Support the following input types: HSTL, LVPECL, HCSL, LVTTL
- Selectable differential input
- Power-down mode
- Full 2.5V power supply
- -40°C to +85°C ambient operating temperature
- Lead-free (RoHS 6) 52-lead VFQFN-P packaging
- Replacement device for the 5T9316

Block Diagram



Pin Assignment



52-lead VFQFN-P, EPad
8mm x 8mm x 0.9mm Package body
NL package
Top View

Pin Description and Pin Characteristic Tables

Table 1: Pin Descriptions

Number	Name	Type		Description
1	nG1	Input	-	Output enable control input for the Q[1:8] differential outputs. See *Table 3C*. LVCMOS/LVTTL interface levels.
2	V_{DD}	Power		Positive power supply voltage.
3	Q1	Output		Differential clock output Q1. LVDS interface signals.
4	nQ1	Output		Differential clock output Q1. LVDS interface signals.
5	Q2	Output		Differential clock output Q2. LVDS interface signals.
6	nQ2	Output		Differential clock output Q2. LVDS interface signals.
7	Q3	Output		Differential clock output Q3. LVDS interface signals.
8	nQ3	Output		Differential clock output Q3. LVDS interface signals.
9	Q4	Output		Differential clock output Q4. LVDS interface signals.
10	nQ4	Output		Differential clock output Q4. LVDS interface signals.
11	V_{DD}	Power		Positive power supply voltage.
12	A1	Input	-	Differential clock signal input 1.
13	nA1	Input	-	Differential clock signal input 1.
14	GL	Input	-	Control input for the output level for outputs in disable state. See *Table 3C* and *Table 3D*. LVCMOS/LVTTL interface levels.
15	V_{DD}	Power		Positive power supply voltage.
16	Q5	Output		Differential clock output Q5. LVDS interface signals.
17	nQ5	Output		Differential clock output Q5. LVDS interface signals.
18	Q6	Output		Differential clock output Q6. LVDS interface signals.
19	nQ6	Output		Differential clock output Q6. LVDS interface signals.
20	Q7	Output		Differential clock output Q7. LVDS interface signals.
21	nQ7	Output		Differential clock output Q7. LVDS interface signals.
22	Q8	Output		Differential clock output Q8. LVDS interface signals.
23	nQ8	Output		Differential clock output Q8. LVDS interface signals.
24	V_{DD}	Power		Positive power supply voltage.
25	GND	Power		Power Supply Ground.
26	nc	-	-	Not connected. It is recommended to connect this pin to board GND (0V).
27	nA2	Input	-	Differential clock signal input 2.
28	A2	Input	-	Differential clock signal input 2.
29	V_{DD}	Power		Positive power supply voltage.
30	nQ9	Output		Differential clock output Q9. LVDS interface signals.
31	Q9	Output		Differential clock output Q9. LVDS interface signals.
32	nQ10	Output		Differential clock output Q10. LVDS interface signals.
33	Q10	Output		Differential clock output Q10. LVDS interface signals.
34	nQ11	Output		Differential clock output Q11. LVDS interface signals.

Table 1: Pin Descriptions

Number	Name	Type		Description
35	Q11	Output		Differential clock output Q11. LVDS interface signals.
36	nQ12	Output		Differential clock output Q12. LVDS interface signals.
37	Q12	Output		Differential clock output Q12. LVDS interface signals.
38	V_{DD}	Power		Positive power supply voltage.
39	nG2	Input	-	Output enable control input for the Q[9:16] differential outputs. See *Table 3D*. LVCMOS/LVTTL interface levels.
40	nc	-	-	Not connected. It is recommended to connect this pin to board GND (0V).
41	nPD	Input	-	Device power-down control input. See *Table 3B*. LVCMOS/LVTTL interface levels.
42	V_{DD}	Power		Positive power supply voltage.
43	nQ13	Output		Differential clock output Q13. LVDS interface signals.
44	Q13	Output		Differential clock output Q13. LVDS interface signals.
45	nQ14	Output		Differential clock output Q14. LVDS interface signals.
46	Q14	Output		Differential clock output Q14. LVDS interface signals.
47	nQ15	Output		Differential clock output Q15. LVDS interface signals.
48	Q15	Output		Differential clock output Q15. LVDS interface signals.
49	nQ16	Output		Differential clock output Q16. LVDS interface signals.
50	Q16	Output		Differential clock output Q16. LVDS interface signals.
51	V_{DD}	Power		Positive power supply voltage.
52	SEL	Input		Reference input signal select control pin. See *Table 3A*. LVCMOS/LVTTL interface levels.
—	GND	Power		Exposed package ground supply voltage (GND). Connect to board GND.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance	GL, nG1, nG2, nPD, SEL			3	pF

Logic Truth Tables

Table 3A: Input Signal Source Select[1]

SEL	Input Selection
0	A2
1	A1

1. Asynchronous control.

Table 3B. Device Power-down control[1]

nPD	Power-down Operation
0	Power-down mode of the entire device. Input and outputs disable and the output voltage is V_{DD} (for each Q1, nQ1 to Q16, nQ16 pair)[2]
1	Normal 0peration

1. Asynchronous control.
2. Disable outputs by setting nG1 = nG2 = 1 before entering power-down mode and while in power-down mode. To enter normal device operation, first enable the outputs by setting nG1 = nG2 = 0 before setting nPD = 1.

Table 3C. Output Q[1:8] Enable Control[1]

GL	nG1	Q1 to Q8 Output State
X	0	Enabled (active)
0	1	Disabled, output state is logic low (Q[1:8] = L, nQ[1:8] = H)
1	1	Disabled, output state is logic high (Q[1:8] = H, nQ[1:8] = L)

1. Asynchronous controls.

Table 3D. Output Q[9:16] Enable Control[1]

GL	nG2	Q9 to Q16 Output State
X	0	Enabled (active)
0	1	Disabled, output state is logic low (Q[9:16] = L, nQ[9:16] = H)
1	1	Disabled, output state is logic high (Q[9:16] = H, nQ[9:16] = L)

1. Asynchronous controls.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4. Absolute Maximum Ratings

Item	Rating
Supply Voltage, V_{DD}	-0.5V to 3.6V
Input Voltage	-0.5V to 3.6V
Output Voltage	-0.5V to V_{DD} + 0.5V and <3.6V
Outputs, I_O (LVDS) Continuous Current Surge Current	 10mA 15mA
Storage Temperature	-65°C to 150°C
Thermal Junction Temperature, T_J	125°C

Table 5. Recommended Operating Range

Item	Minimum	Typical	Maximum	Units
Supply Voltage, V_{DD}	2.3	2.5	2.7	V
Ambient Temperature	-40		+85	°C

DC Electrical Characteristics

Table 6A. Power Supply DC Characteristics, V_{DD} = 2.5V±10%, T_A = -40°C to +85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.3	2.5	2.7	V
I_{DD}	Core and Output Power Supply Current	V_{DD} = 2.7V, f_{REF} = 1GHz			360	mA
I_{DDQ}	Core and Output Power Supply Current	V_{DD} = Maximum, A1, nA1 and A2, nA2 at Logic Low Level, Q[1:16] outputs Enabled			350	mA
$I_{DD, PD}$	Power-down Core and Output Power Supply Current	nPD = 0			5	mA

Table 6B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 2.5V ±10%, T_A = -40°C to +85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Voltage	nPD, nG1, nG2, GL	V_{DD} = 2.7V			150	µA
I_{IL}	Input Low Voltage	nPD, nG1, nG2, GL	V_{DD} = 2.7V	-10			µA
V_{IH}	DC Input High	nPD, nG1, nG2, GL		1.7		3.6	V
V_{IL}	DC Input Low	nPD, nG1, nG2, GL		-0.3		0.7	V

Table 6C. Differential Input DC Characteristics, V_{DD} = 2.5V ±10%, T_A = -40°C to +85°C [1]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Voltage	A1, nA1, A2, nA2	V_{DD} = 2.7V			150	µA
I_{IL}	Input Low Voltage	A1, nA1, A2, nA2	V_{DD} = 2.7V	-10			µA
V_{PP}	Peak-to-Peak Voltage[1]			0.15		3.6	V
V_{CMR}	Common Mode Input Voltage[1, 2]			0.5		V_{DD}	V

1. V_{IL} should not be less than -0.3V.
2. Common mode input voltage is defined at the crosspoint.

Table 6D. LVDS DC Characteristics, V_{DD} = 2.5V±10%, T_A = -40°C to +85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247		454	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.125	1.2	1.375	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV
IOS	Outputs Short Circuit Current	Q_X and nQ_X = 0V		12	24	mA
IOSD	Differential Outputs Short Circuit Current	Q_X = nQ_X		6	12	mA

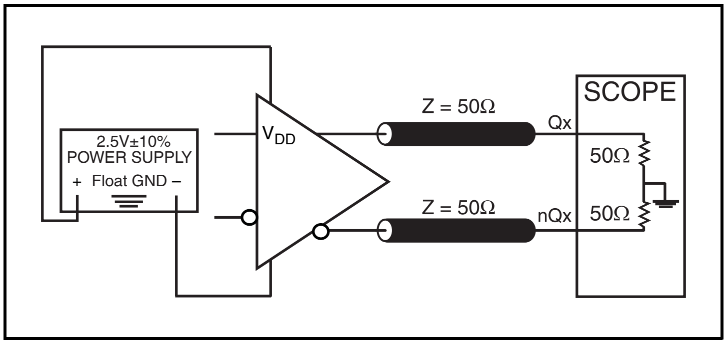
AC Electrical Characteristics

Table 7. AC Characteristics, V_{DD} = 2.5V±10%, T_A = -40°C to +85°C[1]

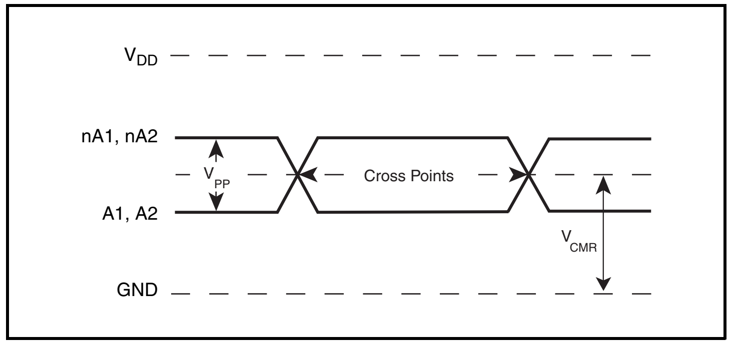
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	Q[1:16]				1	GHz
t_{PD}	Propagation Delay	LH and HL	A1, A2 to Q[1:16]		1.4	1.75	ns
		Output Enable	nG1, nG2 to Q[1:16]			3.5	ns
		Output Disable	nG1, nG2 to Q[1:16]			3.5	ns
		Powered-down	nPD to Q, nQ = V_{DD}			100	µs
		Powered-down	nPD to Q, nQ = Logic Level defined by the Selected Input			100	µs
*t*sk(o)	Output Skew[2 3]	Q[1:16]			12	50	ps
*t*sk(p)	Output Pulse Skew	Q[1:16]			20	125	ps
*t*sk(pp)	Part-to-Part Skew[4]	Q[1:16]				300	ps

1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
2. This parameter is defined in accordance with JEDEC standard 65.
3. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross point.
4. Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross point.

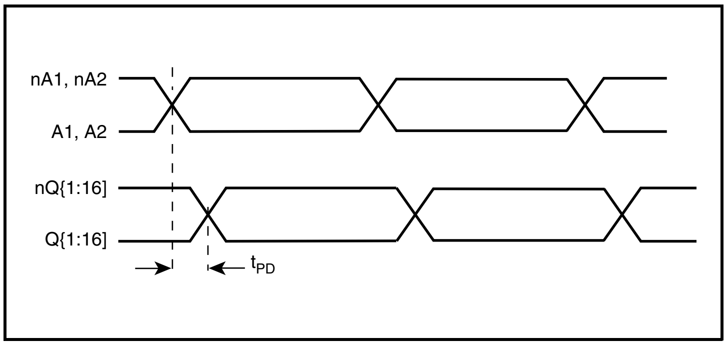
Parameter Measurement Information



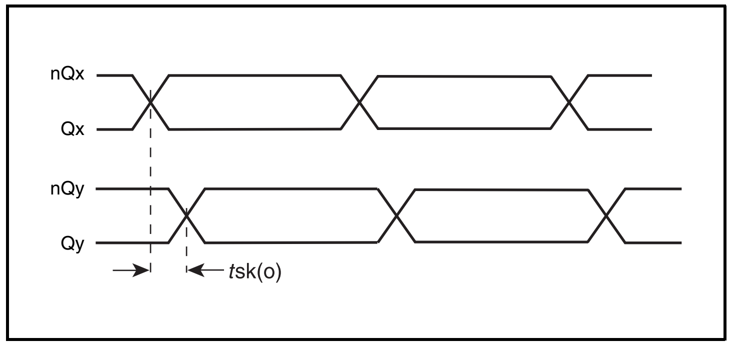
2.5V LVDS Output Load Test Circuit



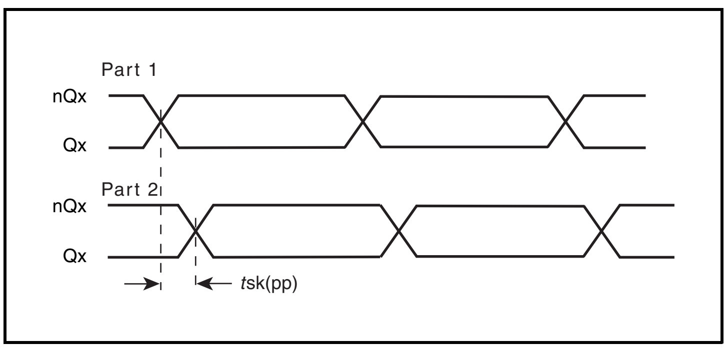
Differential Input Level



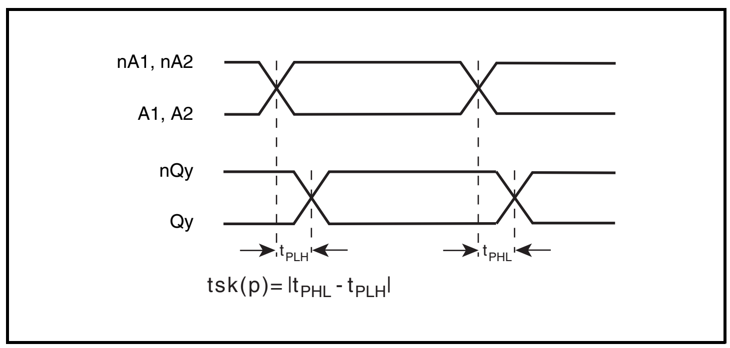
Propagation Delay



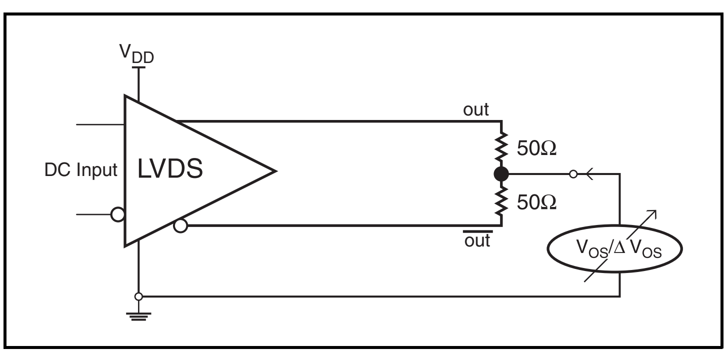
Output Skew



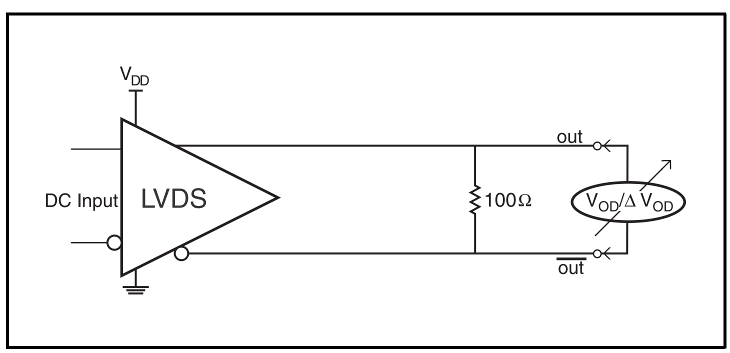
Part-to-Part Skew



Pulse Skew



Offset Voltage Setup



Differential Output Voltage Setup

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

Ax/nAx Clock Inputs

For applications not requiring the use of the differential input, Ax should be pulled up with a 10kΩ resistor and nAx pulled down with a 10kΩ resistor.

LVCMOS Control Pins

All control pins have internal pullup or pulldown resistors; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{DD} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

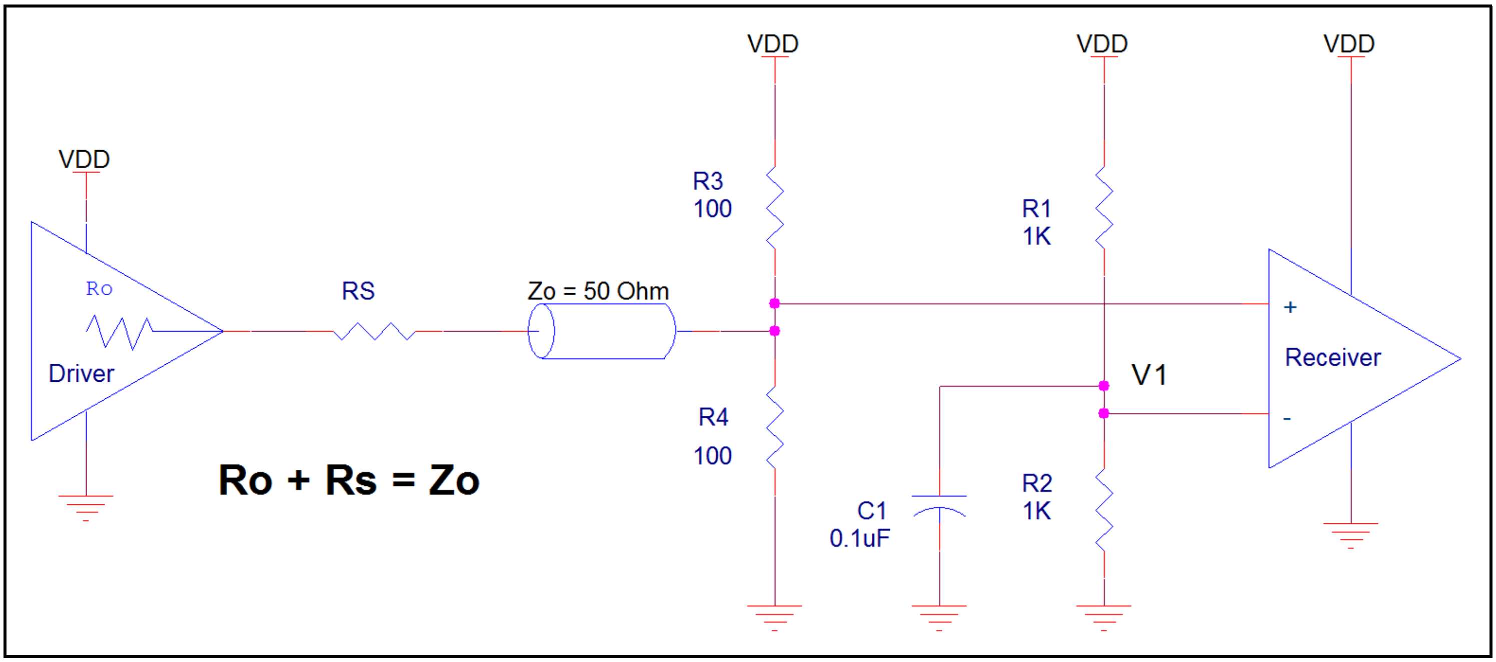


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels.

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 2A* can be used with either type of output structure. *Figure 2B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

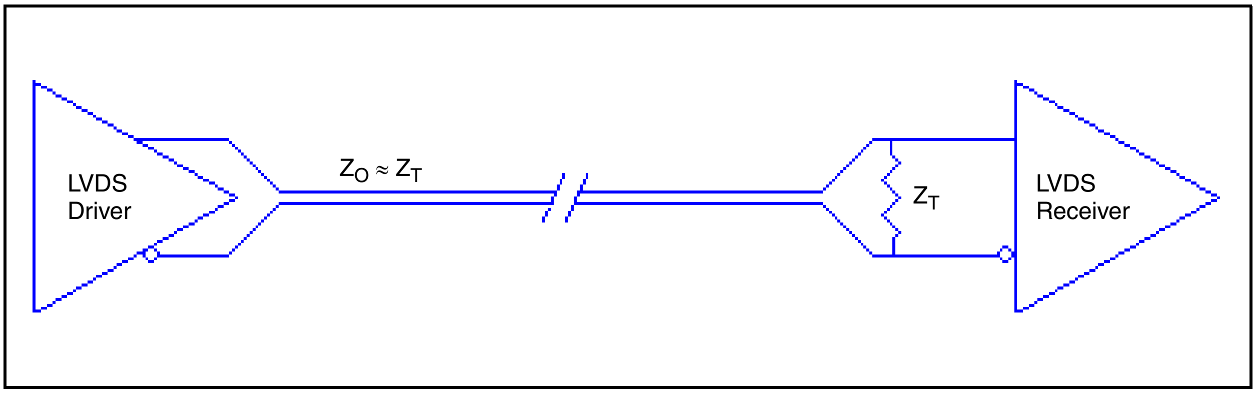


Figure 2A. Standard LVDS Termination

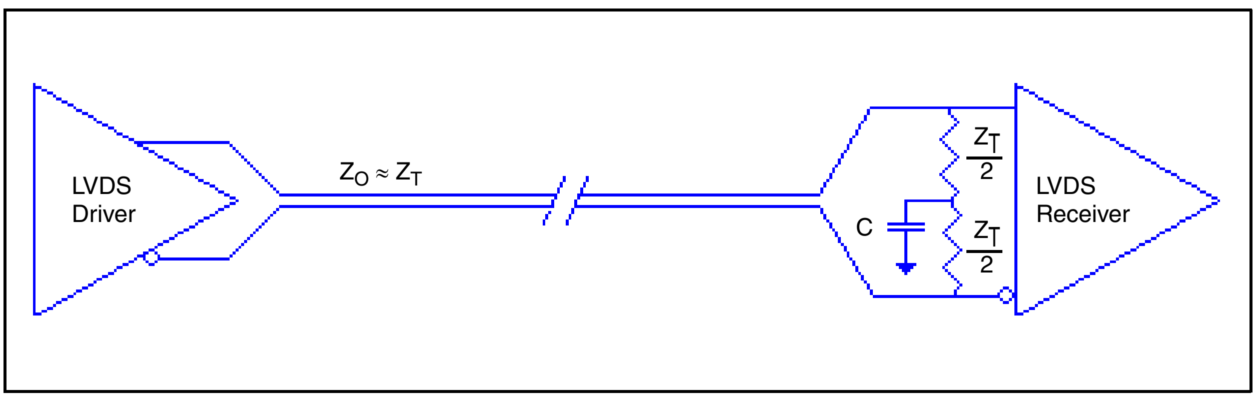


Figure 2B. Optional LVDS Termination

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 3*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor's Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

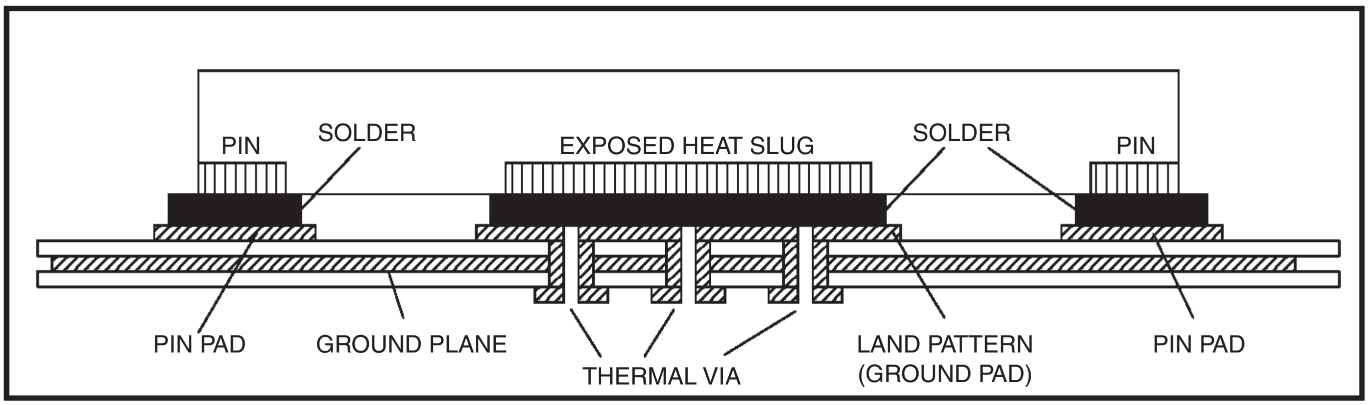


Figure 3. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale).

Power Considerations

This section provides information on power dissipation and junction temperature for the 8T349316. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8T349316 is the sum of the core power plus the output power dissipation due to the load. The following is the power dissipation for V_{DD} = 2.5V + 10% = 2.700V, which gives worst case results.

The maximum current at 85°C is as follows:

I_{DD_MAX} = 360mA

- Power $_{(core)MAX}$ = V_{DD_MAX} * I_{DD_MAX} = 2.7V * 360mA = **972mW**

Total Power$_{_MAX}$ = 972mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + TA

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 33°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.972W * 33°C/W = 117.1°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 52-Lead VFQFN, Forced Convection

θ_{JA} at 0 Air Flow			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	33.0°C/W	29.76°C/W	28.27°C/W

Reliability Information

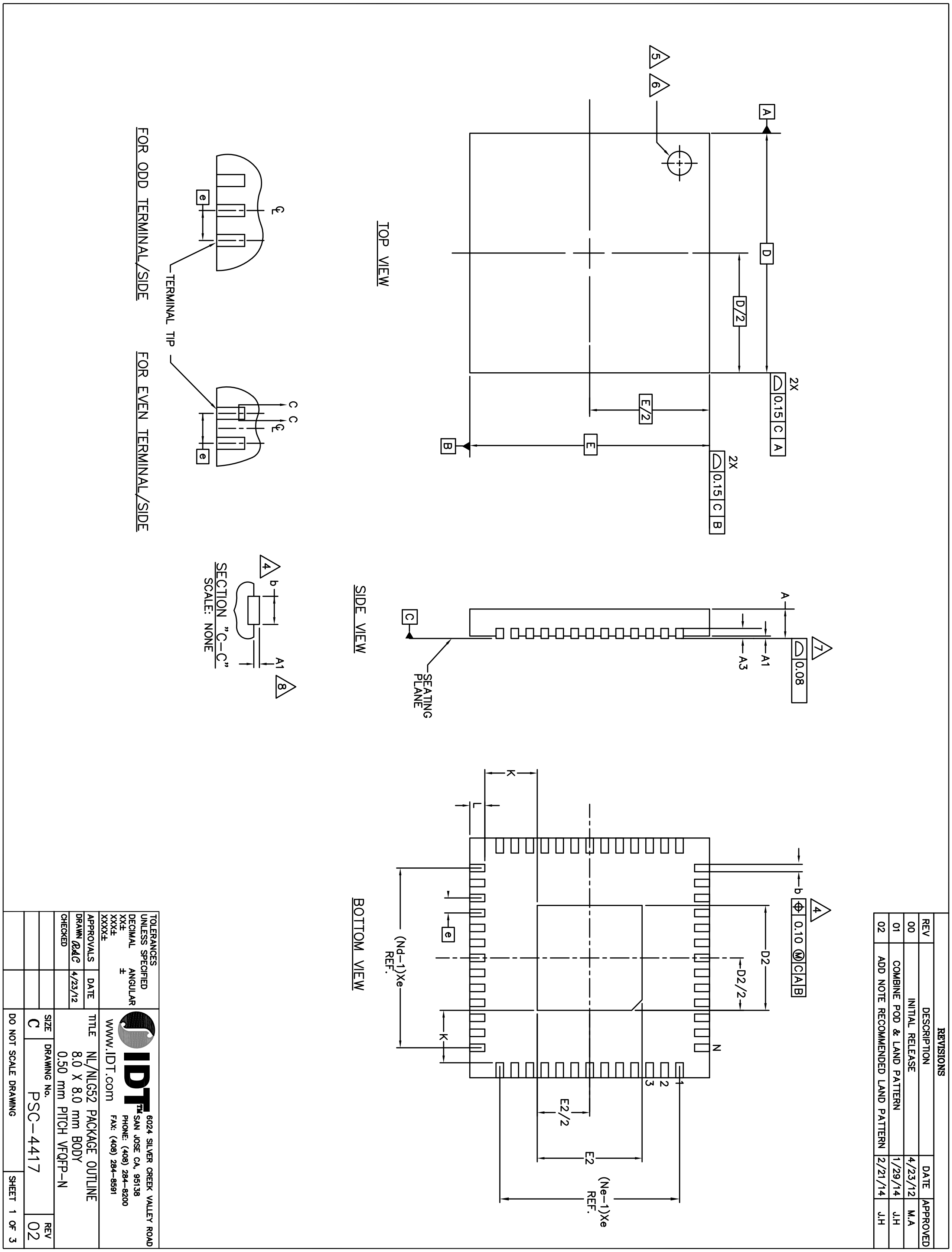
Table 8. θ_{JA} vs. Air Flow Table for a 52-lead VFQFN Package

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	33.0°C/W	29.76°C/W	28.27°C/W

Transistor Count

The transistor count for 8T349316 is: 1821

52-Lead VFQFN Package Outline



52-Lead VFQFN Package Outline, (continued)

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	4/23/12	M.A
01	COMBINE POD & LAND PATTERN	1/29/14	J.H
02	ADD NOTE RECOMMENDED LAND PATTERN	2/21/14	J.H

SYMBOL	VARIATION VLLD-4			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		52		2
Nd		13		2
Ne		13		2
L	0.45	0.50	0.55	
b	0.18	0.25	0.30	4
P		–		
D2	3.4	3.5	3.6	11
E2	3.4	3.5	3.6	11

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	7
A2	–	0.65	1.00	
A3		0.20 REF.		
D		8.00 BSC		
E		8.00 BSC		
k	0.20	–	–	

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M. – 1994.
2. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
3. ALL DIMENSIONS ARE IN MILLIMETERS.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.30mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST EXIST ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. APPLIED TO EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
8. APPLIED ONLY FOR TERMINALS.
9. NOT AN ACTUAL IO.
10. THIS OUTLINES CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO–220, VARIATION VLLD–1, VLLD–2, VLLD–4 & VLLD–5 WITH THE EXCEPTION OF D2 & E2.
11. DIMENSIONS D2 & E2 VARY DEPENDING ON DEVICE, SUPPLIER, ETC.

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
XX± ±
XXX±
XXXX±

IDT™ 6024 SILVER CREEK VALLEY ROAD SAN JOSE CA, 95138
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FAX: (408) 284-8591
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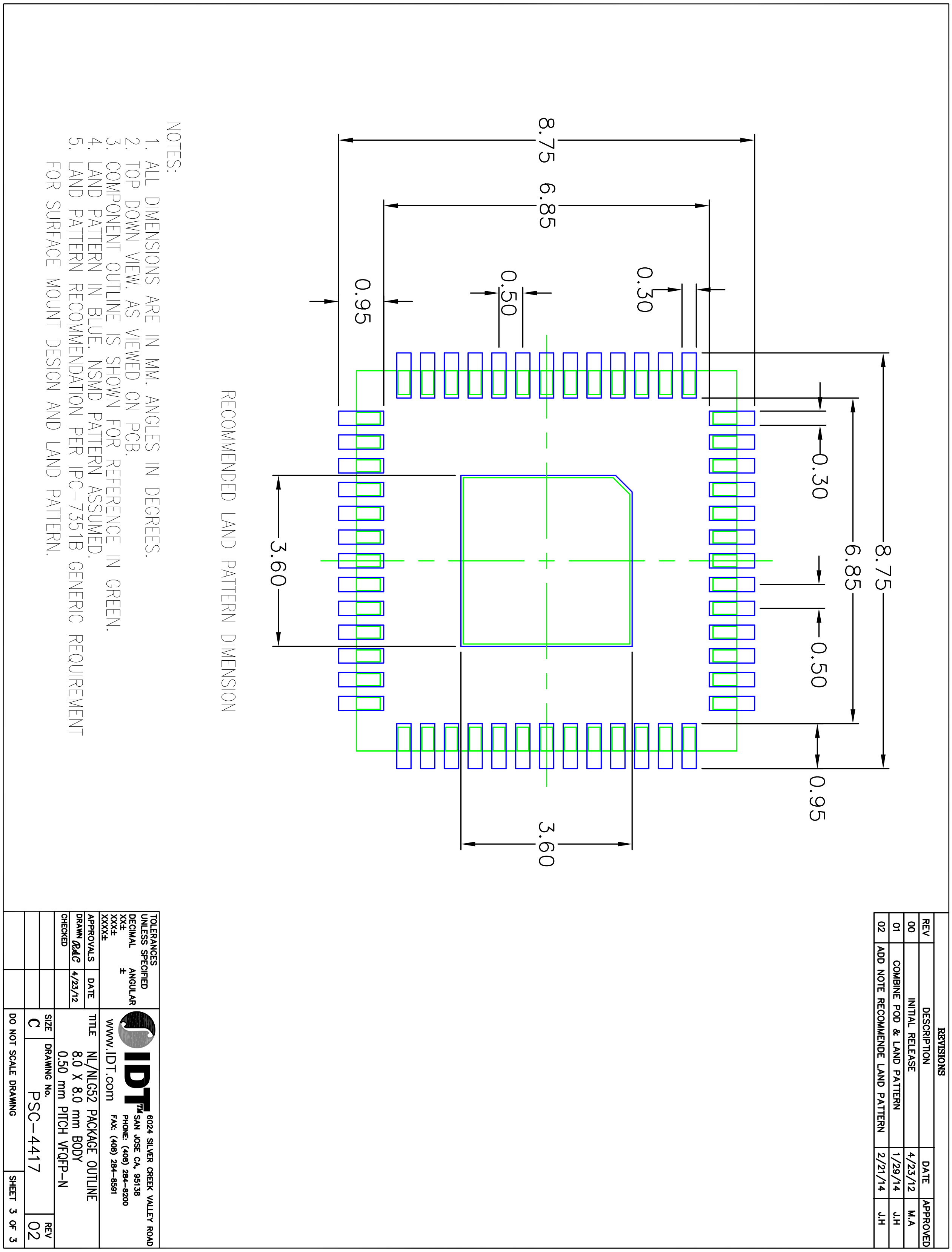
APPROVALS	DATE
DRAWN RAC	4/23/12
CHECKED	

TITLE NL/NLG52 PACKAGE OUTLINE
8.0 X 8.0 mm BODY
0.50 mm PITCH VFQFP–N

SIZE C | DRAWING No. PSC–4417 | REV 02

DO NOT SCALE DRAWING | SHEET 2 OF 3

52-Lead VFQFN Package Outline, (continued)



Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8T349316NLGI	IDT8T349316NLGI	“Lead-free” 52-lead VFQFN-P	Tray	-40°C to +85°C
8T349316NLGI8	IDT8T349316NLGI	“Lead-free” 52-lead VFQFN-P	Tape & Reel	-40°C to +85°C

Corporate Headquarters

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Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.