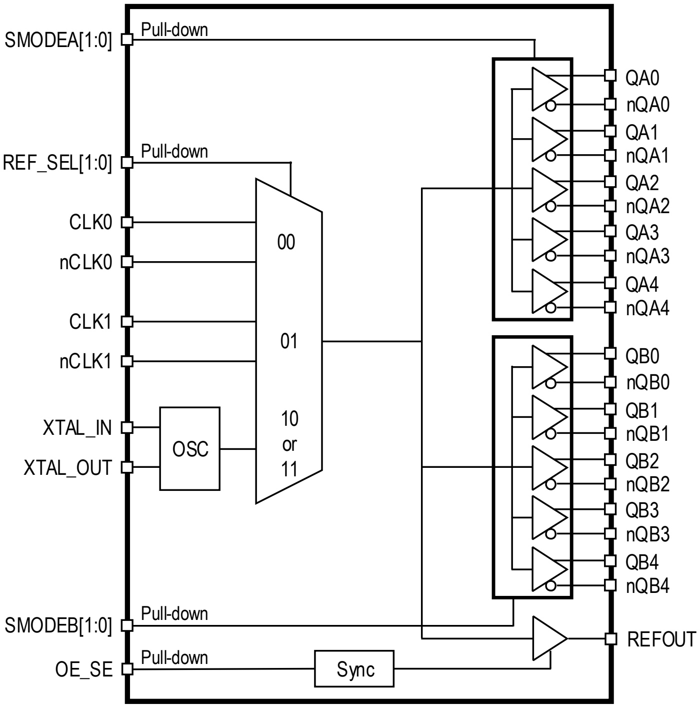
Description

The 8T39210 is a high-performance clock fanout buffer. The input clock can be selected from two differential inputs or one crystal input. The internal oscillator circuit is automatically disabled if the crystal input is not selected. The crystal pin can be driven by a single-ended clock. The selected signal is distributed to ten differential outputs that can be configured as LVPECL, LVDS, or HCSL outputs. In addition, an LVCMOS output is provided. All outputs can be disabled into a high-impedance state.

The device is designed for a signal fanout of high-frequency, low phase-noise clock and data signal. The outputs are at a defined level when inputs are open or tied to ground. It is designed to operate from a 3.3V or 2.5V core power supply, and either a 3.3V or 2.5V output operating supply.

Block Diagram

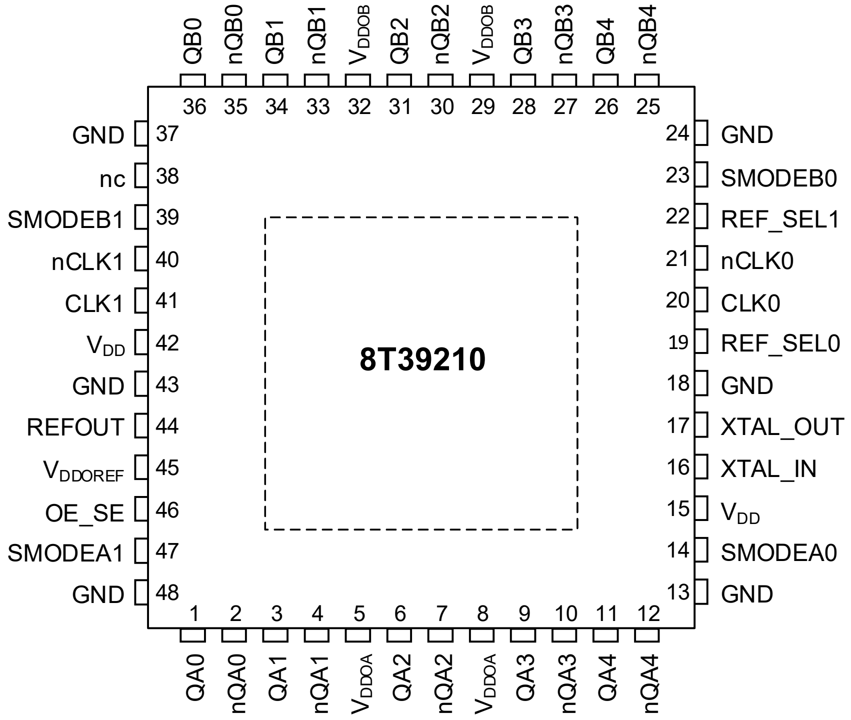


Features

- Two differential reference clock input pairs
- Differential input pairs can accept the following differential input levels: LVPECL, LVDS, HCSL, HSTL, or Single ended
- Crystal Input accepts 10MHz to 40MHz Crystal or Single-ended Clock
- Maximum Output Frequency
  - LVPECL - 1.5GHz
  - LVDS - 1.5GHz
  - HCSL - 750MHz
  - LVCMOS - 250MHz
- Two banks, each has five differential output pairs that can be configured as LVPECL, LVDS, or HCSL
- One single-ended reference output with synchronous enable to avoid clock glitch
- Output skew: 81ps (maximum)
  (Bank A and Bank B at the same output level)
- Part-to-part skew: 200ps (typical)
- Additive RMS phase jitter at 156.25MHz:
  37.6fs RMS (12kHz - 20MHz), typical at 3.3V/3.3V
- Supply voltage modes:
  - V_{DD}/V_{DDO}
  - 3.3V/3.3V
  - 3.3V/2.5V
  - 2.5V/2.5V
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) packaging

Contents

Pin Assignments



Pin Descriptions

Table 1. Pin Descriptions[a]

Number	Name	Type		Description
1	QA0	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
2	nQA0	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
3	QA1	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
4	nQA1	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
5	V_{DDOA}	Power		Output supply pins for Bank QA outputs.
6	QA2	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
7	nQA2	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
8	V_{DDOA}	Power		Output supply pins for Bank QA outputs.
9	QA3	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
10	nQA3	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
11	QA4	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
12	nQA4	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
13	GND	Power		Power supply ground.
14	SMODEA0	Input	Pulldown	Output driver select for Bank A outputs. See Table 8 for function. LVCMOS/LVTTL interface levels.
15	V_{DD}	Power		Power supply pin.
16	XTAL_IN	Input		Crystal oscillator interface.

Table 1. Pin Descriptions[a] (Cont.)

Number	Name	Type		Description
17	XTAL_OUT	Output		Crystal oscillator interface.
18	GND	Power		Power supply ground.
19	REF_SEL0	Input	Pulldown	Input clock selection. LVCMOS/LVTTL interface levels. See Table 3 for function.
20	CLK0	Input	Pullup/ Pulldown	Non-inverting differential clock. Internally biased to 0.33V_{DD}.
21	nCLK0	Input	Pullup/ Pulldown	Inverting differential clock. Internally biased to 0.4V_{DD}.
22	REF_SEL1	Input	Pulldown	Input clock selection. LVCMOS/LVTTL interface levels. See Table 3 for function.
23	SMODEB0	Input	Pulldown	Output driver select for Bank B outputs. See Table 9 for function. LVCMOS/LVTTL interface levels.
24	GND	Power		Power supply ground.
25	nQB4	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
26	QB4	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
27	nQB3	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
28	QB3	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
29	V_{DDOB}	Power		Output supply pins for Bank QB outputs.
30	nQB2	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
31	QB2	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
32	V_{DDOB}	Power		Output supply pins for Bank QB outputs.
33	nQB1	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
34	QB1	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
35	nQB0	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
36	QB0	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
37	GND	Power		Power supply ground.
38	nc	Unused		No connect pin.
39	SMODEB1	Input	Pulldown	Output driver select for Bank B outputs. See Table 9 for function. LVCMOS/LVTTL interface levels.
40	nCLK1	Input	Pullup/ Pulldown	Inverting differential clock. Internally biased to 0.4V_{DD}.
41	CLK1	Input	Pullup/ Pulldown	Non-inverting differential clock. Internally biased to 0.33V_{DD}.
42	V_{DD}	Power		Power supply pin.
43	GND	Power		Power supply ground.
44	REFOUT	Output		Single-ended reference clock output. LVCMOS/LVTTL interface levels.
45	V_{DDOREF}	Power		Output supply pin for REFOUT output.
46	OE_SE	Input	Pulldown	Output enable. LVCMOS/LVTTL interface levels (see Table 4).

Table 1. Pin Descriptions[a] (Cont.)

Number	Name	Type		Description
47	SMODEA1	Input	Pulldown	Output driver select for Bank A outputs. See Table 8 for function. LVCMOS/LVTTL interface levels.
48	GND	Power		Power supply ground.
ePad	$GND_{\_EP}$	Power		Connect ePad to ground to ensure proper heat dissipation.

[a] *Pulldown* and *Pullup* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Pin Characteristics

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Unit
C_{IN}	Input Capacitance	OE_SE, SMODEx[1:0], REF_SEL[1:0]			2		pF
$R_{PULLDOWN}$	Input Pulldown Resistor				50		kΩ
R_{PULLUP}	Input Pullup Resistor	CLK0, CLK1			100		kΩ
		nCLK0, nCLK1			75		kΩ
C_{PD}	Power Dissipation Capacitance	REFOUT	V_{DDOREF} = 3.465V		5.0		pF
		REFOUT	V_{DDOREF} = 2.625V		4.5		pF
R_{OUT}	Output Impedance	REFOUT	V_{DDOREF} = 3.3V		45		Ω
		REFOUT	V_{DDOREF} = 2.5V		58		Ω

Function Tables

Table 3. REF_SELx Function Table

Control Input	Selected Input Reference Clock
REF_SEL[1:0]	
00 (default)	CLK0, nCLK0
01	CLK1, nCLK1
10	XTAL
11	XTAL

Table 4. OE_SE Function Table[a]

OE_SE	REFOUT
0 (default)	High-Impedance
1	Enabled

[a] Synchronous output enable to avoid clock glitch.

Table 5. Input/Output Operation Table, OE_SE

Input Status			Output State
OE_SE	REF_SEL [1:0]	CLKx and nCLKx	REFOUT
0 (default)	Don’t care	Don’t Care	High Impedance
1	10 or 11	Don’t Care	Fanout crystal oscillator
1	00 (default)	CLK0 and nCLK0 are both open circuit	Logic Low
		CLK0 and nCLK0 are tied to ground	Logic Low
		CLK0 is high, nCLK0 is low	Logic High
		CLK0 is low, nCLK0 is high	Logic Low
1	01	CLK1 and nCLK1 are both open circuit	Logic Low
		CLK1 and nCLK1 are tied to ground	Logic Low
		CLK1 is high, nCLK1 is low	Logic High
		CLK1 is low, nCLK1 is high	Logic Low

Table 6. Input/Output Operation Table, SMODEA

Input Status			Output State
SMODEA[1:0]	REF_SEL[1:0]	CLKx and nCLKx	QA[4:0], nQA[4:0]
11	Don't care	Don't Care	High Impedance
00, 01 or 10	10 or 11	Don't Care	Fanout crystal oscillator
00, 01 or 10	00 (default)	CLK0 and nCLK0 are both open circuit	QA[4:0] = Low nQA[4:0] = High
		CLK0 and nCLK0 are tied to ground	QA[4:0] = Low nQA[4:0] = High
		CLK0 is high, nCLK0 is low	QA[4:0] = High nQA[4:0] = Low
		CLK0 is low, nCLK0 is high	QA[4:0] = Low nQA[4:0] = High
00, 01 or 10	01	CLK1 and nCLK1 are both open circuit	QA[4:0] = Low nQA[4:0] = High
		CLK1 and nCLK1 are tied to ground	QA[4:0] = Low nQA[4:0] = High
		CLK1 is high, nCLK1 is low	QA[4:0] = High nQA[4:0] = Low
		CLK1 is low, nCLK1 is high	QA[4:0] = Low nQA[4:0] = High

Table 7. Input/Output Operation Table, SMODEB

Input Status			Output State
SMODEB[1:0]	REF_SEL[1:0]	CLKx and nCLKx	QB[4:0], nQB[4:0]
11	Don't care	Don't Care	High Impedance
00, 01 or 10	10 or 11	Don't Care	Fanout crystal oscillator
00, 01 or 10	00 (default)	CLK0 and nCLK0 are both open circuit	QB[4:0] = Low nQB[4:0] = High
		CLK0 and nCLK0 are tied to ground	QB[4:0] = Low nQB[4:0] = High
		CLK0 is high, nCLK0 is low	QB[4:0] = High nQB[4:0] = Low
		CLK0 is low, nCLK0 is high	QB[4:0] = Low nQB[4:0] = High
00, 01 or 10	01	CLK1 and nCLK1 are both open circuit	QB[4:0] = Low nQB[4:0] = High
		CLK1 and nCLK1 are tied to ground	QB[4:0] = Low nQB[4:0] = High
		CLK1 is high, nCLK1 is low	QB[4:0] = High nQB[4:0] = Low
		CLK1 is low, nCLK1 is high	QB[4:0] = Low nQB[4:0] = High

Table 8. Output Level Selection Table, QA[0:4], nQA[0:4]

SMODEA1	SMODEA0	Output Type
0	0	LVPECL (default)
0	1	LVDS
1	0	HCSL
1	1	High-Impedance

Table 9. Output Level Selection Table, QB[0:4], nQB[0:4]

SMODEB1	SMODEB0	Output Type
0	0	LVPECL (default)
0	1	LVDS
1	0	HCSL
1	1	High-Impedance

Absolute Maximum Ratings

Exposure to absolute maximum rating conditions for extended periods may affect product reliability. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied.

Table 10. Absolute Maximum Ratings

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I XTAL_IN Other Inputs	 0V to 2V -0.5V to V_{DD} + 0.5V
Outputs, V_O, (HCSL, LVCMOS)	-0.5V to V_{DDOX}[a] + 0.5V
Outputs, I_O, (LVPECL) Continuous Current Surge Current	 50mA 100mA
Outputs, I_O, (LVDS) Continuous Current Surge Current	 10mA 15mA
Junction Temperature	150°C
Storage Temperature, T_{STG}	-65°C to 150°C
ESD - Human Body Mode[b]	2000V
ESD - Charged Device Mode[b]	500V

[a] V_{DDOX} denotes V_{DDOA}, V_{DDOB}.

[b] According to JEDEC/JSED JS-001-2012/22-C101 E.

Recommended Operating Conditions

Table 11. Recommended Operating Conditions[a]

Symbol	Parameter	Minimum	Typical	Maximum	Unit
T_A	Ambient air temperature	-40		85	°C
T_J	Junction temperature[b][c]			125	°C

[a] All conditions in the table must be met to guarantee device functionality.

[b] It is the user's responsibility to ensure that device junction temperature remains below the maximum allowed.

[c] The device is verified to the maximum operating junction temperature through simulation.

DC Electrical Characteristics

Table 12. Power Supply DC Characteristics, V_{DD} = 3.3V ±5, V_{DDOA} = V_{DDOB} = 3.3V ±5, GND = 0V, T_A = -40°C to 85°C[a]

Symbol	Parameter	Test Conditions			Minimum	Typical	Maximum	Unit
V_{DD}	Power Supply Voltage				3.135		3.465	V
V_{DDOA}, V_{DOOB}, V_{DDOREF}	Output Power Voltage				3.135		3.465	V
I_{DD}	Power Supply Current					34	38	mA
I_{EE}	Output Power Supply Current	SMODEA/B[1:0]=00 (default, LVPECL)	Outputs Unloaded	f_{OUT} = 156.25MHz		88	100	mA
				f_{OUT} = 781.25MHz		147	166	mA
				f_{OUT} = 1500MHz		181	205	mA

[a] V_{DDOX} denotes V_{DDOA}, V_{DDOB}

Table 13. Power Supply DC Characteristics, V_{DD} = 3.3V ±5 or 2.5V ±5, V_{DDOA} = V_{DDOA} = 2.5V ±5, GND = 0V, T_A = -40°C to 85°C[a]

Symbol	Parameter	Test Conditions			Minimum	Typical	Maximum	Unit
V_{DD}	Power Supply Voltage				2.375		3.465	V
V_{DDOA}, V_{DOOB}, V_{DDOREF}	Output Power Voltage				2.375		3.465	V
I_{DD}	Power Supply Current					34	38	mA
I_{EE}	Output Power Supply Current	SMODEA/B[1:0]=00 (default, LVPECL)	Outputs Unloaded	f_{OUT} = 156.25MHz		83	94	mA
				f_{OUT} = 781.25MHz		140	158	mA
				f_{OUT} = 1500MHz		181	205	mA

[a] V_{DDOX} denotes V_{DDOA}, V_{DDOB}

Table 14. Maximum Output Supply Current, V_{DDOX} = 3.3V ±5, or 2.5V ±5, GND = 0V, T_A = -40°C to 85°C[a]

Symbol	Parameter	Test Conditions		V_{DDOx} = 3.3 ±5%			V_{DDOx} = 2.5 ±5%			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{DDOA} + I_{DDOB}	Bank A & Bank B Current SMODEA/B[1:0]=00 (default; LVPECL)	Outputs Unloaded	f_{OUT} = 156.25MHz		44	51		43	50	mA
			f_{OUT} = 781.25MHz		99	114		99	114	mA
			f_{OUT} = 1500MHz		147	169		147	169	mA
		Outputs Loaded 50Ω to V_{DDOx} - 2V	f_{OUT} = 156.25MHz		243	279		217	249	mA
			f_{OUT} = 781.25MHz		306	352		262	301	mA
			f_{OUT} = 1500MHz		355	408		302	347	mA
I_{DDOA} + I_{DDOB}	Bank A & Bank B Current SMODEA/B[1:0]=01 (LVDS)	Outputs Unloaded	f_{OUT} = 156.25MHz		94	108		93	107	mA
			f_{OUT} = 468.75MHz		135	155		134	154	mA
			f_{OUT} = 800MHz		166	191		166	191	mA
		Outputs Loaded	f_{OUT} = 156.25MHz		91	105		91	105	mA
			f_{OUT} = 468.75MHz		127	146		128	147	mA
			f_{OUT} = 800MHz		165	189		165	190	mA
I_{DDOA} + I_{DDOB}	Bank A & Bank B Current SMODEA/B[1:0]=10 (HCSL)	Outputs Unloaded	f_{OUT} = 100MHz		42	48		41	47	mA
			f_{OUT} = 156.25MHz		48	55		46	53	mA
			f_{OUT} = 250MHz		57	66		55	64	mA
			f_{OUT} = 750MHz		105	118		103	117	mA
		Outputs Loaded	f_{OUT} = 100MHz		190	218		188	216	mA
			f_{OUT} = 156.25MHz		195	224		193	222	mA
			f_{OUT} = 250MHz		204	234		202	233	mA
			f_{OUT} = 750MHz		258	292		257	290	mA

[a] V_{DDOX} denotes V_{DDOA}, V_{DDOB}

Table 15. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ±5%, 2.5V ±5%, V_{DDOREF} = 3.3V ±5% or 2.5V ±5%, GND = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Unit
V_{IH}	Input High Voltage	OE_SE, SMODEA[1:0], SMODEB[1:0], REF_SEL[1:0]	V_{DD} = 3.3V±5%	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V±5%	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V±5%	-0.3		0.8	V
			V_{DD} = 2.5V±5%	-0.3		0.7	V
I_{IH}	Input High Current		V_{DD} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current		V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage	REFOUT	V_{DDOREF}= 3.3V±5%: I_{OH} = -1mA	2.6			V
			V_{DDOREF} = 2.5V±5%: I_{OH} = -1mA	1.8			V
V_{OL}	Output Low Voltage		V_{DDOREF} = 3.3V±5% or 2.5V±5%: I_{OL} = 1mA			0.5	V

Table 16. Differential DC Characteristics, V_{DD} = 3.3V ±5% or 2.5V ±5%, GND = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Unit
I_{IH}	Input High Current	CLK[0:1], nCLK[0:1]	V_{DD} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	CLK[0:1], nCLK[0:1]	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage[a]			0.240		1.3	V
V_{CMR}	Common Mode Input Voltage[a][b]			GND + 0.5		V_{DD} – 0.85	V

[a] Input voltage should not be less than -0.3V, and greater than V_{DD}.

[b] Common mode voltage is defined as the crosspoint.

Table 17. LVPECL DC Characteristics, V_{DD} = V_{DDOA} = V_{DDOB} = 3.3V ±5%, GND = 0V, T_A = -40°C to 85°C[a]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
V_{OH}	Output High Voltage[b]		V_{DDOX} - 1.135		V_{DDOX} - 0.8	V
V_{OL}	Output Low Voltage[b]		V_{DDOX} - 2.1		V_{DDOX} - 1.6	V
V_{SWING}	Peak-to-Peak Output Voltage Swing	DC ≤ f_{OUT} ≤ 500MHz	0.6		1.24	V
		500MHz < f_{OUT} ≤ 1GHz	0.4		1.10	V
		f_{OUT} > 1.0GHz		0.60		V

[a] V_{DDOX} denotes V_{DDOA} and V_{DDOB}.

[b] Outputs terminated with 50Ω to V_{DDOX} – 2V.

Table 18. LVPECL DC Characteristics, $V_{DD} = V_{DDOA} = V_{DDOB} = 3.3V \pm 5\%$, GND = 0V, $T_A = -40°C$ to 85°C[a]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
V_{OH}	Output High Voltage[b]		V_{DDOX} - 1.125		V_{DDOX} - 0.8	V
V_{OL}	Output Low Voltage[b]		V_{DDOX} - 2.1		V_{DDOX} - 1.6	V
V_{SWING}	Peak-to-Peak Output Voltage Swing	DC ≤ f_{OUT} ≤ 500MHz	0.6		1.20	V
		500MHz < f_{OUT} ≤ 1GHz	0.4		1.00	V
		f_{OUT} > 1.0GHz		0.56		V

[a] V_{DDOX} denotes V_{DDOA} and V_{DDOB}.

[b] Outputs terminated with 50Ω to V_{DDOX} – 2V.

Table 19. LVDS DC Characteristics, $V_{DDOA} = V_{DDOB} = 3.3V \pm 5\%$, GND = 0V, $T_A = -40°C$ to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
V_{OD}	Differential Output Voltage		435		570	mV
ΔV_{OD}	V_{OD} Magnitude Change			50		mV
V_{OS}	Offset Voltage		1.16		1.375	V
ΔV_{OS}	V_{OS} Magnitude Change			50		mV

Table 20. LVDS DC Characteristics, $V_{DDOA} = V_{DDOB} = 2.5V \pm 5\%$, GND = 0V, $T_A = -40°C$ to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
V_{OD}	Differential Output Voltage		425		570	mV
ΔV_{OD}	V_{OD} Magnitude Change			50		mV
V_{OS}	Offset Voltage		1.15		1.365	V
ΔV_{OS}	V_{OS} Magnitude Change			50		mV

Table 21. Crystal Characteristics[a]

Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
Mode of Oscillation			Fundamental		
Frequency		10		40	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Capacitive Loading (C_L)			12	18	pF

[a] Crystal operation requires tuning caps. For more information, see Applications Information.

AC Electrical Characteristics

Table 22. AC Characteristics, $V_{DD} = V_{DDOA} = V_{DDOB} = V_{DDOREF} = 3.3V \pm 5\%$, GND = 0V, T_A = -40°C to 85°C[a][b]

Symbol	Parameter		Test Conditions		Minimum	Typical	Maximum	Unit
f_{OUT}	Output Frequency	LVPECL Outputs			DC		1500	MHz
		LVDS Outputs			DC		800	MHz
		HCSL Outputs			DC		750	MHz
		LVCMOS (REFOUT)			DC		250	MHz
t_{jit}	Buffer Additive Phase Jitter, RMS: Integration Range 12kHz - 20MHz REF_SEL[1:0] = 00 or 01		Clock Frequency = 156.25MHz; Input Clock from 8T49NS010A, Input Clock Jitter = 83.9fs; SMODEA/B[1:0] = 00 (default, LVPECL)			37.6		fs
tjit(Ø)	RMS Phase Jitter; 25MHz Integration Range: 100Hz - 1MHz		REF_SEL[1:0] = 10 or 11[c]			0.307		ps
NF	Noise Floor	LVPECL Outputs	Offset Frequency > 10MHz; 156.25MHz Clock Frequency			-159.5		dBc/Hz
		LVDS Outputs				-157.9		dBc/Hz
		HCSL Outputs				-157.7		dBc/Hz
t_{PD}	Propagation Delay[d]	CLK0, nCLK0 or CLK1, nCLK1 to any Qx, nQx Outputs	SMODEA/B[1:0] = 00 (default, LVPECL)	$f_{OUT} \leq$ 1GHz	0.75		1.50	ns
				f_{OUT} > 1GHz		1.23		ns
			SMODEA/B[1:0] = 01 (LVDS)		0.820		1.475	ns
			SMODEA/B[1:0] = 10 (HCSL)		0.860		1.440	ns
tsk(o)	Output Skew[e][f]						81	ps
tsk(pp)	Part-to-Part Skew[f][g]					200		ps
V_{OH}	Voltage High[h][i]	HCSL Outputs	$R_T = 50\Omega$ to GND, $C_L \leq 5pF$		520		931	mV
V_{OL}	Voltage Low[h][j]	HCSL Outputs			-150		150	mV
V_{CROSS}	Absolute Crossing Voltage[h][k][l]	HCSL Outputs			225		460	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all Edges[h][k][m]	HCSL Outputs					140	mV
	Rise/Fall Edge Rate[c][n][o]	HCSL Outputs			0.6		4.0	V/ns
t_R / t_F	Output Rise/Fall Time	LVPECL Outputs	20% to 80%			200	695	ps
		LVDS Outputs	20% to 80%			230	510	ps
		HCSL Outputs	20% to 80%			260	420	ps
		REFOUT	20% to 80%			438	575	ps
odc	Output Duty Cycle[p]		With Crystal Input		45		55	%
			With External 50%/ 50% Duty Cycle Clock Input		45		55	%
$MUX_{\_ISOLATION}$	MUX Isolation		156.25MHz			75		dB

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] LVPECL parameters characterized up to 1.5GHz. LVDS parameters characterized up to 800MHz. HCSL parameters characterized up to 750MHz.

[c] Measurement taken from differential waveform.

[d] Measured from the differential input crosspoint to the differential output crosspoint.

[e] Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential crosspoint.

[f] This parameter is defined in accordance with JEDEC Standard 65.

[g] Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential crosspoint

[h] Measurement taken from single-ended waveform.

[i] Vlow is defined as the statistical average Low value as obtained by using the oscilloscope Vlow Math function.

[j] Vhigh is defined as the statistical average High value as obtained by using the oscilloscope Vhigh Math function.

[k] Measured at crosspoint where the instantaneous voltage value of the rising edge of Qx equals the falling edge of nQx.

[l] Refers to the total variation from the lowest crosspoint to the highest, regardless of which edge is crossing. Refers to all crosspoint for this measurement.

[m] Defined as the total variation of all crossing voltages of rising Qx and falling nQx, This is the maximum allowed variance in Vcross for any particular system.

[n] Measured from -150mV to +150mV on the differential waveform (Qx minus nQx). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

[o] Measured at 100MHz.

[p] Measured for the following frequencies: 25MHz, 100MHz, 125MHz, 156.25MHz, 312.5MHz, 400MHz, 644.5313MHz, and 750MHz.

Table 23. AC Characteristics, V_{DD} = 3.3V ±5%, V_{DDOA} = V_{DDOB} = V_{DDOREF} = 2.5V ±5%, GND = 0V, T_A = -40°C to 85°C[a][b]

Symbol	Parameter		Test Conditions		Minimum	Typical	Maximum	Unit
f_{OUT}	Output Frequency	LVPECL Outputs			DC		1500	MHz
		LVDS Outputs			DC		800	MHz
		HCSL Outputs			DC		750	MHz
		LVCMOS (REFOUT)			DC		250	MHz
t_{jit}	Buffer Additive Phase Jitter, RMS: Integration Range 12kHz - 20MHz REF_SEL[1:0] = 00 or 01		Clock Frequency = 156.25MHz; Input Clock from 8T49NS010A, Input Clock Jitter = 83.9fs; SMODEA/B[1:0] = 00 (default, LVPECL)			45.5		fs
tjit(Ø)	RMS Phase Jitter; 25MHz Integration Range: 100Hz - 1MHz		REF_SEL[1:0] = 10 or 11[c]			0.309		ps
NF	Noise Floor	LVPECL	Offset Frequency > 10MHz; 156.25MHz Clock Frequency			-158.5		dBc/Hz
		LVDS				-158.1		dBc/Hz
		HCSL				-157.6		dBc/Hz
t_{PD}	Propagation Delay[d]	CLK0, nCLK0 or CLK1, nCLK1 to any Qx, nQx Outputs	SMODEA/B[1:0] = 00 (default, LVPECL)	f_{OUT} ≤ 1GHz	0.58		1.66	ns
				f_{OUT} > 1GHz		1.23		ns
			SMODEA/B[1:0] = 01 (LVDS)		0.75		1.50	ns
			SMODEA/B[1:0] = 10 (HCSL)		0.87		1.43	ns
tsk(o)	Output Skew[e][f]						75	ps
tsk(pp)	Part-to-Part Skew[f][g]					200		ps
V_{OH}	Voltage High[h][i]	HCSL Outputs	R_T = 50Ω to GND, C_L ≤ 5pF		520		931	mV
V_{OL}	Voltage Low[h][j]	HCSL Outputs			-150		150	mV
V_{CROSS}	Absolute Crossing Voltage[h][k][l]	HCSL Outputs			225		460	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all Edges[h][k][m]	HCSL Outputs					140	mV
	Rise/Fall Edge Rate[c][n][o]	HCSL Outputs			0.6		4	V/ns
t_R / t_F	Output Rise/Fall Time	LVPECL Outputs	20% to 80%			130	450	ps
		LVDS Outputs	20% to 80%			225	475	ps
		HCSL Outputs	20% to 80%			275	485	ps
		REFOUT	20% to 80%			434	600	ps
odc	Output Duty Cycle[p]		With Crystal Input		45		55	%
			With external 50%/ 50% Duty Cycle Clock Input		45		55	%
$MUX_{\_ISOLATION}$	MUX Isolation		156.25MHz			75		dB

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] LVPECL parameters characterized up to 1.5GHz. LVDS parameters characterized up to 800MHz. HCSL parameters characterized up to 750MHz.

[c] Measurement taken from differential waveform.

[d] Measured from the differential input crosspoint to the differential output crosspoint.

[e] Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential crosspoint.

[f] This parameter is defined in accordance with JEDEC Standard 65.

[g] Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential crosspoint

[h] Measurement taken from single-ended waveform.

[i] Vlow is defined as the statistical average Low value as obtained by using the oscilloscope Vlow Math function.

[j] Vhigh is defined as the statistical average High value as obtained by using the oscilloscope Vhigh Math function.

[k] Measured at crosspoint where the instantaneous voltage value of the rising edge of Qx equals the falling edge of nQx.

[l] Refers to the total variation from the lowest crosspoint to the highest, regardless of which edge is crossing. Refers to all crosspoint for this measurement.

[m] Defined as the total variation of all crossing voltages of rising Qx and falling nQx, This is the maximum allowed variance in Vcross for any particular system.

[n] Measured from -150mV to +150mV on the differential waveform (Qx minus nQx). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

[o] Measured at 100MHz.

[p] Measured for the following frequencies: 25MHz, 100MHz, 125MHz, 156.25MHz, 312.5MHz, 400MHz, 644.5313MHz, and 750MHz.

Table 24. AC Characteristics, V_{DD} = V_{DDOA} = V_{DDOB} = V_{DDOREF} = 2.5V ±5%, GND = 0V, T_A = -40°C to 85°C[a][b]

Symbol	Parameter		Test Conditions		Minimum	Typical	Maximum	Unit
f_{OUT}	Output Frequency	LVPECL Outputs			DC		1500	MHz
		LVDS Outputs			DC		800	MHz
		HCSL Outputs			DC		750	MHz
		LVCMOS (REFOUT)			DC		250	MHz
t_{jit}	Buffer Additive Phase Jitter, RMS: Integration Range 12kHz - 20MHz REF_SEL[1:0] = 00 or 01		Clock Frequency = 156.25MHz; Input Clock from 8T49NS010A, Input Clock Jitter = 83.9fs; SMODEA/B[1:0] = 00 (default, LVPECL)			46.9		fs
tjit(Ø)	RMS Phase Jitter; 25MHz Integration Range: 100Hz - 1MHz		REF_SEL[1:0] = 10 or 11[c]			0.313		ps
NF	Noise Floor	LVPECL	Offset Frequency > 10MHz; 156.25MHz Clock Frequency			-159.3		dBc/Hz
		LVDS				-157.9		dBc/Hz
		HCSL				-157.8		dBc/Hz
t_{PD}	Propagation Delay[d]	CLK0, nCLK0 or CLK1, nCLK1 to any Qx, nQx Outputs	SMODEA/B[1:0] = 00 (default, LVPECL)	f_{OUT} ≤ 1GHz	0.63		1.6	ns
				f_{OUT} > 1GHz		1.23		ns
			SMODEA/B[1:0] = 01 (LVDS)		0.825		1.6	ns
			SMODEA/B[1:0] = 10 (HCSL)		0.865		1.5	ns
*t*sk(o)	Output Skew[e][f]						75	ps
*t*sk(pp)	Part-to-Part Skew[f][g]					200		ps
V_{OH}	Voltage High[h][i]	HCSL Outputs	R_T = 50Ω to GND, C_L ≤ 5pF		520		920	mV
V_{OL}	Voltage Low[h][j]	HCSL Outputs			-150		150	mV
V_{CROSS}	Absolute Crossing Voltage[k][l]	HCSL Outputs			225		460	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all Edges[h][k][m]	HCSL Outputs					140	mV
	Rise/Fall Edge Rate[c][n][o]	HCSL Outputs			0.6		4	V/ns
t_R / t_F	Output Rise/Fall Time	LVPECL Outputs	20% to 80%			200	525	ps
		LVDS Outputs	20% to 80%			220	485	ps
		HCSL Outputs	20% to 80%			265	485	ps
		REFOUT	20% to 80%			432	625	ps
odc	Output Duty Cycle[p]		With Crystal Input		45		55	%
			With external 50%/ 50% Duty Cycle Clock Input		45		55	%
$MUX_{\_ISOLATION}$	MUX Isolation		156.25MHz			75		dB

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] LVPECL parameters characterized up to 1.5GHz. LVDS parameters characterized up to 800MHz. HCSL parameters characterized up to 750MHz.

[c] Measurement taken from differential waveform.

[d] Measured from the differential input crosspoint to the differential output crosspoint.

[e] Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential crosspoint.

[f] This parameter is defined in accordance with JEDEC Standard 65.

[g] Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential crosspoint

[h] Measurement taken from single-ended waveform.

[i] Vlow is defined as the statistical average Low value as obtained by using the oscilloscope Vlow Math function.

[j] Defined as the minimum instantaneous voltage including undershoot.

[k] Measured at crosspoint where the instantaneous voltage value of the rising edge of Qx equals the falling edge of nQx.

[l] Refers to the total variation from the lowest crosspoint to the highest, regardless of which edge is crossing. Refers to all crosspoint for this measurement.

[m] Defined as the total variation of all crossing voltages of rising Qx and falling nQx, This is the maximum allowed variance in Vcross for any particular system.

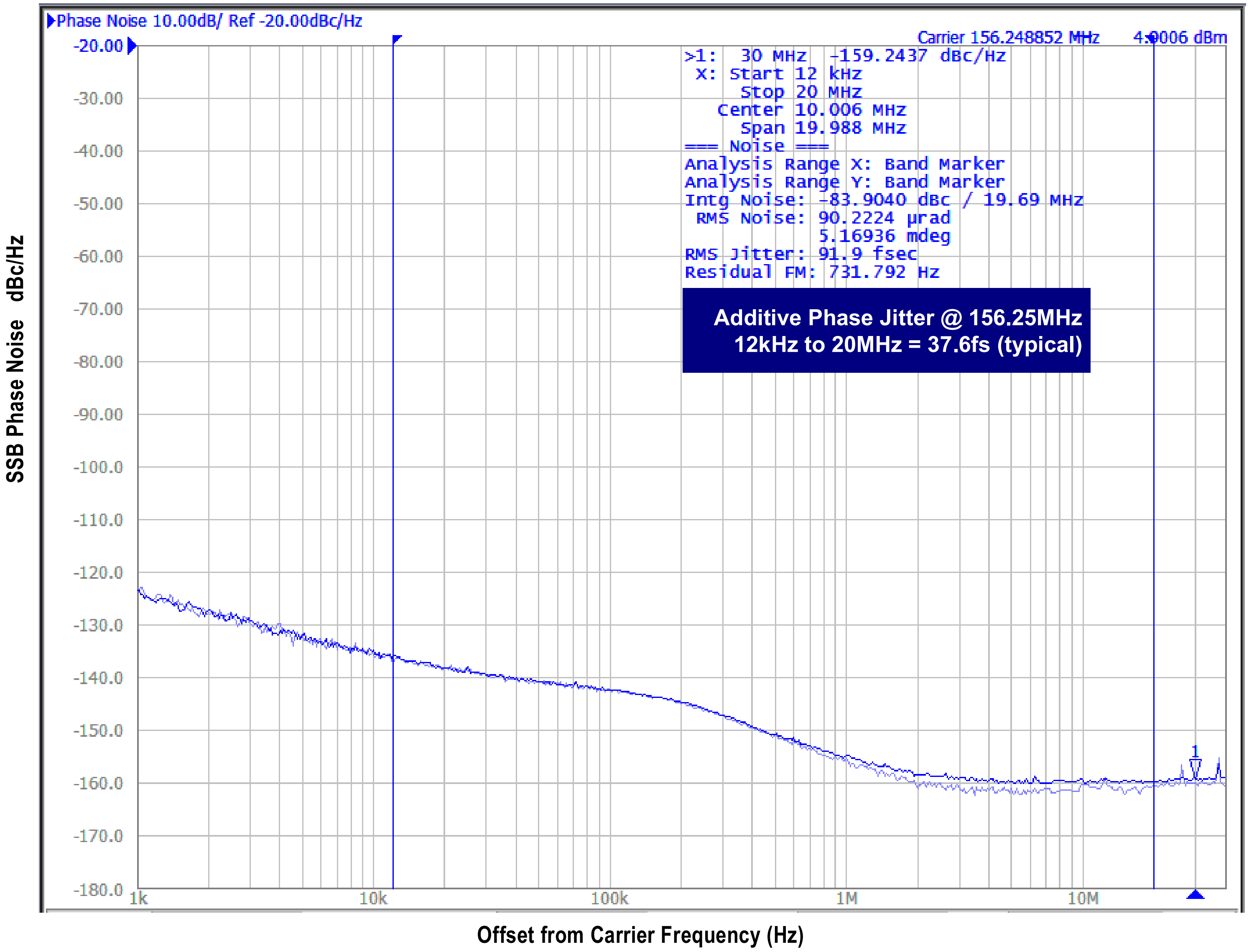
[n] Measured from -150mV to +150mV on the differential waveform (Qx minus nQx). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

[o] Measured at 100MHz.

[p] Measured for the following frequencies: 25MHz, 100MHz, 125MHz, 156.25MHz, 312.5MHz, 400MHz, 644.5313MHz, and 750MHz.

Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



```
>1:  30 MHz  -159.2437 dBc/Hz
 X: Start 12 kHz
     Stop 20 MHz
   Center 10.006 MHz
     Span 19.988 MHz
=== Noise ===
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -83.9040 dBc / 19.69 MHz
 RMS Noise: 90.2224 µrad
            5.16936 mdeg
RMS Jitter: 91.9 fsec
Residual FM: 731.792 Hz
```

Additive Phase Jitter @ 156.25MHz
12kHz to 20MHz = 37.6fs (typical)

As with most timing specifications, phase noise measurements have issues relating to the limitations of the measurement equipment. The noise floor of the equipment can be higher or lower than the noise floor of the device. Additive phase noise is dependent on both the noise floor of the input source and measurement equipment.

The additive phase jitter for this device was measured using an Renesas Clock Driver 8T49NS010A as an input source and Agilent E5052 phase noise analyzer.

Applications Information

Recommendations for Unused Input and Output Pins

Inputs

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, 1kΩ resistors can be tied from CLK to ground and nCLK to V_{DD}.

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

LVCMOS Control Pins

All control pins have internal pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs

LVCMOS Output (REFOUT)

If LVCMOS output is not used, then disable the output and it can be left floating.

LVPECL and HCSL Outputs

Any unused output pairs can be left floating. We recommend that there is no trace attached.

LVDS Outputs

Any unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

Differential Outputs

If all the outputs of any bank are not used, then disable all outputs to High-Impedance.

Crystal Input Interface

The 8T39210 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 1* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error. In addition, the recommended 12pF parallel resonant crystal tuning is shown in *Figure 2*.The optimum C1 and C2 values can be slightly adjusted for different board layouts.

Figure 1. Crystal Input Interface

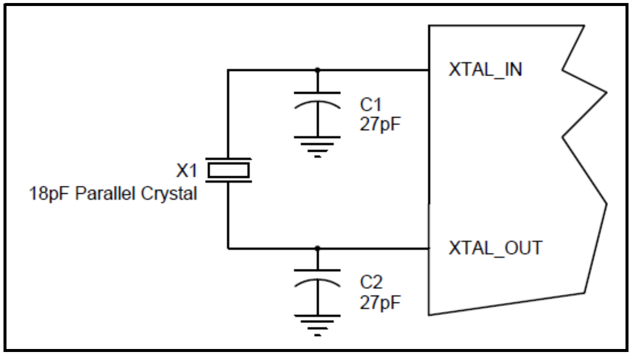
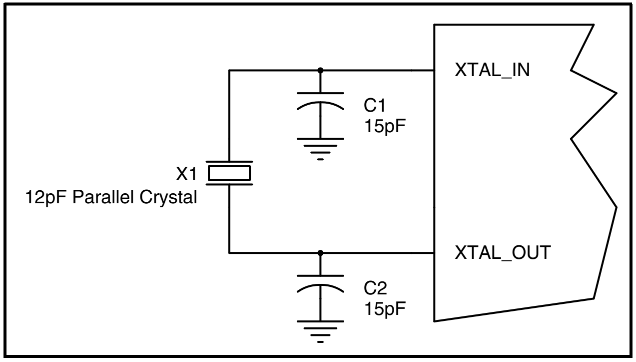


Figure 2. Crystal Input Interface



Power-up Ramp Sequence

This device has multiple supply pins dedicated for different blocks. Output power supplies V_{DDOx} (V_{DDOA}, V_{DDOB}, V_{DDOREF}) must ramp up before, or concurrently with core power supply V_{DD}. All power supplies must ramp up in a linear fashion and monotonically.

Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/ns. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. Figure 3 shows an example of the interface diagram for a high speed 3.3V LVCMOS driver.

This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. Figure 4 shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface

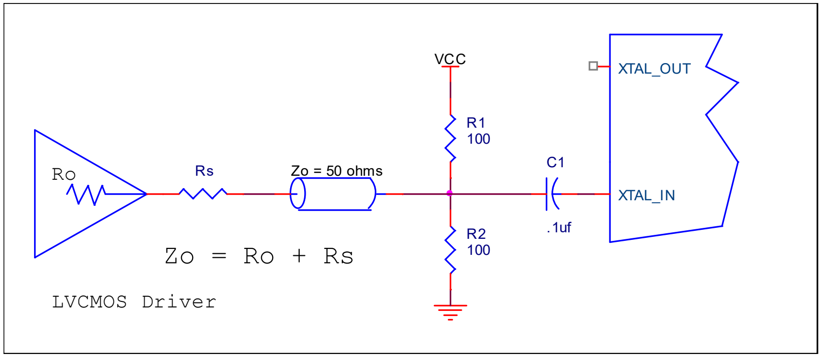
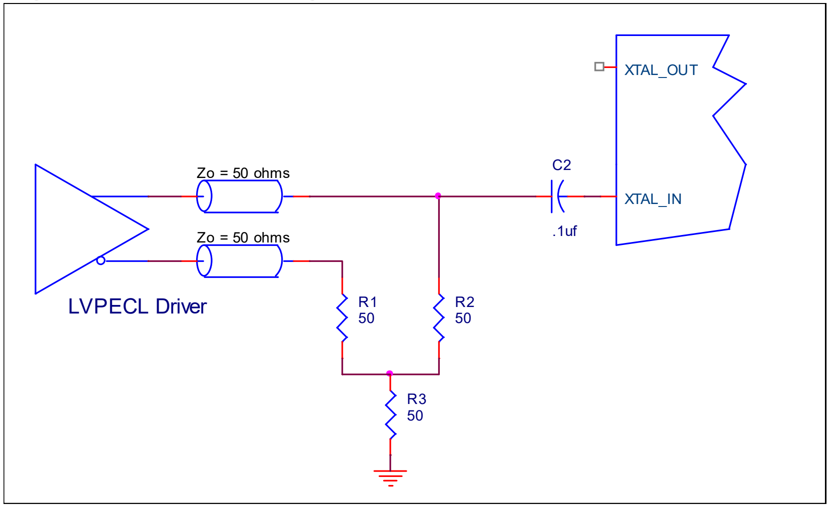


Figure 4. General Diagram for LVPECL Driver to XTAL Input Interface

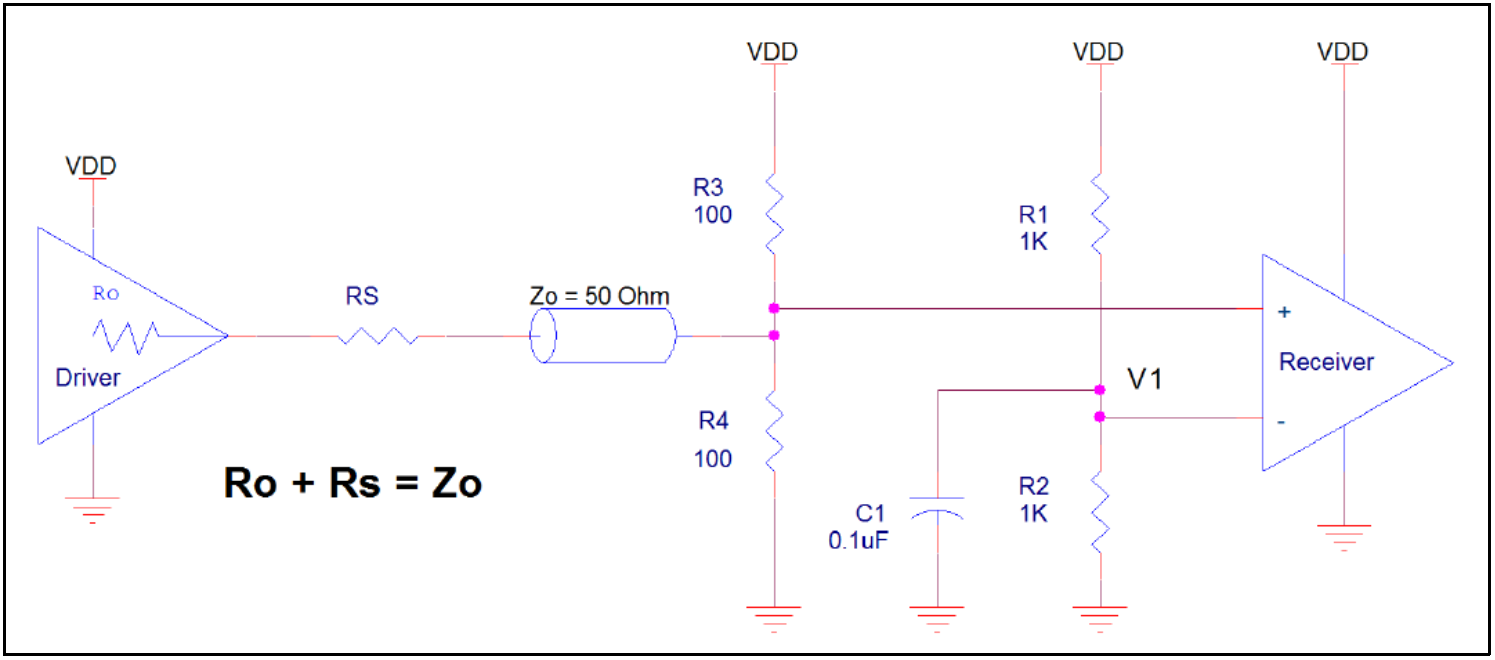


Wiring the Differential Input to Accept Single-Ended Levels

Figure 5 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{DD} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver.

When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Suggest edge rate faster than 1V/ns. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

Figure 5. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels



3.3V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, HCSL and other differential signals. Both differential signals must meet the V_{PP} and V_{CMR} input requirements. *Figure 6 to* Figure 9 show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements.

Figure 6. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

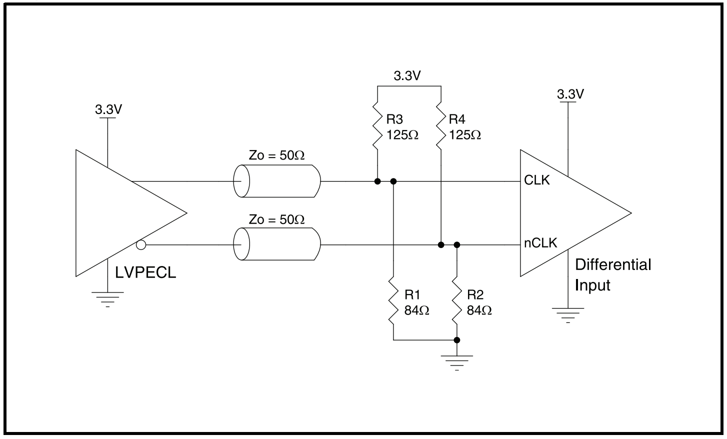


Figure 7. CLK/nCLK Input Driven by a 3.3V HCSL Driver

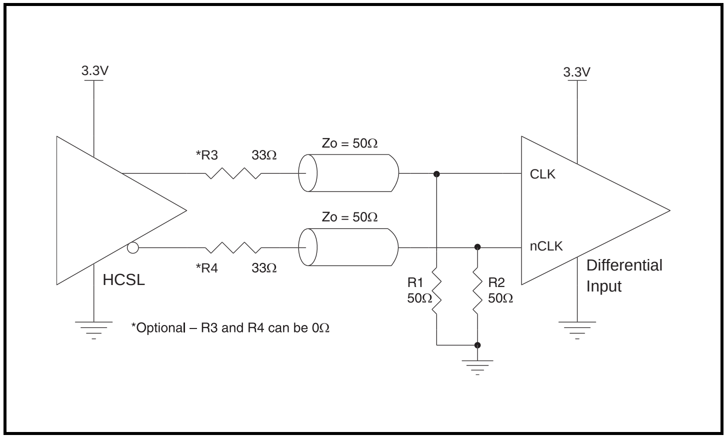


Figure 8. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

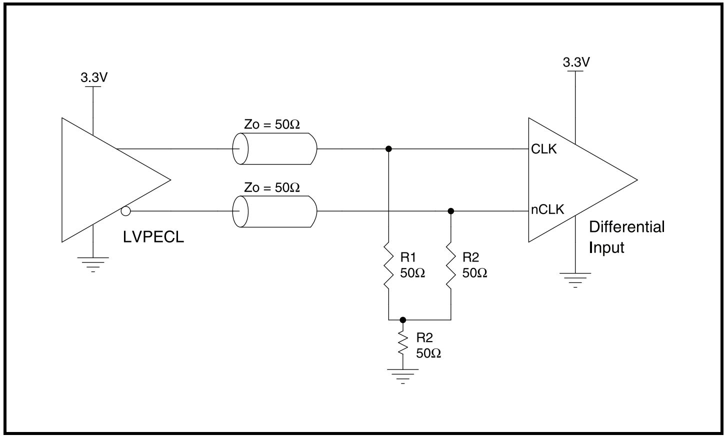
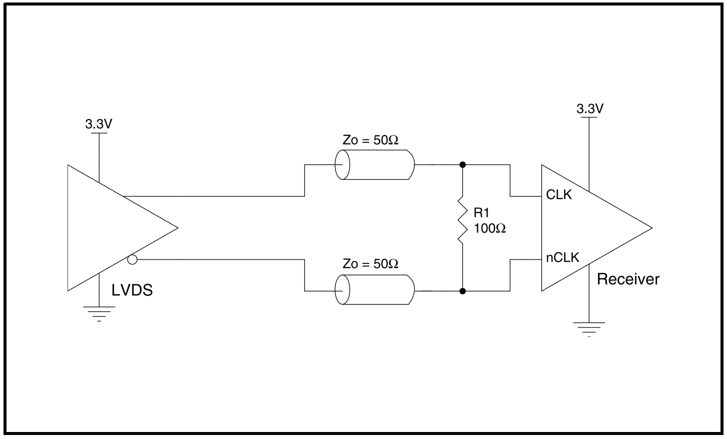


Figure 9. CLK/nCLK Input Driven by a 3.3V LVDS Driver



2.5V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, HCSL and other differential signals. Both differential signals must meet the V_{PP} and V_{CMR} input requirements. Figure 10 *to* Figure 13 show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements.

Figure 10. CLK/nCLK Input Driven by a 2.5V LVPECL Driver

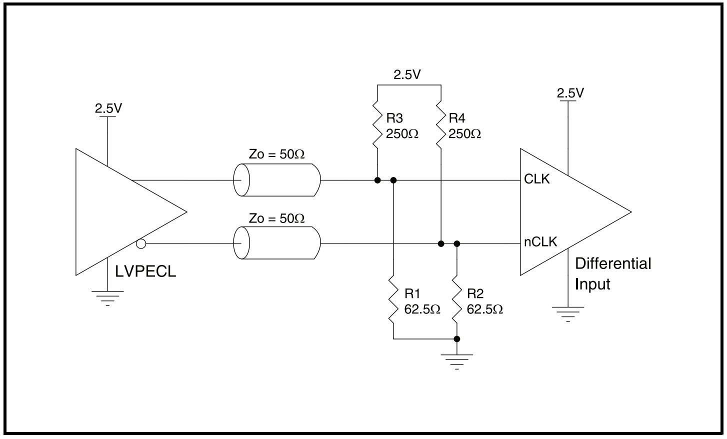


Figure 11. CLK/nCLK Input Driven by a 2.5V LVDS Driver

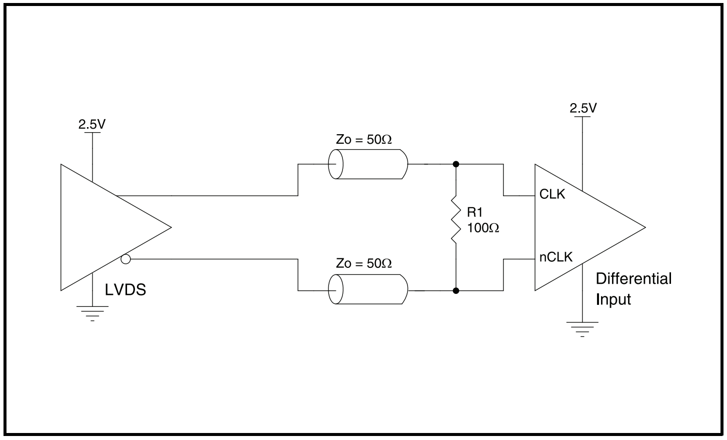


Figure 12. CLK/nCLK Input Driven by a 2.5V LVPECL Driver

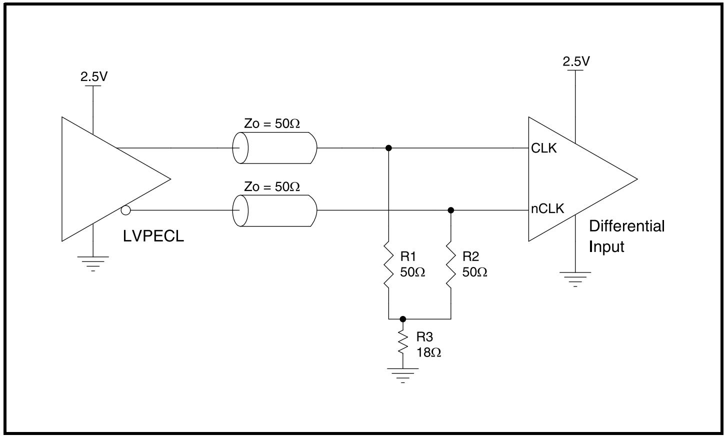
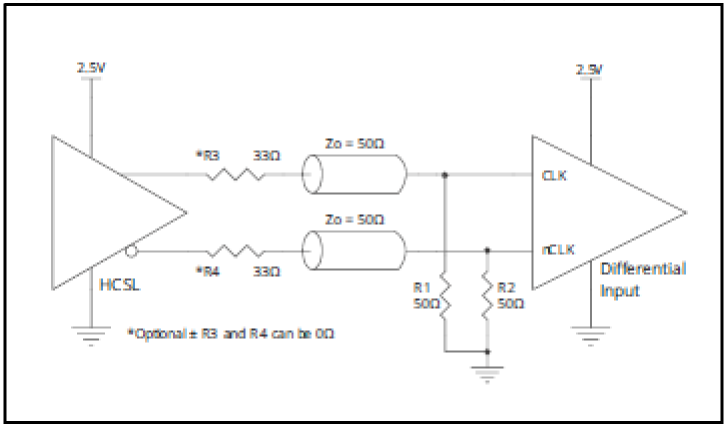


Figure 13. CLK/nCLK Input Driven by a 2.5V HCSL Driver



LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. Renesas offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in Figure 15 can be used with either type of output structure. Figure 15, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact Renesas and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

Figure 14. Standard LVDS Termination

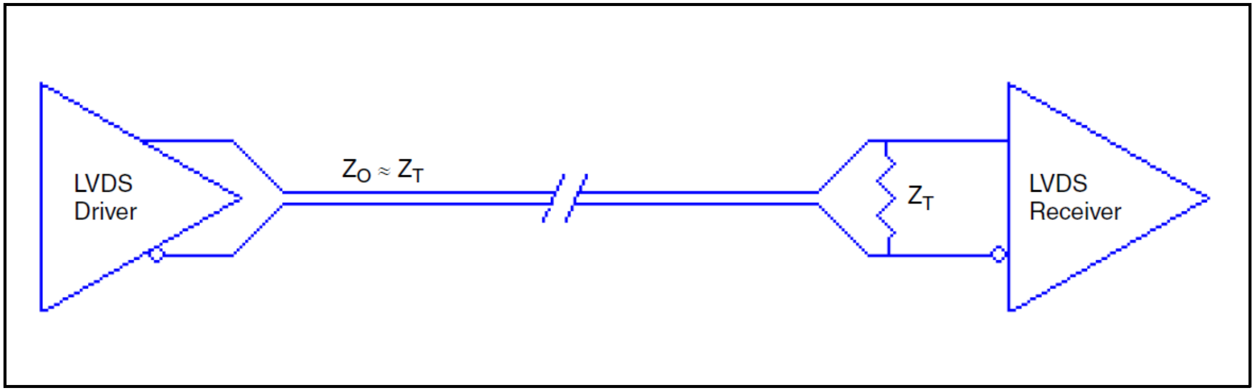
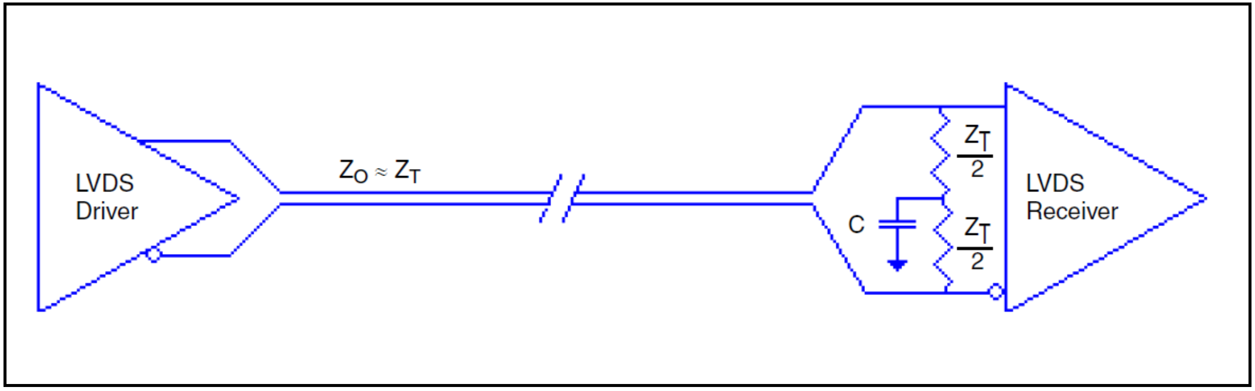


Figure 15. Optional LVDS Termination



Termination for 3.3V LVPECL Outputs

The clock topology shown below is a typical termination for LVPECL outputs. The two different terminations mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion.

Figure 16. 3.3V LVPECL Output Termination

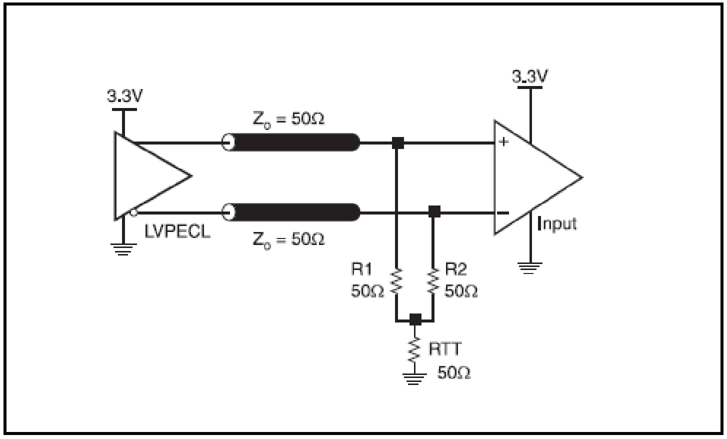
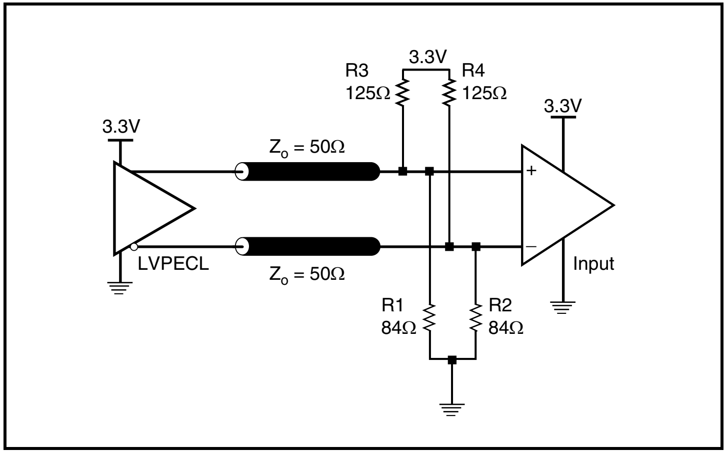


Figure 17. 3.3V LVPECL Output Termination



Termination for 2.5V LVPECL Outputs

Figure 18 and Figure 19 show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{DDO} – 2V. For V_{DDO} = 2.5V, the V_{DDO} – 2V is very close to ground level. The R3 in Figure 19 can be eliminated and the termination is shown in Figure 20.

Figure 18. 2.5V LVPECL Driver Termination Example

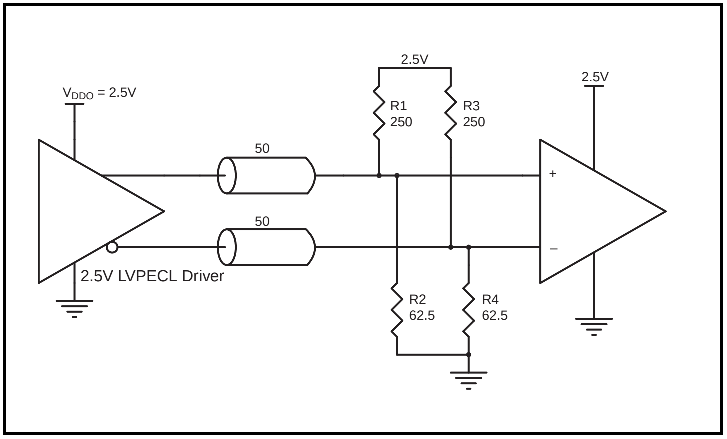


Figure 19. 2.5V LVPECL Driver Termination Example

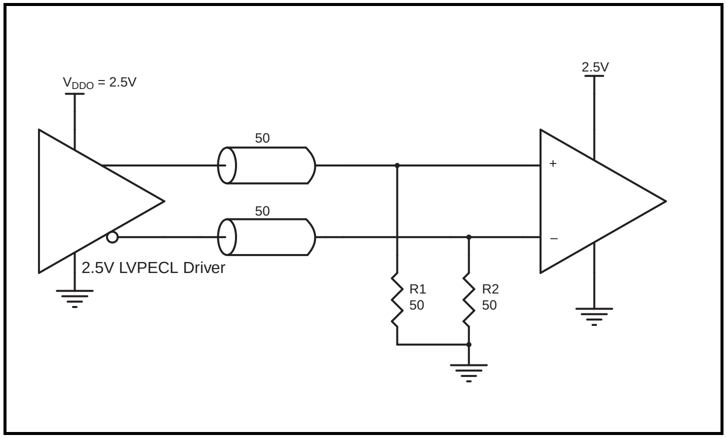
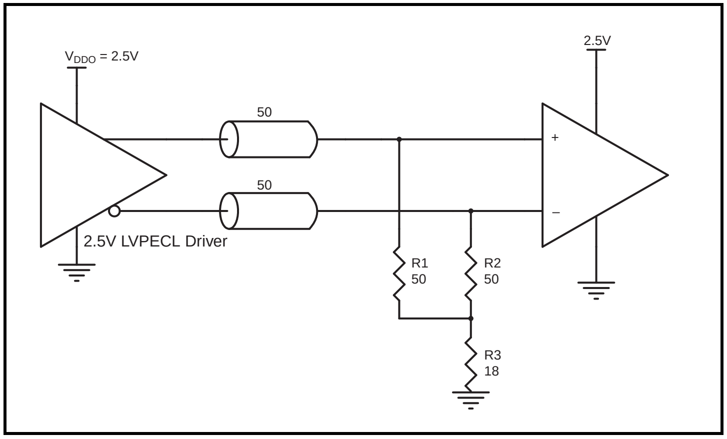


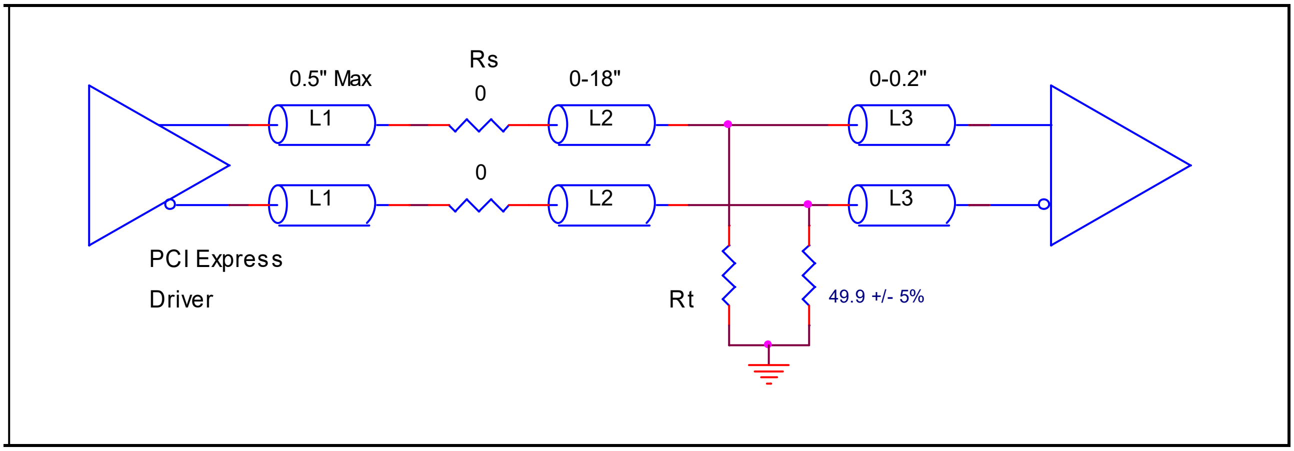
Figure 20. 2.5V LVPECL Driver Termination Example



Recommended Termination

Figure 21 is the recommended termination for applications where a point-to-point connection can be used. A point-to-point connection contains both the driver and the receiver on the same PCB. With a matched termination at the receiver, transmission-line reflections will be minimized. In addition, a series resistor (Rs) at the driver offers flexibility and can help dampen unwanted reflections. All traces should be 50Ω impedance single-ended or 100Ω differential.

Figure 21. Recommended Termination (where a point-to-point connection can be used)

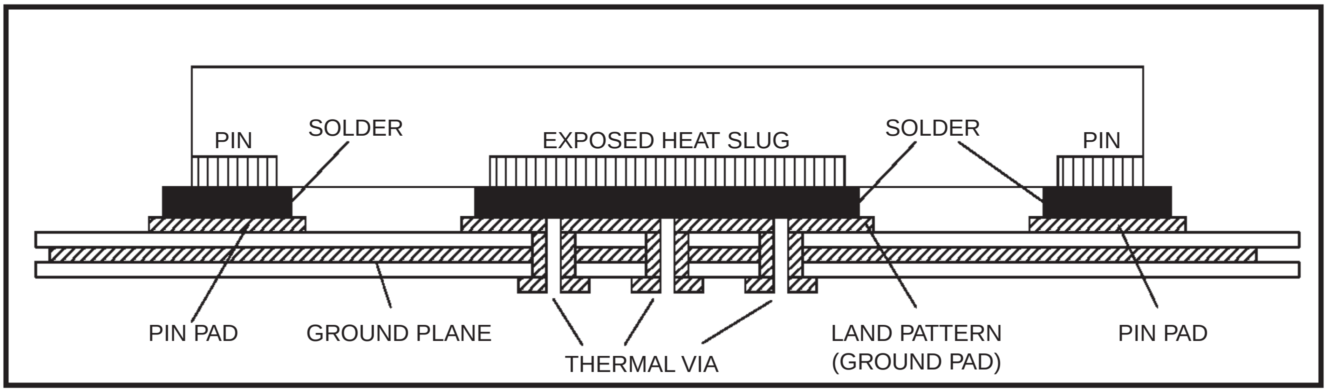


VFQFPN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 22.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Lead frame Base Package, Amkor Technology.

Figure 22. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)



LVPECL Power Considerations

This section provides information on power dissipation and junction temperature for the 8T39210.
Equations and example calculations are also provided.

LVPECL Power Considerations

1. Power Dissipation.

The total power dissipation for the 8T39210 is the sum of the core power plus the power dissipated due to outputs switching.
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

The Maximum current at 85°C is as follows:

I_{EE_MAX} = 204.614mA

- Power $(core)_{MAX} = I_{EE\_MAX} * V_{DD\_MAX}$ = 3.465V * 204.61mA = **708.99mW**
- Power $(outputs)_{MAX}$ = **32mW/Loaded Output pair**

If all outputs are loaded, the total output power is 10 * 32mW = **320mW**

Max LVPECL Power Dissipation = 708.99mW + 320mW = **1029mW**

LVCMOS Output Power Dissipation

- Static Power Dissipation:
  Power (static)_max = $V_{DDOREF\_max} * I_{DDOREF\_max}$ = 3.465V * 2mA **= 6.93mW**
  (I_{DDOREF_max} = 2mA)
- Dynamic Power Dissipation at 250MHz:
  Power (Dynamic)_max = $C_{PD} * f_{MAX} * N * V_{DDOREF}^2$ = 5.0pF * 250MHz * 1 * 3.465^2 = **15.01mW**
- LVCMOS Power Dissipation = 6.93mW + 15.01mW = **21.938mW**

Total Power Dissipation = 1029mW + 21.938mW = **1051mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 25.58°C/W per the following table. Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 1.051W * 25.58°C/W = 111.88°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 25. Thermal Resistance θ_{JA} for 48-Lead VFQFN

Symbol	Parameter		Value	Unit
θ_{JA}	Theta J_A, Junction to Ambient Air Thermal Coefficient	0m/s air flow	25.58	°C/W
		1m/s air flow	21.78	
		2m/s air flow	20.35	
θ_{JB}	Theta J_B, Junction to Board Thermal Coefficient		2.82	°C/W

LVPECL Power Considerations (Application Frequency 156.25MHz)

This section provides information on power dissipation and junction temperature for the 8T39210. Equations and example calculations are also provided.

LVPECL Power Considerations

1. Power Dissipation.

The total power dissipation for the 8T39210 is the sum of the core power plus the power dissipated due to outputs switching.
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

The Maximum current at 85°C is as follows:

I_{EE_MAX} = 98.961mA

- Power $(core)_{MAX}$ = I_{EE_MAX} * V_{DD_MAX} = 3.465V * 98.961mA = **342.9mW**
- Power $(outputs)_{MAX}$ = **32mW/Loaded Output pair**

If all outputs are loaded, the total output power is 10 * 32mW = **320mW**

Max LVPECL Power Dissipation = 342.9mW + 320mW = **662.9mW**

LVCMOS Output Power Dissipation

- Static Power Dissipation:
  Power (static)_max = V_{DDOREF_max} * I_{DDOREF_max} = 3.465V * 2mA **= 6.93mW**
  (I_{DDOREF_max} = 2mA)
- Dynamic Power Dissipation at 250MHz:
  Power (Dynamic)_max = C_{PD} * f_{MAX} * N * V_{DDOREF}^2 = 5.0pF * 156.25MHz * 1 * 3.465^2 = **9.38mW**
- LVCMOS Power Dissipation = 6.93mW + 9.38mW = **16.31mW**

Total Power Dissipation = 662.9mW + 16.31mW = **679.21mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 25.58°C/W per the following table. Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.679W * 25.58°C/W = 102.37°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 26. Thermal Resistance θ_{JA} for 48-Lead VFQFN

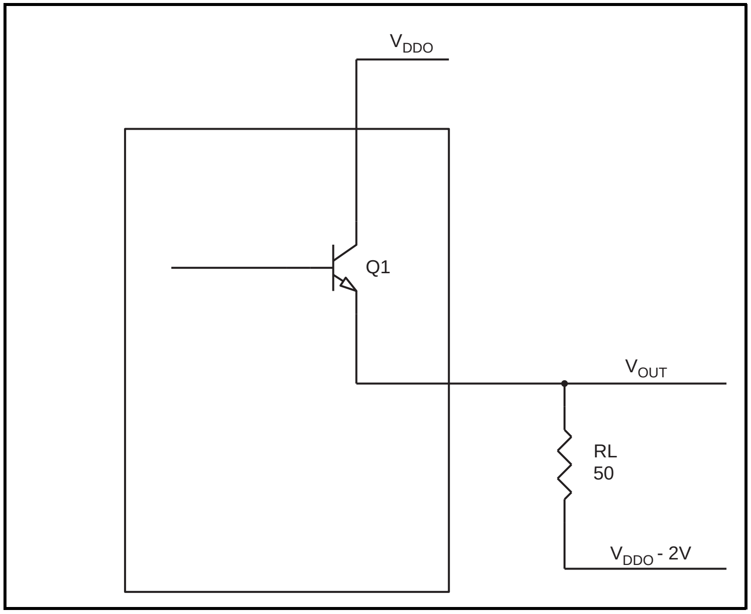
Symbol	Parameter		Value	Unit
θ_{JA}	Theta J_A, Junction to Ambient Air Thermal Coefficient	0m/s air flow	25.58	°C/W
		1m/s air flow	21.78	
		2m/s air flow	20.35	
θ_{JB}	Theta J_B, Junction to Board Thermal Coefficient		2.82	°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

LVPECL output driver circuit and termination are shown in Figure 23.

Figure 23. LVPECL Driver Circuit and Termination



To calculate power dissipation per output pair due to loading, use the following equations which assume a 50Ω load, and a termination voltage of V_{DDO} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{DDO\_MAX}} - \mathbf{0.8V}$
  $(V_{DDO\_MAX} - V_{OH\_MAX})$ = **0.8V**
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{DDO\_MAX}} - \mathbf{1.6V}$
  $(V_{DDO\_MAX} - V_{OL\_MAX})$ = **1.6V**

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

Pd_H = $[(V_{OH\_MAX} - (V_{DDO\_MAX} - 2V))/R_L] * (V_{DDO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{DDO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{DDO\_MAX} - V_{OH\_MAX}) =$ [(2V – 0.8V)/50Ω] * 0.8V = **19.20mW**

Pd_L = $[(V_{OL\_MAX} - (V_{DDO\_MAX} - 2V))/R_L] * (V_{DDO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{DDO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{DDO\_MAX} - V_{OL\_MAX}) =$ [(2V – 1.6V)/50Ω] * 1.6V = **12.80mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = 32mW

LVDS Power Considerations

This section provides information on power dissipation and junction temperature for the 8T39210. Equations and example calculations are also provided.

LVDS Power Considerations

1. Power Dissipation.

The total power dissipation for the 8T39210 is the sum of the core power plus the power dissipated due to outputs switching.
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

The Maximum current at 85°C is as follows:

I_{DD_MAX} = 37mA

I_{DDO_MAX} = 189mA

Max LVDS Power Dissipation = $V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDO\_MAX})$ = 3.465V * (37mA + 189mA) = **782.55mW**

LVCMOS Output Power Dissipation

- Static Power Dissipation:
  Power (static)_max = $V_{DDOREF\_max} * I_{DDOREF\_max}$ = 3.465V * 2mA **= 6.93mW**
  (I_{DDOREF_max} = 2mA)
- Dynamic Power Dissipation at 250MHz:
  Power (Dynamic)_max = $C_{PD} * f_{MAX} * N * V_{DDOREF}^2$ = 5.0pF * 250MHz * 1 * 3.465^2 = **15.01mW**
- LVCMOS Power Dissipation = 6.93mW + 15.01mW = **21.938mW**

Total Power Dissipation = 782.55mW + 21.938mW = **804.49mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 25.58°C/W per Table 25. Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.805W * 25.58°C/W = 105.58°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

LVDS Power Considerations (Application Frequency 156.25MHz)

This section provides information on power dissipation and junction temperature for the 8T39210. Equations and example calculations are also provided.

LVDS Power Considerations

1. Power Dissipation.

The total power dissipation for the 8T39210 is the sum of the core power plus the power dissipated due to outputs switching.
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

The Maximum current at 85°C is as follows:

I_{DD_MAX} = 36mA

I_{DDO_MAX} = 105mA

Max LVDS Power Dissipation = V_{DD_MAX} * (I_{DD_MAX} + I_{DDO_MAX}) = 3.465V * (36mA + 105mA) = **487.67mW**

LVCMOS Output Power Dissipation

- Static Power Dissipation:
  Power (static)_max = V_{DDOREF_max} * I_{DDOREF_max} = 3.465V * 2mA **= 6.93mW**
  (I_{DDOREF_max} = 2mA)
- Dynamic Power Dissipation at 156.25MHz:
  Power (Dynamic)_max = C_{PD} * f_{MAX} * N * V_{DDOREF}^2 = 5.0pF * 156.25MHz * 1 * 3.465^2 = **9.38mW**
- LVCMOS Power Dissipation = 6.93mW + 9.38mW = **16.31mW**

Total Power Dissipation = 487.67mW + 16.31mW = **503.98mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 25.58°C/W per Table 25. Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.504W * 25.58°C/W = 97.9°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

HCSL Power Considerations

This section provides information on power dissipation and junction temperature for the 8T39210. Equations and example calculations are also provided.

HCSL Power Considerations

1. Power Dissipation.

The total power dissipation for the 8T39210 is the sum of the core power plus the power dissipated due to outputs switching.
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

The Maximum current at 85°C is as follows:

I_{DD_MAX} = 38mA

I_{DDO_MAX} = 118mA (application frequency = 750MHz)

- Power (core)$_{MAX}$ = V_{DD_MAX} * (I_{DD_MAX} + I_{DDO_MAX}) = 3.465V * (38mA + 118mA) = **541.92mW**
- Power (outputs)$_{MAX}$ = **44.5mW/Loaded Output pair**

If all outputs are loaded, the total power is 10 * 44.5mW = **445mW**

Max HCSL Power Dissipation = 541.92mW + 445mW = **986.92mW**

LVCMOS Output Power Dissipation

- Static Power Dissipation:
  Power (static)_max = V_{DDOREF_max} * I_{DDOREF_max} = 3.465V * 2mA **= 6.93mW**
  (I_{DDOREF_max} = 2mA)
- Dynamic Power Dissipation at 250MHz:
  Power (Dynamic)_max = C_{PD} * f_{MAX} * N * V_{DDOREF}^2 = 5.0pF * 250MHz * 1 * 3.465^2 = **15.01mW**
- LVCMOS Power Dissipation = 6.93mW + 15.01mW = **21.938mW**

Total Power Dissipation = 986.92mW + 21.94mW = **1008.85mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 25.58°C/W per Table 25. Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 1.009W * 25.58°C/W = 110.81°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

HCSL Power Considerations (Application Frequency 156.25MHz)

This section provides information on power dissipation and junction temperature for the 8T39210. Equations and example calculations are also provided.

HCSL Power Considerations

1. Power Dissipation.

The total power dissipation for the 8T39210 is the sum of the core power plus the power dissipated due to outputs switching.
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

The Maximum current at 85°C is as follows:

I_{DD_MAX} = 38mA

I_{DDO_MAX} = 48mA (Application Frequency = 156.25MHz)

- Power (core)$_{MAX}$ = V_{DD_MAX} * (I_{DD_MAX} + I_{DDO_MAX}) = 3.465V * (38mA + 48mA) = **300.34mW**
- Power (outputs)$_{MAX}$ = **44.5mW/Loaded Output pair**

If all outputs are loaded, the total power is 10 * 44.5mW = **445mW**

Max HCSL Power Dissipation = 300.34mW + 445mW = **745.34mW**

LVCMOS Output Power Dissipation

- Static Power Dissipation:
  Power (static)_max = V_{DDOREF_max} * I_{DDOREF_max} = 3.465V * 2mA **= 6.93mW**
  (I_{DDOREF_max} = 2mA)
- Dynamic Power Dissipation at 156.25MHz:
  Power (Dynamic)_max = C_{PD} * f_{MAX} * N * V_{DDOREF}^2 = 5.0pF * 156.25MHz * 1 * 3.465^2 = **9.38mW**
- LVCMOS Power Dissipation = 6.93mW + 9.38mW = **16.31mW**

Total Power Dissipation = 745.34mW + 16.31mW = **761.65mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 25.58°C/W per Table 25. Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.761W * 25.58°C/W = 104.6°C. This is below the limit of 125°C.

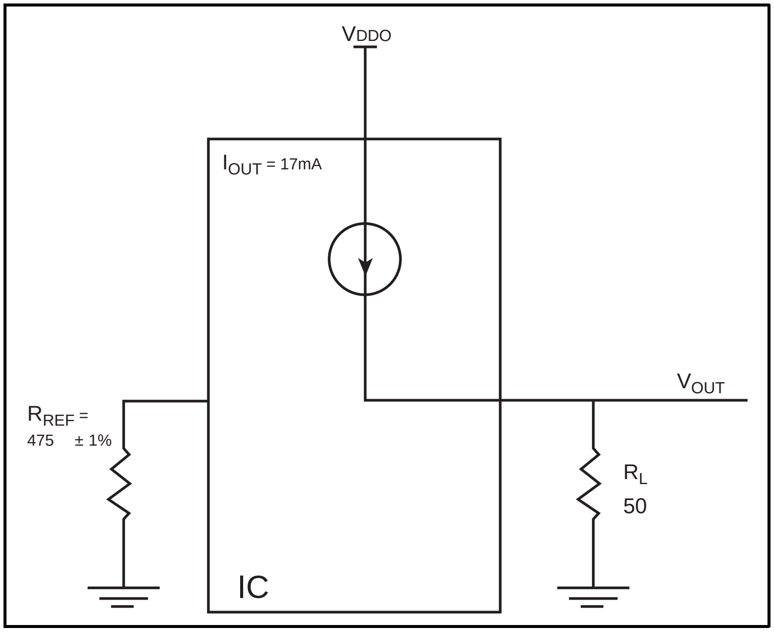
This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

3. Calculations and Equations.

The purpose of this section is to calculate power dissipation on the IC per HCSL output pair.

HCSL output driver circuit and termination are shown in Figure 24.

Figure 24. HCSL Driver Circuit and Termination



HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs when $V_{DDO–MAX}$.

Power= $(V_{DDO\_MAX} – V_{OUT}) * I_{OUT}$,
since $V_{OUT} – I_{OUT} * R_L$

= $(V_{DDO\_MA} – I_{OUT} * R_L) * I_{OUT}$

= (3.465V – 17mA * 50Ω) * 17mA

Total Power Dissipation per output pair = **44.5mW**

Reliability Information

See Table 25.

Transistor Count

The transistor count for 8T39210 is: 8654

Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

Ordering Information

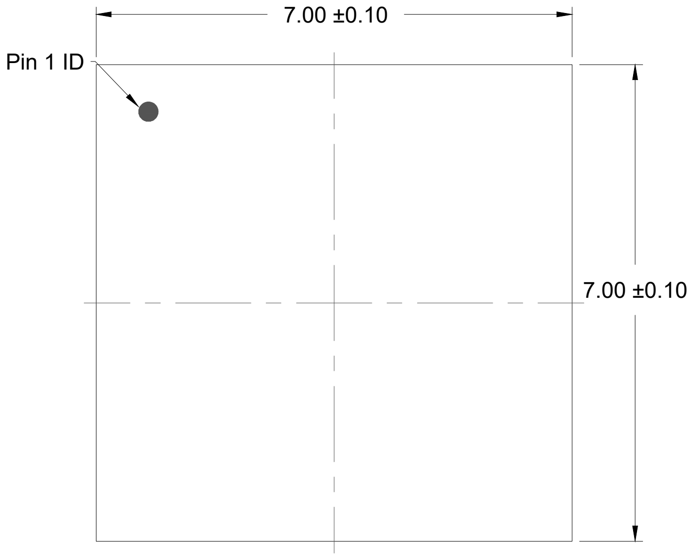
Part Number	Marking	Package Description	Carrier Type	Temperature Range
8T39210NLGI	IDT8T39210NLGI	48-VFQFPN, Lead-Free	Tray	-40°C to 85°C
8T39210NLGI8	IDT8T39210NLGI	48-VFQFPN, Lead-Free	Tape and Reel	-40°C to 85°C

Revision History

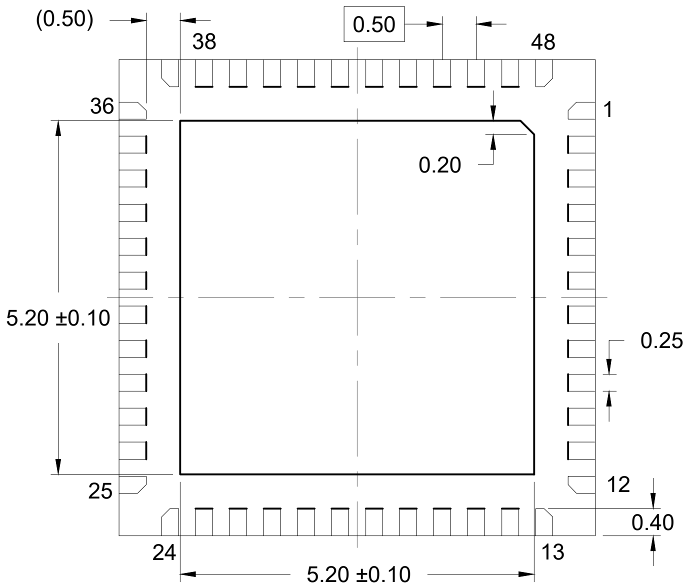
Revision Date	Description of Change
February 2, 2023	▪ Updated Recommended Termination section. ▪ Updated Rs value in Figure 21 to ‘0’ from ‘0 to 33’.
February 22, 2021	▪ Updated footnote [p] in Table 22, Table 23, and Table 24
February 19, 2021	▪ Increased maximum frequency for HCSL output
December 16, 2019	▪ Corrected a calculation mistake in LVDS Power Considerations (Application Frequency 156.25MHz) ▪ Dynamically linked the package outline drawings to the document; however, no technical changes.
December 6, 2019	Added package outline drawings.
November 22, 2019	Initial release.

Package Outline Drawing

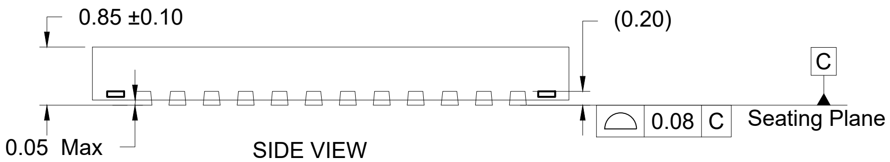
Package Code: NLG48P2
48-VFQFPN 7.0 x 7.0 x 0.85 mm Body, 0.5mm Pitch
PSC-4203-05, Revision: 02, Date Created: Apr 5, 2024



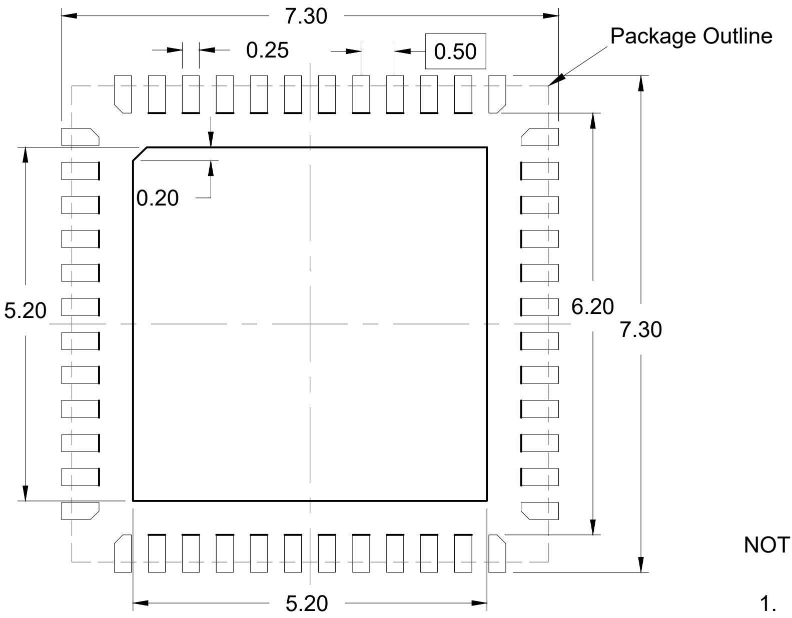
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

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