8V19N882

RF Sampling Clock Generator and Jitter Attenuator

The 8V19N882 is a fully integrated FemtoClock® RF Sampling Clock Generator and Jitter Attenuator. The device is designed as a high-performance clock solution for conditioning and frequency/phase management of wireless base station radio equipment boards. The 8V19N882 is optimized to deliver excellent phase noise performance as required in 4G, 5G, and including mmWave radio implementations. The device supports JESD204B (subclass 0 and 1) and JESD204C.

A two-stage PLL architecture supports both jitter attenuation and frequency multiplication. The first stage PLL is the jitter attenuator and uses an external VCXO for best possible phase noise characteristics. The second stage PLL locks on the first PLL output signal and synthesizes the target frequency. The second stage PLL can use the internal or an external high-frequency VCO.

The 8V19N882 generates the high-frequency clocks and the low-frequency synchronization signals (SYSREF) from the selected VCO. SYSREF signals are internally synchronized to the clock signals. The integrated signal delay blocks can be used to achieve phase alignment, controlled phase offsets between system reference and clock signals, and to align/delay individual output signals. The two redundant inputs are monitored for activity. Four selectable clock switching modes can handle clock input failure scenarios. Auto-lock, individually programmable output frequency dividers, and phase adjustment capabilities are added for flexibility.

The 8V19N882 is configured through a 3/4-wire SPI interface and reports lock and signal loss status in internal registers and via the GPIO[1:0] outputs. Internal status bit changes can also be reported via a GPIO output.

Features

- High-performance clock RF sampling clock generator and clock jitter attenuator with support for JESD204B/C
- Low phase noise: -144.7dBc/Hz (800kHz offset; 491.52MHz)
- Integrated phase noise of 74fs RMS (12k-20MHz, 491.52MHz)
- Dual-PLL architecture with internal and optional external VCO
- Eight output channels with a total of 16 outputs
- Configurable integer clock frequency dividers
- Clock output frequencies: up to 3932.16MHz (Internal VCO) and ≤ 6GHz (optional external VCO)
- Differential, low noise I/O
- Deterministic phase delay and integrated phase delay circuits
- Redundant input clock architecture with two inputs and monitors, holdover, and input switching
- SPI 3/4 wire configuration interface
- Supply voltage: 1.8V, 2.5V, and 3.3V
- Package: 76 VFQFN (9 x 9 mm²)
- Temperature range: -40°C to +105°C (board)

Applicable Standards

- JESD204B and C

Applications

- Wireless infrastructure applications: 4G, 5G, and mmWave
- Data acquisition: jitter-sensitive ADC and DAC circuits
- Radar, imaging, instrumentation, and medical

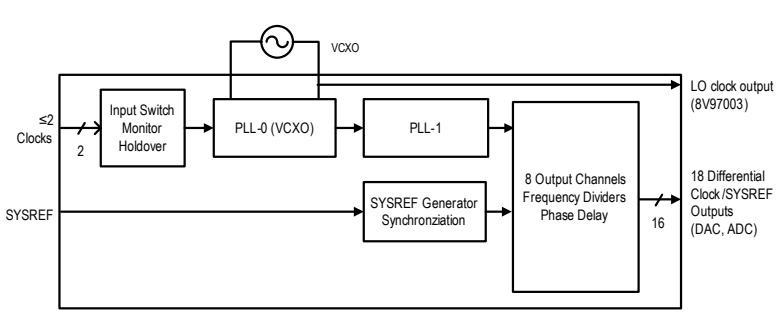

Figure 1. Simplified Block Diagram

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1. Block Diagram

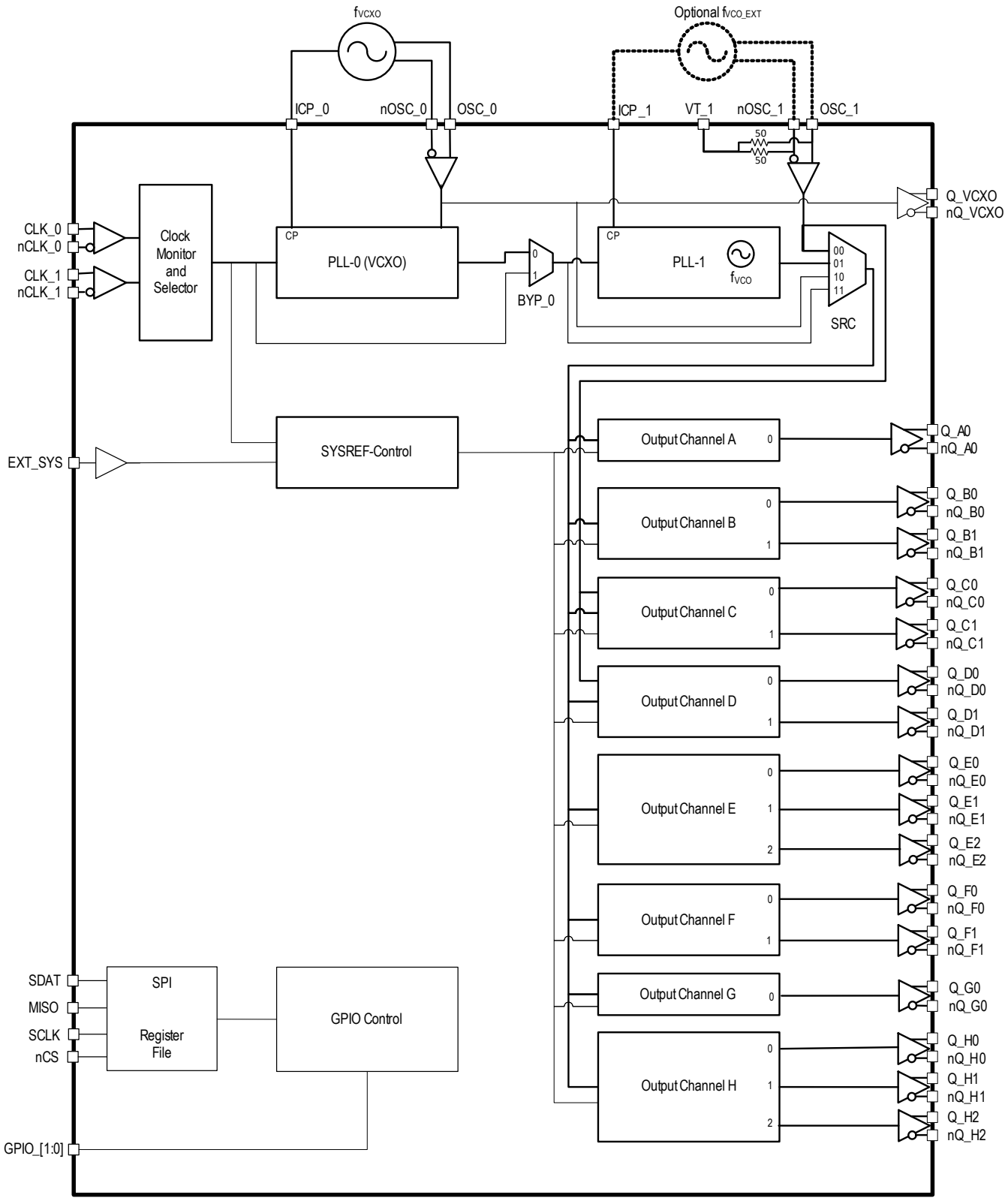


Figure 2. Block Diagram (f_{VCO} = 3932.16MHz)

2. Features (Full List)

- High-performance clock RF-PLL with support for JESD204B/C
- Low phase noise: -144.7dBc/Hz (800kHz offset; 491.52MHz)
- Integrated phase noise of 74fs RMS (12k-20MHz, 491.52MHz)
- Dual-PLL architecture with optional external VCO
- 1st-PLL stage with external VCXO for clock jitter attenuation
- 2nd-PLL with internal FemtoClockNG PLL: 3932.16MHz
  - Optional external VCO frequency range: 700MHz to 6GHz
- Eight output channels with a total of 16 outputs, organized in:
  - Two RF clock channels each consisting of two device clocks (≤ 4GHz)/SYSREF outputs; each output can buffer external VCO clocks up to 6GHz
  - Six device clock/SYSREF channels (2 or 3 outputs, ≤ 4GHz)
  - One VCXO-PLL (PLL-0) output
- Configurable integer clock frequency dividers
- Supported clock output frequencies include:
  - From internal VCO: 3932.16, 1966.08, 983.04, 491.52 and 245.76MHz
  - From external VCO: ≤ 6GHz
- Low-power LVPECL/LVDS outputs support configurable signal amplitude, DC and AC coupling and LVPECL, LVDS line terminations techniques
- Phase delay circuits
  - PLL feedback phase delay for output-to-input alignment
  - Channel phase delay with 512 steps of 127ps
  - Individual SYSREF output phase delay with steps of 254ps and 30ps analog delay for output alignment
- Redundant input clock architecture with two inputs and the following:
  - Input activity monitoring
  - Manual and automatic, fault-triggered clock selection modes
  - Priority controlled clock selection
  - Digital holdover and smooth input clock switching
  - Differential inputs accept LVDS and LVPECL signals
- SYSREF generation modes include internal and external trigger mode for JESD204B/C
- SPI 3/4 wire configuration interface
- Supply voltage: 1.8V (core, outputs) and 3.3V (oscillator interfaces, 6GHz output supply)
- Supply voltage: 1.8V (core), 3.3V (oscillator interfaces, 6GHz output supply), 1.8V, 2.5V, and 3.3V (output supplies)
- SPI and control I/O voltage: 1.8V
- Package: 76 VFQFN (9 x 9 mm²)
- Temperature range: -40°C to +105°C (board)

3. Pin Information

3.1 Pin Assignments

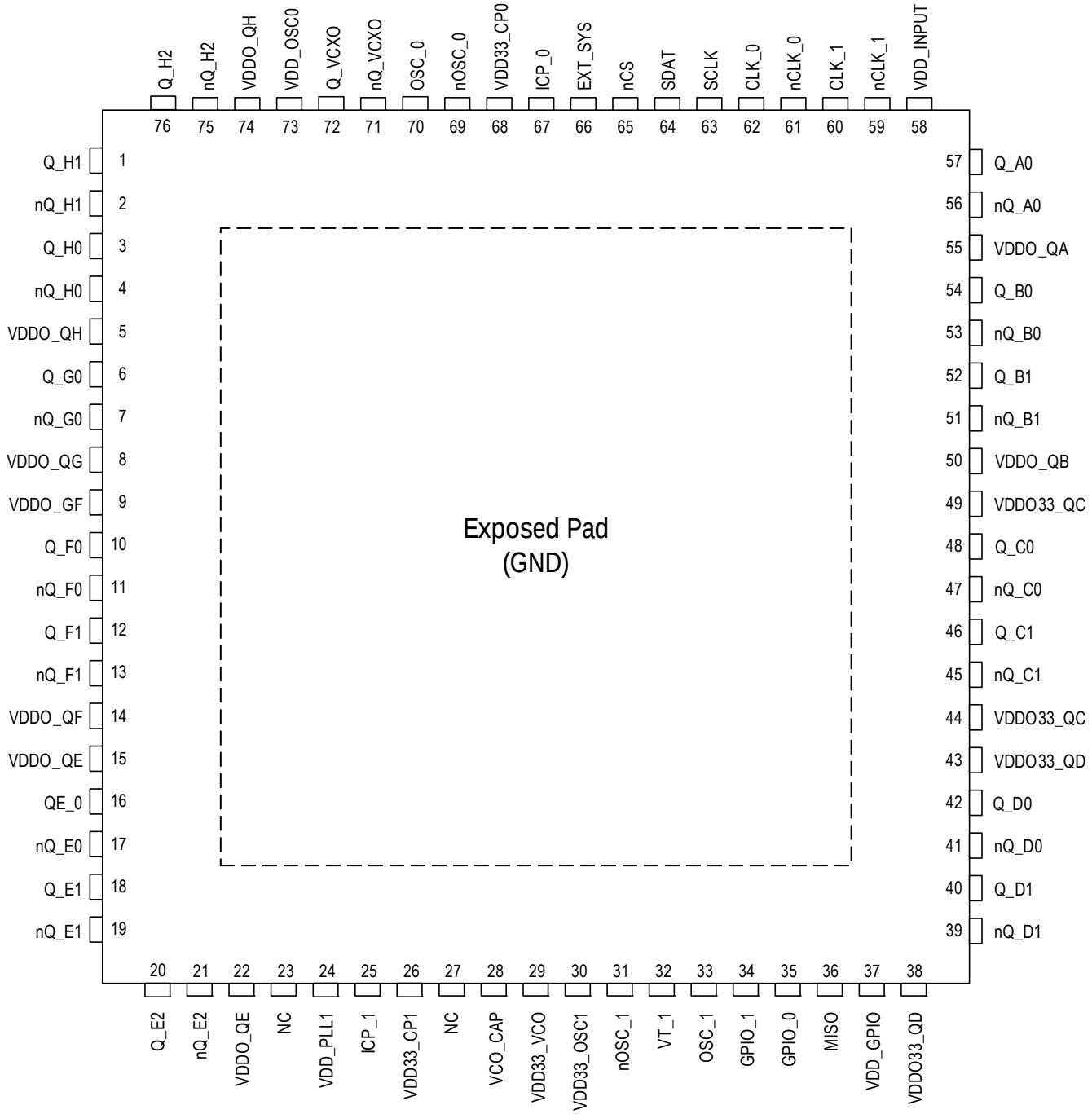


Figure 3. Pin Assignments for 9 x 9 mm² 76 VFQFN Package (Top View)

3.2 Pin Descriptions

Table 1. Pin Descriptions

Pin	Name	Type[1]		Description
Clock and SYSREF Signal Inputs				
62	CLK_0	Input	PD	Device clock 0 non-inverting and inverting differential clock input. Inverting input is biased to ~1.05V by default when left floating. Compatible with LVPECL, LVDS, and LVCMOS signals.
61	nCLK_0		PD/PU	
60	CLK_1	Input	PD	Device clock 1 non-inverting and inverting differential clock input. Inverting input is biased to ~1.05V by default when left floating. Compatible with LVPECL, LVDS and LVCMOS signals.
59	nCLK_1		PD/PU	
66	EXT_SYS	Input	PD	External SYSREF pulse trigger input. 1.8V LVCMOS interface levels.
External Oscillator Interface Pins				
67	ICP_0	Output		PLL-0 (VCXO-PLL) charge pump output. Connect to the frequency control input of the external VCXO and to the loop filter.
70	OSC_0	Input	PD	VCXO non-inverting and inverting differential clock input. Inverting input is biased to ~1.05V by default when left floating. Compatible with LVPECL, LVDS, and LVCMOS signals.
69	nOSC_0		PD/PU	
25	ICP_1	Output		PLL-1 charge pump output. Connect to the frequency control input of the external VCO and the loop filter. Leave open if PLL-1 is not used (bypassed).
33	OSC_1	Input	50Ω	External VCO non-inverting and inverting differential clock input. Compatible with LVPECL and LVDS signals, also accepts single-ended sinusoidal signals on the OSC_1 pin.
31	nOSC_1		50Ω	
32	VT_1	Termination 50Ω to OSC_1, nOSC_1		Input for termination. Both OSC_1 and nOSC_1 inputs are internally terminated 50Ω to this pin. For input termination information, see OSC_1 Input Termination (External VCO).
Clock and SYSREF Outputs				
57, 56	Q_A0, nQ_A0	Output		Differential clock/SYSREF output A0 (Channel A). Configurable LVPECL/LVDS style and amplitude.
54, 53	Q_B0, nQ_B0	Output		Differential clock/SYSREF output B0 (Channel B). Configurable LVPECL/LVDS style and amplitude.
52, 51	Q_B1, nQ_B1	Output		Differential clock/SYSREF output B1 (Channel B). Configurable LVPECL/LVDS style and amplitude.
48, 47	Q_C0, nQ_C0	Output		Differential clock/SYSREF output C0 (Channel C). LVPECL style and configurable amplitude.
46, 45	Q_C1, nQ_C1	Output		Differential clock/SYSREF output C1 (Channel C). LVPECL style and configurable amplitude.
42, 41	Q_D0, nQ_D0	Output		Differential clock/SYSREF output D0 (Channel D). LVPECL style and configurable amplitude.
40, 39	Q_D1, nQ_D1	Output		Differential clock/SYSREF output D1 (Channel D). LVPECL style and configurable amplitude.
16, 17	Q_E0, nQ_E0	Output		Differential clock/SYSREF output E0 (Channel E). Configurable LVPECL/LVDS style and amplitude.
18, 19	Q_E1, nQ_E1	Output		Differential clock/SYSREF output E1 (Channel E). Configurable LVPECL/LVDS style and amplitude.
20, 21	Q_E2, nQ_E2	Output		Differential clock/SYSREF output E2 (Channel E). Configurable LVPECL/LVDS style and amplitude.

Table 1. Pin Descriptions (Cont.)

Pin	Name	Type[1]		Description
10, 11	Q_F0, nQ_F0	Output		Differential clock/SYSREF output F0 (Channel F). Configurable LVPECL/LVDS style and amplitude.
12, 13	Q_F1, nQ_F1	Output		Differential clock/SYSREF output F1 (Channel F). Configurable LVPECL/LVDS style and amplitude.
6, 7	Q_G0, nQ_G0	Output		Differential clock/SYSREF output G0 (Channel G). Configurable LVPECL/LVDS style and amplitude.
3, 4	Q_H0, nQ_H0	Output		Differential clock/SYSREF output H0 (Channel H). Configurable LVPECL/LVDS style and amplitude.
1, 2	Q_H1, nQ_H1	Output		Differential clock/SYSREF output H1 (Channel H). Configurable LVPECL/LVDS style and amplitude.
76, 75	Q_H2, nQ_H2	Output		Differential clock/SYSREF output H2 (Channel H). Configurable LVPECL/LVDS style and amplitude.
72, 71	Q_VCXO, nQ_VCXO	Output		Differential PLL-0 (VCXO-PLL) clock outputs. Configurable LVPECL/LVDS style.
Control I/O				
35	GPIO_0	Input/ Output	PD	Configurable control input/status output pin 0. 1.8V LVCMOS interface levels.
34	GPIO_1	Input/ Output	PD	Configurable control input/status output pin 1. 1.8V LVCMOS interface levels.
64	SDAT	Input/ Output	PU	SPI serial configuration interface data pin. Input/Output in SPI 3-wire mode. Input in 4-wire SPI mode. 1.8V interface levels.
63	SCLK	Input	PD	SPI serial configuration interface clock pin. 1.8V interface levels.
65	nCS	Input	PU	SPI serial configuration interface chip-select pin. 1.8V interface levels.
36	MISO	Output		SPI serial configuration interface data output (in SPI 4-wire mode). Not used in SPI 3-wire mode. 1.8V interface levels.
Power Supply, Ground (GND), and Bypass				
55	VDDO_QA	Power		Positive supply voltage (1.8V, 2.5V, 3.3V) for the Q_A[1:0] outputs.
50	VDDO_QB	Power		Positive supply voltage (1.8V, 2.5V, 3.3V) for the Q_B[1:0] outputs.
44, 49	VDDO33_QC	Power		Positive supply voltage (3.3V) for the Q_C[1:0] outputs.
38, 43	VDDO33_QD	Power		Positive supply voltage (3.3V) for the Q_D[1:0] outputs.
15, 22	VDDO_QE	Power		Positive supply voltage (1.8V, 2.5V, 3.3V) for the Q_E[2:0] outputs.
9, 14	VDDO_QF	Power		Positive supply voltage (1.8V, 2.5V, 3.3V) for the Q_F[1:0] outputs.
8	VDDO_QG	Power		Positive supply voltage (1.8V, 2.5V, 3.3V) for the Q_G[1:0] outputs.
5, 74	VDDO_QH	Power		Positive supply voltage (1.8V, 2.5V, 3.3V) for the Q_H[2:0] outputs.
68	VDD33_CP0	Power		Positive supply voltage (3.3V) for the charge pump output of PLL-0.
26	VDD33_CP1	Power		Positive supply voltage (3.3V) for the charge pump output of PLL-1.
73	VDD_OSC0	Power		Positive supply voltage (1.8V) for the OSC_0 input and Q_VCXO outputs.
30	VDD33_OSC1	Power		Positive supply voltage (3.3V, 1.8V) for the OSC_1 input. This pin can also be supplied by 1.8V for setting the OSC_1 interface voltage to 1.8V.
29	VDD33_VCO	Power		Positive supply voltage (3.3V) for the internal VCO of PLL-1.
58	VDD_INPUT	Power		Positive supply voltage (1.8V) for the SPI interface and the differential clock inputs CLK0-1.

Table 1. Pin Descriptions (Cont.)

Pin	Name	Type[1]		Description
37	VDD_GPIO	Power		Positive supply voltage (1.8V) for the GPIO interface.
24	VDD_PLL1	Power		Positive supply voltage (1.8V) for PLL-1.
28	VCO_CAP	Analog		Internal VCO regulator bypass capacitor. Use a 1.0 µF capacitor from this pin to GND.
Exposed pad	GND	Power		Ground supply voltage (GND) and ground return path. Connect to board GND (0V).
23, 27	NC			Do not connect

1. PU (pull-up) and PD (pull-down) indicate internal input resistors (for values, see Table 57).

4. Principles Of Operation

4.1 Overview

The 8V19N882 generates low-phase noise, synchronized clock and SYSREF output signals locked to an input reference frequency. The device contains two PLLs with configurable frequency dividers. The first PLL (VCXO-PLL or PLL-0) uses an external VCXO (f_{VCXO}) as the oscillator and provides jitter attenuation to the input signal. The external loop filter is used to set the VCXO-PLL bandwidth frequency in conjunction with internal parameters. A VCXO buffer output is available for cascading multiple devices or to drive other clock devices at the VCXO frequency.

The second, low-phase noise PLL (PLL-1) multiplies the PLL-0 frequency to a high frequency from which all output signals are generated. PLL-1 can use an external oscillator (VCO, f_{VCO}) in the range of 700MHz to 6GHz, or use the internal oscillator of 3932.16MHz. The use of the internal oscillator is sufficient for most applications; only applications requiring extraordinary low phase noise or frequency plans can use an external oscillator for PLL-1. Each PLL can be bypassed. PLL-0 bypass is recommended for applications with clean input clock signals: PLL-1 will synthesize the output clock signals directly from the selected input. The PLL-0-bypass mode does not require an external VCXO component.

If the VCXO frequency is suitable as the highest application frequency, PLL-1 can be bypassed.

The output of PLL-1 (output of PLL-0 if PLL-1 is bypassed) provides a central timing reference point for all output signals. From this point, fully synchronous dividers generate the output frequencies and the internal timing references for JESD204B/C support.

The device supports the generation of SYSREF pulses synchronous to the clock signals. There are eight output channels, each can be configured as a clock or SYSREF channel. The clock outputs are configurable with support for LVPECL or LVDS formats and a variable output amplitude. Each channel and each output offer adjustable phase delay functionality. Individual outputs and channels and unused circuit blocks support powered-down states for operating at lower power consumption.

The synchronous design allows an operation mode with deterministic phase delay between the active input and any clock and SYSREF output and also allows zero-delay configurations. Desired input-to-output and output-to-output phase relations can be configured by the programmable phase delay circuits. The deterministic delay capabilities support cascading multiple devices.

For redundancy purpose, there are two selectable reference frequency inputs and a configurable switch logic with priority-controlled auto-selection and holdover support.

The register map, which is accessible through the SPI interface with read-back capability, controls the main device settings and delivers device status information. Two configurable I/O pins can be used for general-purpose I/O, control, or status signaling functions.

4.2 Phase-Locked Loop Operation

4.2.1 Frequency Generation

The 8V19N882 generates output frequencies in one of three modes: dual PLL mode, frequency synthesizer mode, and PLL-0 mode. Frequency dividers must be set by the user to match input and oscillator frequencies to achieve frequency and phase lock on the used PLLs. The frequency of the external VCXO and external VCO (if used) is selected by the user; the internal VCO frequency of PLL-1 is set to 3932.16MHz.

Table 2. PLL Modes

Mode	Description	Configuration
Dual PLL	Input jitter attenuation	BYP_0 = 0, SRC = 00 or 01
Frequency Synthesizer	Frequency generation without jitter attenuation	BYP_0 = 1, SRC = 00 or 01
VCXO-PLL	Input jitter attenuation, output frequency ≤ f_{VCXO}	SRC = 10
PLL Bypass	Fanout buffer/frequency divider	SRC = 11, BYP_0 = 1

4.2.1.1 Dual PLL Mode

Application for the dual PLL mode is input clock jitter attenuation and frequency generation. PLL-0 must use an external VCXO and PLL-1 uses the internal VCO or an external VCO for frequency generation. Set BYP_0 = 0. The dividers for both PLLs must be configured to achieve frequency lock. Figure 4 displays a detailed circuit and Table 3 shows the available frequency dividers for this mode. For information on selecting the feedback path for this mode, see PLL Feedback Path. Input to output delay is deterministic when the device is configured in dual PLL mode and the PLL feedback path is set through both M_0 and M_1 feedback divider (FBSEL_PLL_0 = 1).

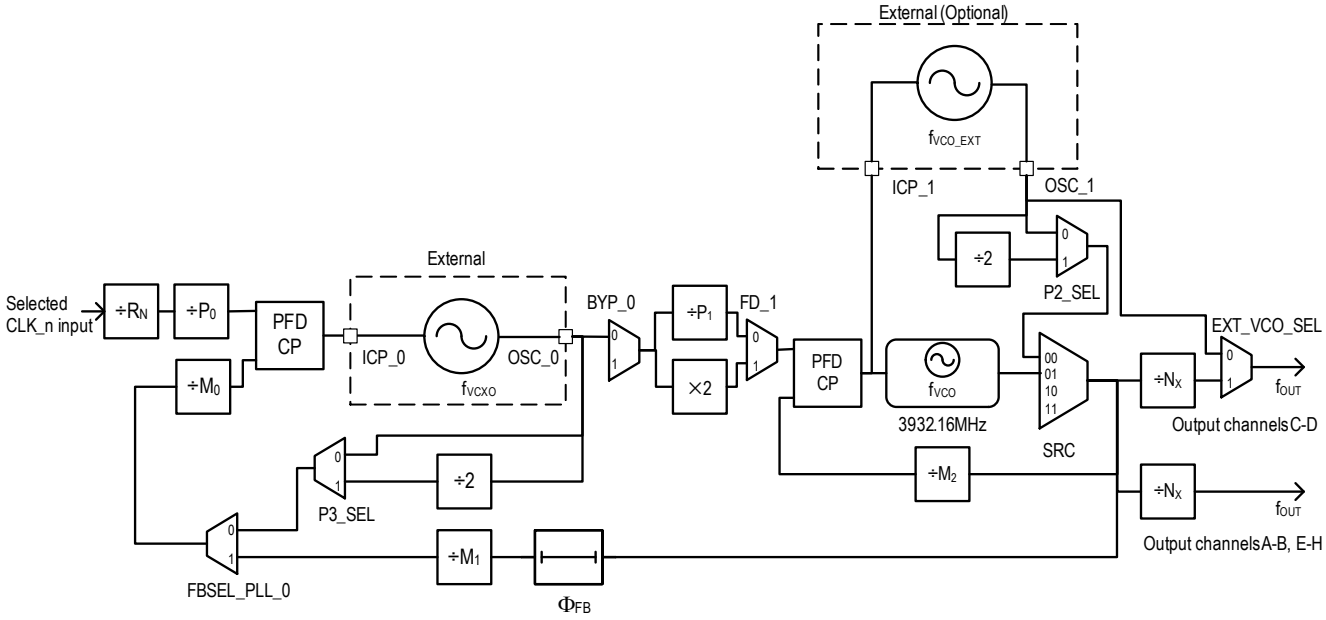


Figure 4. Dual PLL Mode

Table 3. Dual PLL Mode Settings and Divider Values

Divider	Range	Operation for f_{VCO} = 3932.16MHz[1]
Input Divider R_N[2]	÷1, ÷2, ÷4, ÷8	Input clock frequency (FBSEL_PLL_0 = 1): $f_{CLK} = R_N \times P_0 \times \frac{f_{VCXO}}{P_1} \times \frac{M_2}{M_0 \times M_1}$
PLL-0 Pre-Divider P_0	÷1…÷32,767: (15 bit)	
PLL-0 Feedback Divider M_0	÷1…÷32,767: (15 bit)	
PLL-0/1 Feedback Divider M_1[3]	÷1…÷16,383: (14 bit)	
PLL-1 Pre-Divider P_1	÷1…÷127: (7 bit)	VCXO frequency: $f_{VCXO} = f_{VCO} \times \frac{P_1}{M_2}$ P_1: Set P_1 to 0.5 in above equation if the frequency doubler is engaged by setting FD_1 = 1.
Frequency Doubler	FD_1 = ×1 or ×2	
PLL-1 Feedback Divider M_2[4]	÷1 …÷1,023: (10 bit)	

Table 3. Dual PLL Mode Settings and Divider Values (Cont.)

Divider	Range	Operation for f_{VCO} = 3932.16MHz[1]
Clock Output Divider N_x (x = A, B, C, D, E, F, G, H)	÷1…÷20,480 N = {1,2,3,4,5} × 2^m with m = 0 to 12	Output clock frequency: $f_{OUT} = \frac{f_{VCO}}{N_X}$
SYSREF Output Divider N_x (x = A, B, C, D, E, F, G, H)	÷1…÷83,886,080 N = {1,2,3,4,5} × 2^m× 2^p with m = 0 to 12 and p = 1 to 12	Output SYSREF frequency: $f_{OUT} = \frac{f_{VCO}}{N_X}$

1. External VCO operation: use the frequency of the external VCO for f_{VCO} in above equations. For external VCO frequencies greater than 4GHz, set P2_SEL to select the ÷2 path to reduce the external VCO frequency and enter f_{VCO}÷2 as VCO frequency in above equations.
2. Input divider R_N: Use R_N to limit the input frequency to the P_0 divider to ≤ 250MHz.
3. Maximum M_1 input frequency is: 1GHz for M_1 = ÷1…÷7 and 4GHz for M_1>÷7
4. Maximum M_2 input frequency is: 1GHz for M_2 = ÷1…÷7 and 4GHz for M_2>÷7

4.2.1.2 Frequency Synthesizer Mode

The application for the frequency mode is frequency generation by PLL-1. PLL-0 is bypassed by setting BYP_0 = 1. It is not required to fit an external VCXO in this mode. PLL-1 can use the internal VCO or an external VCO. The dividers of PLL-1 must be configured to achieve frequency lock to the selected clock input. Figure 5 displays a detailed circuit and Table 4 shows the available frequency dividers for this mode.

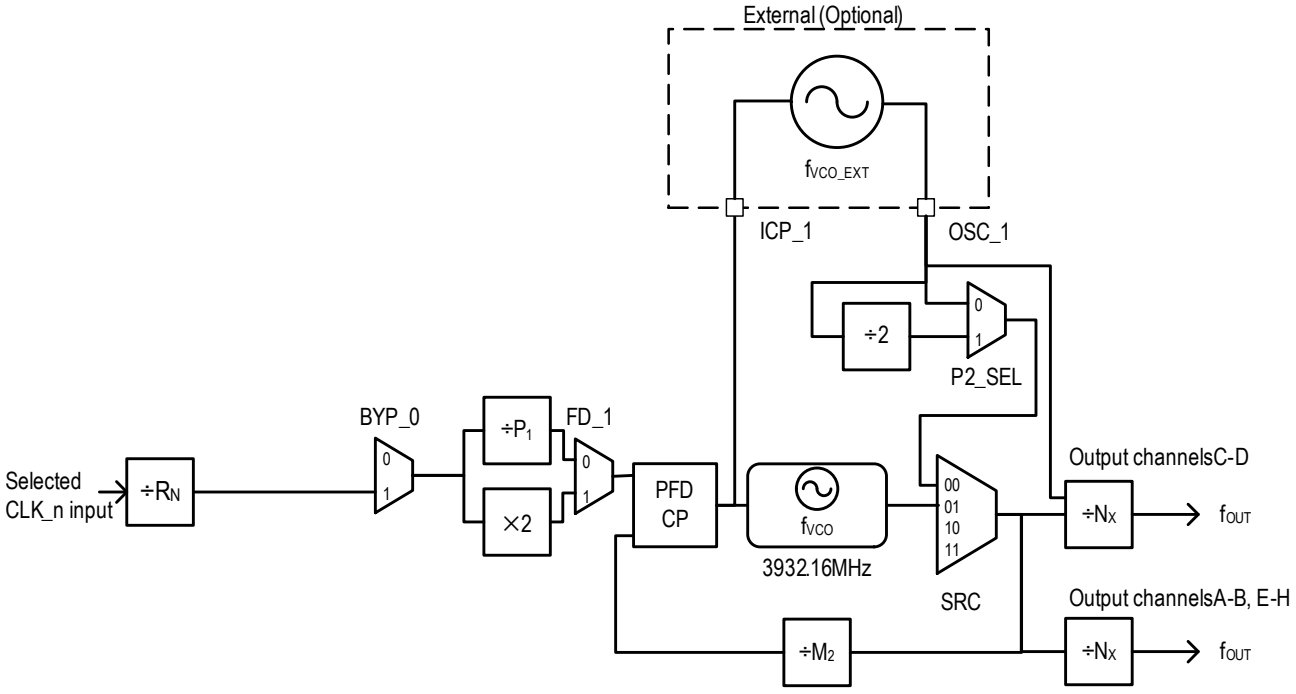


Figure 5. Frequency Synthesizer Mode

Table 4. Frequency Synthesizer Mode Settings and Divider Values

Divider	Range	Operation for f_{VCO} = 3932.16MHz[1]
Input Divider R_N	÷1, ÷2, ÷4, ÷8	Input clock frequency: $f_{CLK} = f_{VCO} \times \frac{R_N \times P_1}{M_2}$ P_1: Set P_1 to 0.5 in above equation if the frequency doubler is engaged by setting FD_1 = 1.
PLL-1 Pre-Divider P_1	÷1…÷127: (7 bit)	
Frequency Doubler	FD_1 = ×1 or ×2	
PLL-2 Feedback Dividers M_2	÷8 …÷1,023: (10 bit)	
Output Divider N_x (x = A, B, C, D, E, F, G, H)	÷1…÷20,480 N = {1,2,3,4,5} × 2^m with m = 0 to 12	Output (clock or SYSREF) frequency: $f_{OUT} = \frac{f_{VCO}}{N_X}$

1. External VCO operation: use the frequency of the external VCO for f_{VCO} in above equations. For external VCO frequencies greater than 4GHz, set PS_SEL to select the ÷2 path to reduce the external VCO frequency and enter f_{VCO}÷2 as VCO frequency in above equations.

4.2.1.3 VCXO-PLL Mode

Application for the VCXO-PLL mode is input clock jitter attenuation without the use of PLL-1 for additional frequency generation. Set SRC[1:0] = 10 to bypass PLL-1. PLL-0 must use an external VCXO. The frequency of the VCXO component determines the highest frequency that can be generated at the outputs. The PLL-0 dividers P_0 and M_0 must be configured to achieve frequency lock. For VCXO frequencies higher than 250MHz, set P3_SEL = 1 to select an additional divide-by-2 in the PLL-0 feedback path. Figure 6 displays a detailed circuit and Table 5 shows the available frequency dividers for this mode.

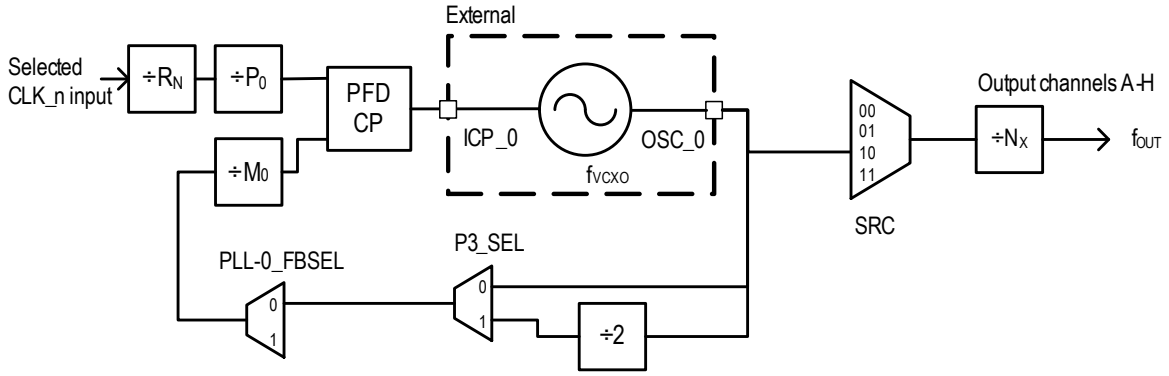


Figure 6. VCXO-PLL Mode

Table 5. VCXO-PLL (PLL-0) Mode Settings and Divider Values

Divider	Range	Operation (no VCO)
Input Divider R_N	÷1, ÷2, ÷4, ÷8	Input clock frequency (f_{VCXO}≤250MHz): $f_{CLK} = R_N \times P_0 \times \frac{f_{VCXO}}{M_0}$ P3_SEL: Set to 1 for VCXO frequencies higher than 250MHz: $f_{CLK} = R_N \times P_0 \times \frac{f_{VCXO}}{2 \times M_0}$
PLL-0 Pre-Divider P_0	÷1…÷32,767: (15 bit)	
PLL-0 Feedback Divider M_0	÷1…÷32,767: (15 bit)	
Output Divider N_x (x = A, B, C, D, E, F, G, H)	÷1…÷20,480 N = {1,2,3,4,5} × 2^m with m = 0 to 12	Output frequency: $f_{OUT} = \frac{f_{VCXO}}{N_X}$

4.2.1.4 PLL Bypass (Fanout Buffer/Frequency Divider) Mode

Application for the buffer/divider mode is the fanout of the input signal with optional frequency division. PLL-0 and PLL-1 are not used in this mode, thus frequency multiplication, input jitter attenuation, automatic input switching, PLL lock and input loss detection are not available. Inputs must be selected manually by using the SEL[1:0] register bits. Set BYP_0 to 1, FD_1 = 0 and SRC = 11. The dividers R_N, P_1 and the output dividers frequency divide the input frequency, the three dividers can be set to a value of ÷1 to replicate the input frequency at the outputs.

The highest frequency that this mode supports is limited to the maximum input frequency (2GHz). Figure 7 displays a detailed circuit and Table 7 shows the available frequency dividers for this mode. The output divider N_x can be used to divide the input frequency to lower output frequencies (it is recommended to use R_N = ÷1 and P_1 = ÷1). The delay circuits use a delay unit controlled by the clock signal frequency at the SRC multiplexer.

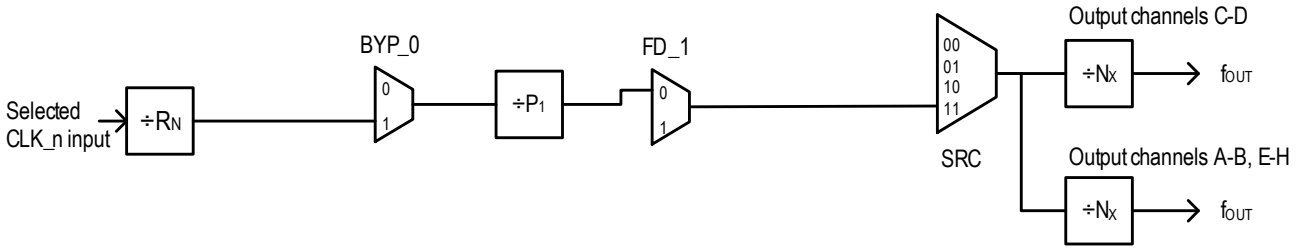


Figure 7. PLL Bypass Mode

Table 6. PLL Bypass (Fanout Buffer/Frequency Divider) Mode

Divider	Range	Operation (no VCO)
Input Divider R_N	÷1, ÷2, ÷4, ÷8	Output frequency: $f_{OUT} = \frac{f_{CLK}}{R_N \times P_1 \times N_x}$
PLL-1 Pre-Divider P_1	÷1…÷127: (7 bit)	
Output Divider N_x (x = A, B, C, D, E, F, G, H)	÷1…÷20,480 N = {1,2,3,4,5} × 2^m with m = 0 to 12	

4.2.2 PLL Description

4.2.2.1 VCXO-PLL (PLL-0)

The FBSEL_PLL_0 register bit controls the routing of the VCXO-PLL feedback path applicable in dual PLL mode. PLL feedback is routed through the M_0 divider; alternatively, the feedback path is routed through the second PLL and both the M_0 and M_1 feedback divider. The recommended feedback path for achieving deterministic phase delay from the clock input to the outputs is the path through both the M_0 and M_1, in combination with the divider setting P_1 = ÷1. The pre-dividers R_N and P_0, and the feedback dividers M_0 and M_1, require configuration to match the input frequency to the VCXO-frequency. M_0 has a divider value range of 15 bits; M_1 has 14 bits. Multiple divider settings are available to enable support for input frequencies of e.g. 245.76, 122.88, 61.44 and 30.72MHz and the VCXO-frequencies of 122.88MHz, 61.44, 38.4, 30.72, 245.76 and 491.52MHz. In addition, the range of available input and feedback dividers allows to adjust the phase detector frequency independent on the input and VCXO frequencies.

The PLL-0 charge pump is configurable via the I_CP0, I_CP0_SINK_EN, and I_ICP0_OFFSET registers. The charge pump current can be set in the range up to 3mA in 100 or 200µA steps. At startup, the VCXO control voltage at the ICP_0 pin is held at 50% of the VDD33_CP0 voltage level (1.65V) to center the VCXO frequency (FCV0 = 1). After startup, the user must set the FVC_0 control bit to 0 to enable VCXO-PLL lock. Input clock switching and holdover functions require the use of the VCXO-PLL in the active signal path.

Low input frequency configurations: If the input frequency after the divider R_N is lower than the output of the M_1 divider, then the user must set the “BLOCK_LOR” register bit to 1 in order for PLL-0 to operate correctly. In this condition, the LOS (Loss of input signal) function is not valid, also preventing the automatic input switching function of the device.

In frequency synthesizer mode, PLL-0 is not used and holdover functions are not available.

Table 7. PLL-0 Example Configurations for f_{VCXO} = 122.88MHz[1]

Input Frequency (MHz)	PLL-0 Divider Settings			f_{PFD} (MHz)
	R_N	P_0	M_0	
245.76	1	2	1	122.88
	1	32	16	7.68
	1	256	128	0.96
	1	2048	1024	0.12
122.88	1	1	1	122.88
	1	16	16	7.68
	1	128	128	0.96
	1	1024	1024	0.12
1966.08	8	2	1	122.88

1. BYP_1=0

4.2.2.2 PLL Feedback Path

PLL-0 uses M_0 or $M_0 \times M_1$; PLL-1 uses M_2 as the feedback divider. Configuring the feedback path through the M_0 and M_1 dividers enables deterministic delay from the input to the outputs (for more information, see Table 8).

Table 8. VCXO-PLL (PLL-0) Feedback Path Settings

FBSEL_PLL_0	Operation
0	Independent PLL feedback. PLL-0 feedback path through the M_0 divider (and through an additional ÷2 if P3_SEL = 1) PLL-1 feedback path uses the M_2 divider.
1	Recommended feedback configuration for achieving deterministic delay from input to the outputs. PLL-0 feedback path through the $M_1 \times M_0$ dividers. PLL-1 feedback path uses the M_2 divider.

4.2.2.3 PLL-1

PLL-1 is a high-frequency synthesizer. This PLL locks to the output signal of PLL-0 in dual PLL mode or to the input frequency in frequency synthesis mode. PLL-1 uses the internal VCO (3932.16MHz) or an external VCO at any frequency from 700MHz to 6GHz. Achieving PLL lock requires the configuration of FD_1 (frequency doubler) or P_1 (pre-divider), and the feedback divider M_2 to match the input and feedback frequency at the phase detector. These settings may change depending on the actual VCO and input frequencies. If the external VCO frequency f_{VCO} is greater than 4GHz, set P2_SEL to 1 to select the path through the divider ÷2. The effective VCO frequency routed to the PLL-1 feedback divider, output divider, and SYSREF generator is then f_{VCO}÷ 2. The P2_SEL setting also impacts the reference frequency for the delay circuits: the frequency at the SRC multiplexer output is the reference frequency for all digital delay circuits. The M_2 feedback divider in PLL-1 is integer. The PLL-1 charge pump is configurable via the I_CP1, I_CP1_SINK_EN, and I_ICP1_OFFSET registers. The charge pump current can be set in the range up to 3mA in 100 or 200µA steps.

This PLL is internally configured to high-bandwidth. Best phase noise is typically achieved by engaging the internal frequency doubler (FD_1 = 1, ×2). If engaged, the input signal to PLL-1 is first doubled in frequency, increasing the phase detector frequency of PLL-1. Enabling the frequency doubler disables the frequency pre-divider P_1. If the frequency doubler is not used (FD_1 = 0), the P_1 pre-divider has to be configured. Typically P_1 is set to ÷1 to keep the phase detector frequency as high as possible. Set P_1 to other divider values to achieve specific frequency ratios (1 to 19.2, 1 to 76.8, etc.) between the first and second PLL.

Table 9. PLL-1 Mode

Description	RF_PLL Operation[1]	M_2 Registers
Integer frequency synthesis	$f_{VCO} = f_{PFD\_1} \times M2$	0x2C - 0x2D

1. f_{PFD_1} is the phase detector frequency of PLL-1. In dual PLL mode, f_{PFD_1} is the output frequency of PLL-0 divided by P_1 or multiplied by 2.

Table 10. Frequency Doubler

FD_1	Operation
0	Frequency doubler off (×1). P_1 divides the PLL-1 input signal
1	Frequency doubler on (×2). The PLL-1 input signal is doubled in frequency. The P_1 divider has no effect.

Table 11. Example PLL-1 Configuration

PLL-1 Input-Frequency (MHz)	PLL-1			
	FD_1	P_1	M_2	f_{VCO} (MHz)
122.88	×2	–	16	3932.16
245.76	×2	–	8	3932.16
245.76	×1	1	16	3932.16
491.52	×1	1	8	3932.16
491.52	×1	2	12	5898.24 (external)

4.2.3 PLL-0 (VCXO-PLL) Lock Detect

The PLL-0 lock detect circuit uses the signal phase difference at the phase detector as lock criteria; the phase detector is fed by the output signals of the M_0 and P_0 dividers. PLL lock is reported when the phase difference between both signals into the PLL-0 phase detector is lower than or equal to the phase difference set by LOCK_TH[14:0] for more than the number clock cycles (of the M_0 divider output) set by LOCK_GOOD_COUNT[1:0]. PLL-0 lock state is reported through the ST_PLL0_LOCK (momentary) and LS_PLL0_LOCK (sticky, resettable) status bits (for status bit functions, see Table 25). PLL lock can be reported by a GPIO pin. Loss-of-lock can also be signaled as interrupt signal via a GPIO pin.

The PLL-0 lock detect function is available in dual PLL and VCXO-PLL (PLL-0 only) mode. The divider M_0 is used as frequency divider for the comparison signal. The M_0 divider must be set to a value equal to or greater than ÷4 for lock detect to work correctly.

A static clock input is detected as PLL loss of lock. PLL-0 lock detect is not available in PLL bypass (fanout buffer) mode or in configurations that do not feed a clock signal to the frequency divider M_0. The maximum input frequency to the M_0 and P_0 dividers is 250MHz. For higher input frequencies than 250MHz, use the R_N divider to divide the frequency down to ≤ 250MHz. The lock detect circuits works for the input frequencies that achieve PLL-0 lock. Setting the FVC_0 register bit will unlock PLL-0 and identifies this as a loss of lock condition. Entering holdover also reports a PLL-0 loss of lock.

4.2.4 PLL-1 Lock Detect

PLL-1 lock detect evaluates the calibration state machine status flag for completion and compares the PLL-1 loop filter voltage to a voltage range (window). PLL-1 lock is signaled through the ST_PLL1_LOCK (momentary) and LS_PLL1_LOCK (sticky, resettable) status bits (see Table 25). Lock status can be reported as a hardware signal through the GPIO_[1:0] pin interface.

A static clock input to PLL-1 is detected as loss of lock. The PLL-1 lock detect function is available in dual PLL and synthesizer mode (PLL-1). PLL-1 lock detect works up to the specified PLL-1 phase detector frequency (500MHz) and over the entire frequency range PLL-1 lock range. PLL-1 lock detect is not supported in configurations that do not use PLL-1. Lock detect is also available in PLL synthesizer mode with an external VCO.

4.3 Output Channel and JESD204B/C Logic

4.3.1 Channel Description

The 8V19N882 has eight output channels with a total of 16 differential channels plus one VCXO output channel. Two channels (A, G) support one differential output, four channels (B, C, D, F) support two differential outputs, and two channels (E, H) support three differential outputs. The outputs of channels C and D support output frequencies up to 6GHz and require a 3.3V output supply. Channels A, B, E, F, G, and H are supplied by 1.8V, 2.5V, or 3.3V and support output frequencies up to 4GHz.Each channel can be configured as a clock channel or as a SYSREF channel by using the respective nC/S_SEL_x multiplexer register bit. The clock/SYSREF configuration applies to all outputs of a channel.

Table 12. Output Channel Description

Channel	Number of Outputs	Output Signals	Output Supply Voltage	Diagram
A, G	1	▪ Clock ≤ 4GHz (from PLL-1) or ▪ SYSREF	1.8V, 2.5V, 3.3V	Figure
B, F	2	▪ Clock ≤ 4GHz (from PLL-1) or ▪ SYSREF	1.8V, 2.5V, 3.3V	Figure
C, D	2	▪ Clock ≤ 6GHz (directly from OSC_1 input) or ▪ Clock ≤ 4GHz (from PLL-1) or ▪ SYSREF	3.3V	Figure 9
E, H	3	▪ Clock ≤ 4GHz (from PLL-1) or ▪ SYSREF	1.8V, 2.5V, 3.3V	Figure

4.3.1.1 Clock/SYSREF Channels A, B, E, F, G, H

The channels A, B, E, F, G, and H can operate as a device clock or as a SYSREF channel, controlled by the nC/S_SEL_x selector (for information, see Figure 8).

4.3.1.1.1 Clock Operation

A channel configured to clock operation (nC/S_SEL_x = 0) contains a two-stage frequency divider N_x and one digital phase delay circuit Φ_{WIDE_x}. Frequency and phase settings are applied to all outputs of a channel. The purpose of the N_x divider is frequency generation from the selected frequency source (SRC multiplexer). N_x can be set to a range of discrete values from ÷1 to ÷20,480. N_x is a composite divider consisting of two serial dividers N_x0 and N_x1: N_x = N_x0 × N_x1. For example, setting N_x0 to ÷2 and N_x1 to ÷8 will result in a channel frequency divider of N_x = ÷16. This example divider value generates an output frequency of 245.76MHz if the internal VCO is used. Clock channels with different clock frequencies are synchronized on the incident edge. The digital phase delay circuit Φ_{WIDE_x} is used to apply phase offsets in the channels.

4.3.1.1.2 SYSREF Operation

A channel configured to clock operation (nC/S_SEL_x = 1) participates in the central SYSREF pulse/frequency generation. The clock divider N_x divides the selected source signal to the SYSREF frequency. Similar to clock operation, the frequency is applied to all outputs of that channel. N_x can be set to a range of discrete values from ÷1 to ÷83,886,080. N_x consists of three serial dividers N_x0, N_x1, and N_S: N_x = N_x0 × N_x1 × N_S. For example, setting N_x0 to ÷2, N_x1 to ÷8, and N_S to ÷32 will result in a SYSREF frequency divider of N_x = ÷512. This example divider value generates a SYSREF output frequency of 7.68MHz if the internal VCO is used. A N_S divider physically exists in each channel, however, all N_S dividers share the same global setting (N_S in register 0x38). For phase delay, a SYSREF channel contains the circuits Φ_{WIDE_x}, Φ_{FINE_y}, and Φ_{ANLG_y}. Similar to a clock channel, Φ_{WIDE_x} phase settings are applied to all channel outputs. Each output can use the additional delay circuits Φ_{FINE_y} and Φ_{ANLG_y} for output-to-output fine phase alignment. These output delay circuits are unavailable when the channel is configured to clock operation.

4.3.1.1.3 Synchronization of Clock and SYSREF Channels

The device can synchronize the phase of clock and SYSREF outputs across channels. For synchronization, rules apply for the selection of N_x0 and N_x1 dividers. In a SYSREF channel, the input frequency to the N_S divider block must be set to a common divisor of the frequencies of the clock channels. For example, channels A, B, and E are configured as clock channel with the output frequencies of 122.88MHz (channel A, N = 32), 245.76 MHz (channel B, N = 16) and 983.04MHz (channel E, N = 4); channel F is configured to SYSREF at 7.68MHz. A common divisor of the three clock frequencies in channels A, B, and E is 122.88MHz. This divisor is calculated by dividing the VCO frequency by the lowest common multiple clock frequency divider: 3932.16MHz ÷ LCM(32, 16, 4). In the SYSREF channel, the input to the N_S divider must now be configured to 122.88MHz (by setting N_x0 × N_x1 to ÷32: the VCO frequency of 3932.16MHz is divided by 32). The SYSREF divider N_S is then configured to 16 to achieve 7.68MHz at the channel F outputs. Failure to set the SYSREF channel divider to a common frequency of the clock channels may result in the SYSREF outputs not being synchronous to clock outputs.

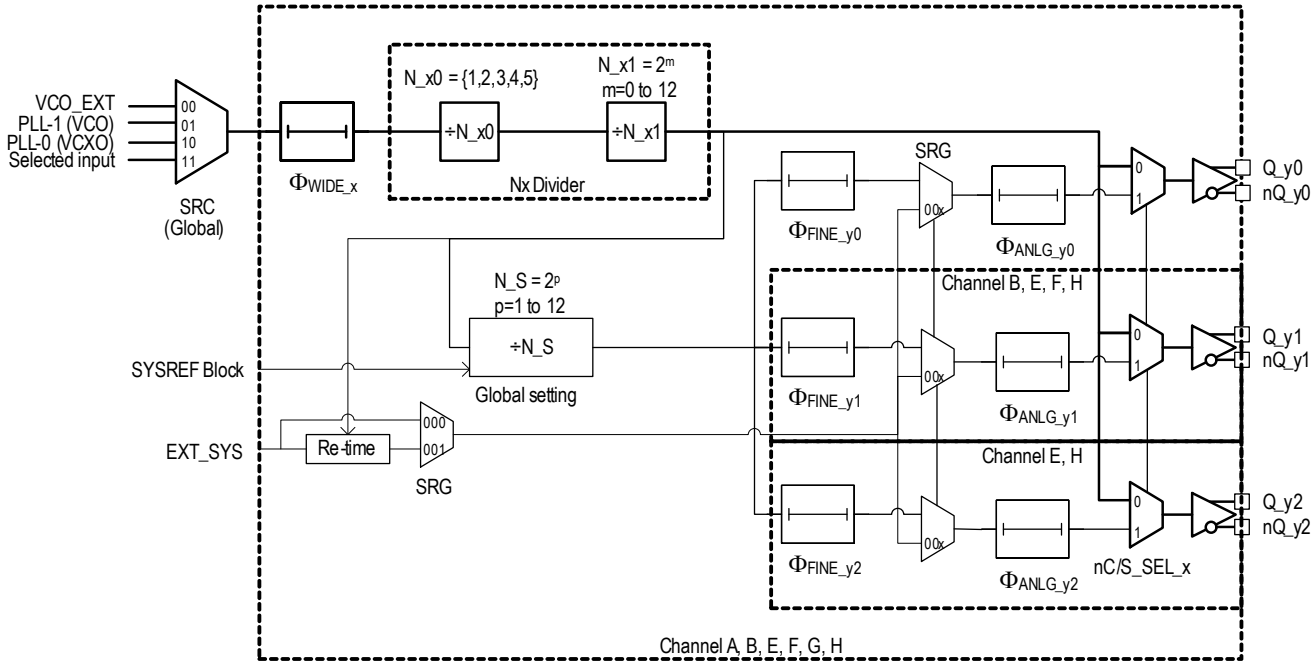


Figure 8. Output Channels A, B, E, F, G, and H

4.3.1.2 6GHz RF Clock/SYSREF Channels C, D

The two RF clock channels C and D buffer the external oscillator signal (VCO_EXT) up to an output frequency of 6GHz (see Figure 9). Alternatively, the channels C and D operate as device clock/SYSREF signal channel as described in Clock/SYSREF Channels A, B, E, F, G, H where the frequency source is PLL-0 or PLL-1 (internal

VCO). In the alternative mode, the maximum output frequency is 4GHz. For channels C and D, the output supply voltage is V_{DDO33_V} = 3.3V.

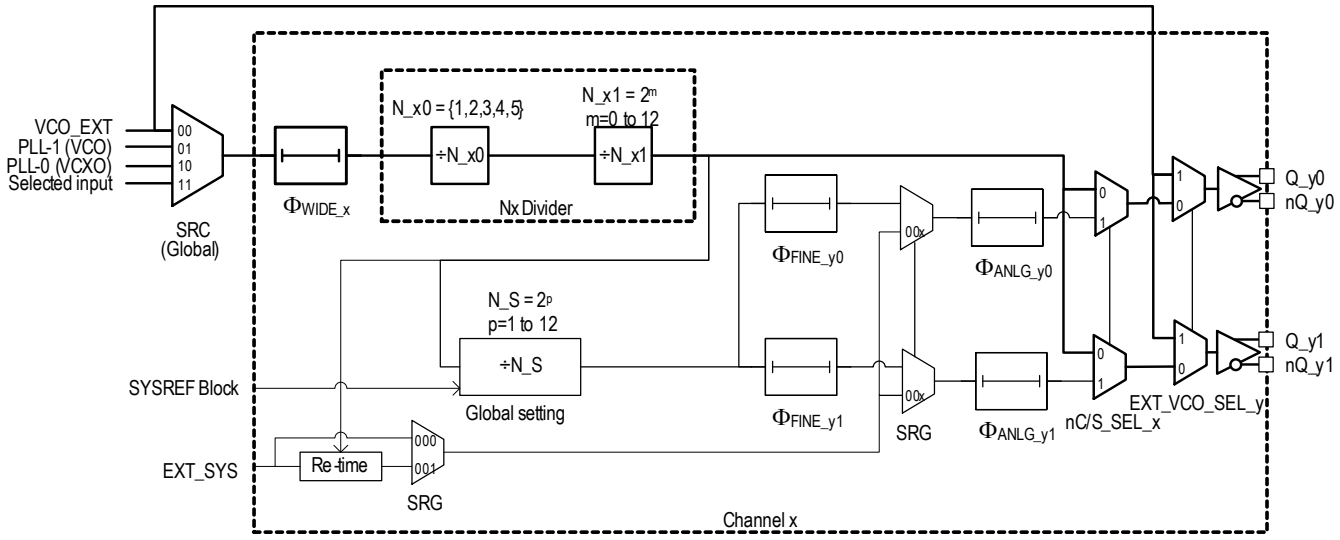


Figure 9. RF Output Channels C, D (Two Outputs)

4.3.2 Clock Delay Circuits

The purpose of the phase delay circuits is to establish a desired phase relationship between the selected input and any output, and across outputs (see Table 13). In JESD204B/C applications, the delay circuits establish phase offsets between SYSREF signals and their corresponding device clocks. The phase delay circuits Φ_{FB}, Φ_{WIDE_x}, and Φ_{FINE_y} (for SYSREF) are a function of the source frequency at the output of the SRC multiplexer.

If the *internal VCO* (3932.16MHz) is the channel signal source: the delay step size is selectable 127ps (one-half VCO cycle, channel delay) or 254ps (one VCO cycle, SYSREF delay). If an *external VCO* or *external VCXO* is the signal source: the frequency at the SRC multiplexer determines the delay units. External VCO frequencies of greater than 4GHz have to be divided by 2 (by using P2_SEL = 1). The Φ_{ANLG_y} circuits are implemented by gate delays and have a very small delay step size of approximately 30ps, independent of any internal or external VCO reference frequency.

The phase delay circuits Φ_{WIDE_x} have a wide range and can be used for coarse clock and SYSREF signal phase alignments. The delay circuits Φ_{FINE_y0} and Φ_{ANLG_y0}; Φ_{FINE_y1} and Φ_{ANLG_y1} are available in SYSREF channels and have a short range and finer resolution for use in board signal de-skewing and the exact placement of a SYSREF signal edge to the rising edge of a clock signal. Changing the setting of the delay circuit Φ_{FINE_y0} and Φ_{ANLG_y0}; Φ_{FINE_y1} and Φ_{ANLG_y1} will not result in output voltage transients, gaps, or runt pulses so that delay setting changes during device operation are supported.

Table 13. Delay Circuit Settings

Delay Circuit	Unit[1]	Steps	Range (ns)	Use for Alignment
PLL-0 Feedback Clock Φ_{FB}	$\frac{1}{f_{VCO}} = 254ps$	4096 (12 bit)	0 – 1,041.41	Input to output (incident edge) alignment.
Channel Clock Φ_{WIDE_x}	$\frac{1}{2 \times f_{VCO}} = 127ps$	512 (9 bit)	0 – 64.977	Incident rising clock edges are aligned, independent on the divider N_x across channels

Table 13. Delay Circuit Settings (Cont.)

Delay Circuit	Unit[1]	Steps	Range (ns)	Use for Alignment
Output SYSREF Φ_{FINE_y0} Φ_{FINE_y1} Φ_{FINE_y2}	$f_{VCO} \geq 2GHz$ and internal VCO: $\frac{1}{f_{VCO}} = 254ps$ $f_{VCO} < 2GHz$[2]: $\frac{1}{2 \times f_{VCO}}$	4 (2 bit)	0 – 0.763 0 – 3 ÷ ($2f_{VCO}$)	Output-to-output in channel and across channels, clock to SYSREF alignment. Can be powered down for lowest noise floor operation.
Output SYSREF Φ_{ANLG_y0} Φ_{ANLG_y1} Φ_{ANLG_y2}	30ps (analog)	8 (3 bit)	0 – 0.210	

1. Table is valid for using the internal VCO at a frequency of 3932.16MHz. For an external VCO, replace f_{VCO} by the actual VCO frequency or VCO frequency ÷ 2 if greater than 4GHz. Examples: external VCO of 2949.12MHz: Φ_{WIDE_x} is 169ps (P2_SEL = 0). External VCO of 5898.24MHz: Φ_{WIDE_x} is also 169ps (P2_SEL = 1, external VCO is pre-divided).
2. When using an external VCO at frequencies < 2GHz, the output SYSREF delay unit can be selected: $1/f_{VCO}$ and $1/2f_{VCO}$. See RETIME_DIV_x function.

4.3.3 Differential Outputs

Table 14. Output Features

Outputs	Description	Config.	Source	Supply Voltage	Style	Termination[1]	Ampl.[2] [3](mV)	Disable	Power Down
Q_C0-1, Q_D0-1	Clock ≤ 6GHz	EXT_VCO_SEL_y = 1	OSC_1	3.3V	LVPECL	50Ω to V_{TT}	300, 400, 550, 700	Y	Y
	Clock ≤ 4GHz	EXT_VCO_SEL_y = 0 nC/S_SEL_x = 0	PLL-0, PLL-1 or selected input	3.3V	LVPECL	50Ω to V_{TT}	300, 400, 550, 700		
	SYSREF	EXT_VCO_SEL_y = 0 nC/S_SEL_x = 1	SYSREF Generator	3.3V	LVPECL	50Ω to V_{TT}	300, 400, 550, 700	Y	Y
Q_A, Q_B0-1, Q_E0-2, Q_F0-1, Q_G, Q_H0-2	Clock ≤ 4GHz	nC/S_SEL_x = 0	PLL-0, PLL-1 or selected input	1.8V, 2.5V 3.3V	LVPECL	50Ω to V_{TT}	300, 400, 550, 700	Y	Y
					LVDS	100Ω differential	350, 500, line bias		
	SYSREF	nC/S_SEL_x = 1	SYSREF Generator	1.8V, 2.5V 3.3V	LVPECL	50Ω to V_{TT}	300, 400, 550, 700	Y	Y
					LVDS	100Ω differential	350, 500, line bias	Y	Y
Q_VCXO	PLL-0 buffered output	-	PLL-0	1.8V	LVPECL	50Ω to V_{TT}	700	N	Y
					LVDS	100Ω differential	350		

1. AC coupling and DC coupling supported.
2. Amplitudes are measured single-endedly.
3. See Table 17 for LVPECL termination voltages (V_{TT}).

Table 15. Q_y Output States in Clock Mode (nC/SEL = 0)[1]

PD	EN	Output Operation Description
0	0	Static low (Q = low, nQ = high)[2]
	1	Switching (Clock)
1	X	Powered down

1. Clock mode: Configuration bits nBIAS_r, PD_SYSREF, BIAS_TYPE, and INV_SYS have no effect on Q_y outputs.
2. Output disable operation of Q_C and Q_D outputs when outputs are used for an external VCO (EXT_VCO_SEL_y = 1): Q = High and nQ = High.

Table 16. Q_y Output States in SYSREF Mode (nC/SEL = 1)

PD_y	EN	nBIAS	PD_SYSREF	BIAS_TYPE	INV_SYS	Output Operation Description[1]
0	0	X	X	X	X	Static low level
	1	0	0	0	0	Switching (SYSREF)[2]
					1	Switching (SYSREF inverted)[2]
				1	0	Switching (SYSREF) / crosspoint level[2]
					1	Switching (SYSREF inverted) / crosspoint level[2]
			1	0	0	SYSREF power down Static high level
					1	
				1	0	
					1	
		1	0	0	0	SYSREF static low level[2]
					1	
				1	0	SYSREF static crosspoint level[2]
					1	
			1	0	0	SYSREF power down Static high level
					1	
				1	0	
					1	
1	X	X	X	X	X	Powered down

1. Level description: Static low: Q = low, nQ = high; Static high: Q = high, nQ = high; Crosspoint: Q and nQ are both at the LVDS crosspoint voltage.
2. For more information, see Table 20.

Table 17. LVPECL Termination Voltage, V_{TT}

Output Supply Voltage	Amplitude (mV)	V_{TT}
V_{DDO_V} = 1.8V	300	0.25V (V_{DDO_V} - 1.55V)
	400	0.15V (V_{DDO_V} - 1.65V)
	550	GND
	700	GND
V_{DDO_V} = 2.5V	300	0.95V (V_{DDO_V} - 1.55V)
	400	0.85V (V_{DDO_V} -1.65V)
	550	0.7V (V_{DDO_V} - 1.8V)
	700	0.55V (V_{DDO_V} - 1.95V)
V_{DDO_V} = 3.3V	300	1.75V (V_{DDO_V} - 1.55V)
	400	1.65V (V_{DDO_V} - 1.65V)
	550	1.5V (V_{DDO_V} - 1.8V)
	700	1.35V (V_{DDO_V} - 1.95V)

4.4 Redundant Clock Inputs

The two inputs are compatible with LVDS and LVPECL signal formats, and also support single-ended signals.

4.4.1 Monitoring and LOS of Input Signal

The two inputs are individually and permanently monitored for activity. Inactivity is defined by a static input signal.

The clock input monitors compare the pre-divided device input frequency ($f_{CLK} \div R_N$) to the output frequency of the M_1 divider regardless of the internal feedback path using or not using M_1[1]. A clock input is declared invalid with the corresponding LOS (Loss-of-input-signal) indicator bit set after three consecutive missing clock edges (at the output of the respective R_N divider). LOS is reported for each input CLK*n* individually through the ST_CLK*n* (momentary) and LS_CLK*n* (sticky, resettable) status bits, see Table 25. LOS can be reported by a GPIO output and can also be signaled as an interrupt signal via a GPIO pin. When reported through a GPIO output, the LOS signal represents the combination of the LOS status of enabled CLK_*n* inputs (GPIO = 0: LOS on any of the enabled inputs, GPIO = 1: all enabled inputs are active). Disable unused inputs by the control bits DIS_CLK*n* to prevent false LOS reporting.

Dual PLL and synthesizer mode: the M_1 divider must be set so that the LOS detect reference frequency matches the pre-divided input frequency. For example, if the input frequency is 245.76MHz and R_N = ÷1, M_1 should be set to ÷16: The VCO frequency of 3932.16MHz divided by 16 equals the input frequency of 245.76MHz. For an input frequency of 122.88MHz, set M_1 to ÷32 etc. Failure to set M_1 to match the input frequency can result in a false LOS indication. The minimum frequency that the circuit can monitor is $f_{VCO} / M_1(MAX) = 0.24MHz$.

VCXO-PLL (PLL-0 only) mode: The VCXO drives the SRC multiplexer output. Set the M_1 divider to match: $f_{VCXO} \div M_1 = f_{CLK} \div R_N$

The LOS function is available in dual PLL, VCXO-PLL, and synthesizer mode (PLL-1 only). In each of the PLL modes, LOS uses the output of the M_1 divider as a comparison signal and requires a configuration of the M_1 divider as described above. With a valid M_1 configuration for LOS, the LOS function is available across the entire input frequency range up to 250MHz. For input frequencies higher than 250MHz, use the R_N divider to divide the input frequency to 250MHz or less.

4.4.2 Input Re-Validation

A clock input is declared valid and the corresponding LOS bit is reset after the clock input signal returned for user-configurable number of consecutive input periods. This re-validation of the selected input clock is controlled by the CNTV setting (verification pulse counter).

1. M_1 must be configured and powered-on by setting PD_M1 = 0.

4.4.3 Clock Selection

The device supports multiple input selection modes: manual, short-term holdover, and two automatic switch modes.

Table 18. Clock Selection Settings

Mode	Description	Application
Manual nM/A = 00	Input selection follows user-configuration of SEL[1:0]. Selection is *never* changed by the internal state machine. A failing reference clock will cause a LOS event and the PLL will unlock if the failing clock is selected. Re-validation of the selected input clock will result in the PLL to re-lock on that input clock. This mode is supported in each PLL and in PLL bypass (fanout buffer) mode.	Startup and external selection control
Automatic nM/A = 01	Input selection follows LOS status by user preset input switch priorities. A failing input clock will cause a LOS event for that clock input. If the selected clock has a LOS event, the device will immediately initiate a clock failover switch. The switch target is determined by pre-set input priorities. No valid clock scenario: If no valid input clocks exist, the device will not attempt to switch and will not enter the holdover state. The PLL is not locked. Re-validation of any input clock that is not the selected clock will result in the PLL to attempt to lock on that input clock (for more information, see Revertive Switching). This mode is supported in dual PLL and PLL synthesizer modes.	Multiple inputs with qualified clock signals
Short-term Holdover nM/A = 10	Input selection follows user-configuration of SEL[1:0]. Selection is never changed by the internal state machine. A failing reference clock will cause a LOS event. If the selected reference fails, the device will enter holdover *immediately*. Re-validation of the selected input clock is controlled by the CNTV setting. A successful re-validation will result in the PLL to re-lock on that input clock. This mode is supported in dual PLL and PLL synthesizer modes.	Single reference
Automatic with Holdover nM/A = 11	Input selection follows LOS status by user preset input priorities. Each failing input clock will cause a LOS event for that clock input. If the *selected* clock detects a LOS event, the device will go into holdover and the hold-off down-counter (CNTH) starts. The device initiates a clock failover switch *after* expiration of the hold-off counter. The switch target is determined by the preset input priorities. No valid clock scenario: If no valid input clocks exist, the device will not attempt to switch and will remain in the holdover state. Re-validation of any input clock will result in the PLL to attempt to lock on that input clock (for more information, see Revertive Switching). This mode is supported in dual PLL mode.	Multiple inputs

4.4.4 Holdover

In holdover state, the output frequency and phase is derived from an internal, digital value based on previous frequency and phase information. Holdover characteristics are defined in AC Characteristics.

4.4.5 Input Priorities

Configurable settings encompass two selectable priorities with the range 0 (lowest priority) to 3 (highest priority). If an input has the priority 0, it will not be selected as reference input for the PLLs. The user can change the input priorities at any time. In the automatic switch modes, input priority changes may cause immediate input selection changes.

4.4.6 Hold-off Counter

A configurable down-counter applicable to the “Automatic with holdover” selection mode. The purpose of this counter is a deferred, user-configurable, input switch after a LOS event. The counter expires when a zero-transition occurs; this triggers a new reference clock selection. The counter is clocked by the frequency-divided PLL-0 signal. The CNTR setting determines the hold-off counter frequency divider and the CNTH setting

the start value of the hold-off counter. For example, set CNTR to a value of ÷131072 to achieve 937.5Hz (or a period of 1.066 ms at f_{VCXO}= 122.88MHz): the 8-bit CNTH counter is clocked by 937.5Hz and the user-configurable hold-off period range is 0ms (CNTR = 0x00) to 272ms (CNTR = 0xFF). After the counter expires, it reloads automatically from the CNTH SPI register. After the LOS status bit (LS_CLK*n*) for the corresponding input CLK_*n* has been cleared by the user, the input is enabled for generating a new LOS event. The CNTR counter is only clocked if the device is configured in the clock selection mode “Automatic with holdover” *AND* the *selected* reference clock experiences a *LOS* event. Otherwise, the counter is automatically disabled (not clocked).

4.5 Revertive Switching

Revertive switching is applicable only to the two automatic switch modes shown in Table 18.

- Revertive switching enabled – Re-validation of any non-selected input clock(s) will cause a new input selection according to the user-preset input priorities (revertive switch). An input switch is only done if the re-validated input has a higher priority than the currently selected reference clock.
- Revertive switching disabled – Re-validation of a non-selected input clock has no impact on the clock selection. Default setting is revertive switching disabled.

4.6 Configuration for JESD204B Operation

4.6.1 SYSREF Generation

A SYSREF event is the generation of one or more consecutive pulses on Q_y outputs where the channel is configured to SYSREF operation. An event can be triggered by a SPI command or by a signal-transition on the EXT_SYS input. The number of SYSREF pulses generated and wait periods in between SYSREF pulses is programmable. The SYSREF signal can also be programmed to be continuous and be started and stopped by a signal on the EXT_SYS input. The N_x and N_S frequency divider in each channel configures the SYSREF frequency/pulse rate. SYSREF output pulses are aligned to coincident rising clock edges of channels configured as clock outputs. Device settings for phase alignment between Q_*y* outputs is discussed in Clock to SYSREF Phase Alignment.

The generation of SYSREF is available after the initial setup of output clock divider and phase delay stages. A SYSREF event will automatically turn on the SYSREF outputs. After the event, SYSREF outputs are automatically turned off (power-down). SYSREF outputs with the nBIAS bit set high will bias the outputs at the LVDS crosspoint voltage level. The following SYSREF pulse generation modes and trigger modes are available and configurable by SPI:

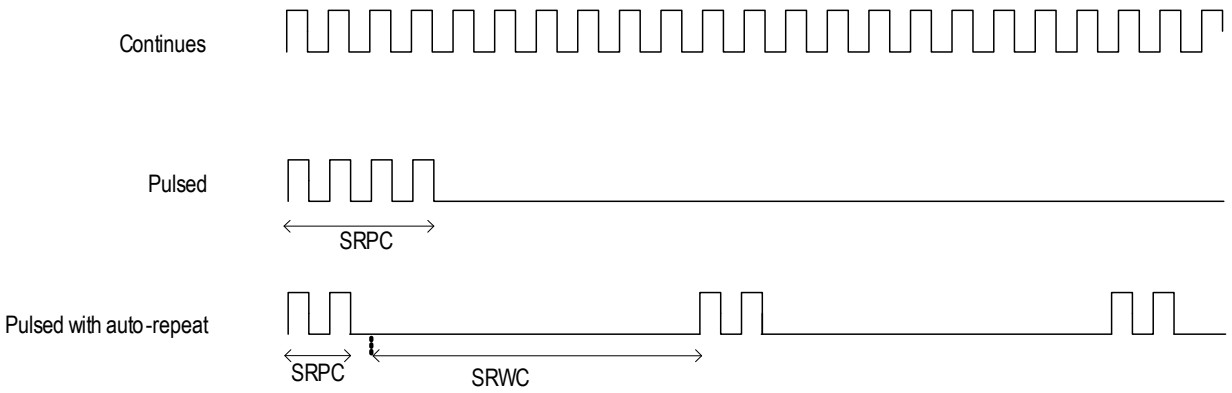


Figure 10. SYSREF Pulse Generation Modes

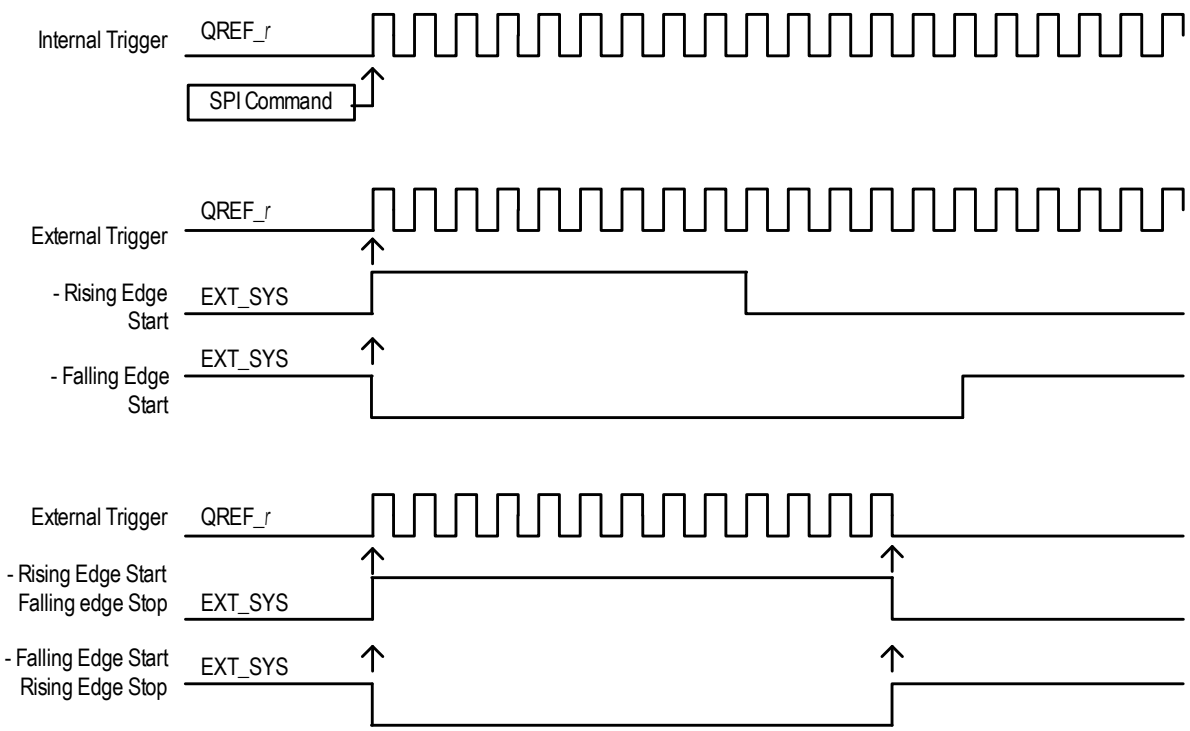


Figure 11. SYSREF Trigger Modes

Table 19. SYSREF Generation Modes

SRG	Operation	SYSREF Frequency	Pulse Generation	
			Trigger/Start	Stop
000	EXT_SYS input signal is buffered out to all SYSREF outputs[1]	Same as EXT_SYS	Same as EXT_SYS input	
001	EXT_SYS input signal is synchronized to the incident edge of the Q_y (clock) outputs and buffered out to all SYSREF outputs[2][3][4]		Same as EXT_SYS input	

Table 19. SYSREF Generation Modes (Cont.)

SRG	Operation	SYSREF Frequency	Pulse Generation		
			Trigger/Start		Stop
010	Externally triggered mode[5]	f_{VCO} ÷ (N_x × N_S)[6]	SRO		
			00	Pulsed, rising edge trigger	Automatically after pulse count ended[7]
			01	Pulsed, falling edge trigger	
			10	Rising EXT_SYS edge starts pulses	Falling EXT_SYS edge stops pulses
			11	Falling EXT_SYS edge starts pulses	Rising EXT_SYS edge stops pulses
011	Internally triggered mode		SRO		
			00	Pulsed Set INIT_REF = 1 to start	Automatically after pulse count ended
			01	Pulsed with auto repeat [8] Set INIT_REF = 1	Set SRG = 111
100	Continuous SYSREF mode		00, 10	Set INIT_REF = 1	Set SRG = 111
			01	Rising EXT_SYS edge starts pulses	Set SRG = 111
			11	Falling EXT_SYS edge starts pulses	Set SRG = 111
111	Terminate SYSREF generation[9]	—	—		

1. Requires external synchronization.
2. SRG = 001: Set the SYSREF channel Nx to ≥ 8. To sample the signal at EXT_SYS, the frequency f_{VCO}÷ Nx in the SYSREF channel should be ≥ 4 times higher than the frequency or pulse rate at EXT_SYS. The EXT_SYS input pulse width should be $T_P > 1 / (f_{VCO}÷Nx)$. Lower Nx dividers (higher output channel frequencies) allow narrower EXT_SYS input pulses.
3. SRG = 001 mode: The output of the (internal) Nx divider determines the signal edge of the SYSREF output (EXT_SYS going high: the next Nx divider rising edge will cause SYSREF outputs to from 0 to 1. EXT_SYS going low will cause SYSREF outputs to go low at the next Nx divider rising edge).
4. Synchronized to the output of the Nx channel divider.
5. Set the INIT_REF bit before the first external trigger signal on the EXT_REF input.
6. SYSREF output pulse duty cycle is 50% for SRG = 010, 011, 100.
7. Pulse count: Number of generated pulses set by SRPC register (1-255 pulses).
8. In pulsed mode with auto repeat, SRPC defines the number (1-255) of pulses to generate. SRWC defines the length of the stop period (in number of pulses, 1-255) before the next pulses are generated.
9. Terminates continuous SYSREF pulse generation by setting SRG to 111. Output pulses are not truncated (no runt pulse).

The generation of SYSREF pulses is configured by SPI commands and is available after the initial setup of output clock divider and Q_y phase delay stages. A SYSREF event will automatically turn on the SYSREF outputs. After the event in a pulsed mode, SYSREF outputs are automatically turned off (power-down or active low).

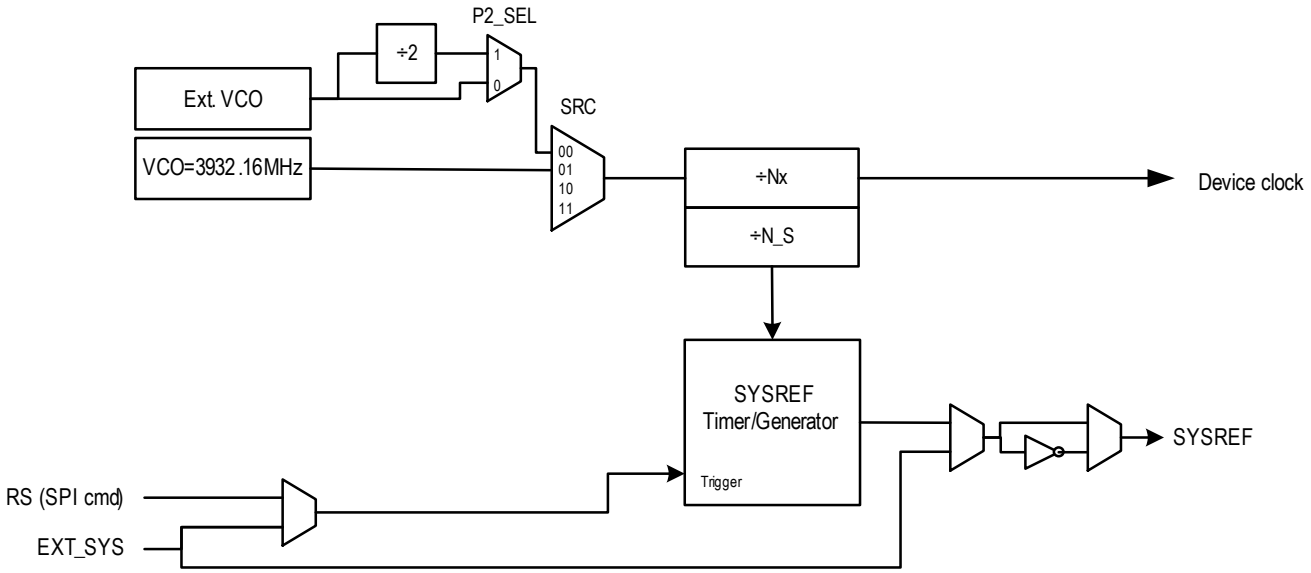


Figure 12. RF-PLL JESD204B Circuit Diagram

Table 20. Output Settings for JESD204B/C Applications

BIAS_TYPE	nBIAS_r	Q_y Output (in SYSREF operation)			Application
		Initial	During SYSREF Event	SYSREF Completed	
0	0	Static low (Q_y = L, nQ_y = H)	Start switching for the number of configured SYSREF pulses	Released to static low (Q_y = L, nQ_y = H)	Q_y DC coupled
	1	Static low (Q_y = L, nQ_y = H)			
1	0	Static LVDS crosspoint level (Q_y = nQ_y = VOS)	Start switching for the number of configured SYSREF pulses	Released to static LVDS crosspoint level (Q_y = nQ_y = VOS)	Q_y AC coupled
	1	Static LVDS crosspoint level (Q_y = nQ_y = VOS)			

4.6.2 Clock to SYSREF Phase Alignment

Figure 13 shows phase alignment between the input and any of the Q_y clock/SYSREF and Q_VCXO outputs. In any configuration, Q_y (clock or SYSREF) outputs are automatically aligned on the incident rising edge. Alignment between clock and SYSREF outputs and inputs is achieved by setting the delay circuits to the values specified in Table 21. The alignment is deterministic to the same phase positions across power cycles of the device. By changing the settings of the delay circuits, any phase offsets can be achieved. For example, Figure 14 shows an output phase configuration for clocking JESD204B/C receivers: the phase of the SYSREF outputs is advanced versus the incident edge of the clock outputs. The exact phase alignment can be adjusted by using the phase delay circuits (see Table 13). Different frequency/divider configurations than shown in Table 21 may require different phase delay settings.

Table 21. Example Settings for Phase Alignment

Block/Mode	Setting for Phase Alignment (Figure 13)		Setting for JESD204B/C (Figure 14)	
PLL mode	Dual PLL, internal VCO	M_0 = ÷32, M_1 = ÷32, M_2 = ÷16 FB_SEL = 1 Φ_{FB} = 6 SRG = 100	Dual PLL, internal VCO	M_0 = ÷32, M_1 = ÷32, M_2 = ÷16 FB_SEL = 1 Φ_{FB} = 6 SRG = 100
CLK_n input frequency	122.88MHz	R_N = ÷1 P_0 = ÷32, P_1 = ÷1	122.88MHz	R_N = ÷1 P_0 = ÷32, P_1 = ÷1
Q_VCXO output frequency	122.88MHz		122.88MHz	
Q_y Clock output frequency	122.MHz 245.76MHz 491.52MHz	N_x = ÷32, Φ_{WIDE} = 49 N_x = ÷16, Φ_{WIDE} = 49 N_x = ÷8, Φ_{WIDE} = 49	122.MHz 245.76MHz 491.52MHz	N_x = ÷32, Φ_{WIDE} = 53 N_x = ÷16, Φ_{WIDE} = 53 N_x = ÷8, Φ_{WIDE} = 53
Q_y SYSREF output	15.36MHz, continues or pulsed	N_x = ÷32 N_S = ÷8 Φ_{WIDE} = 40, Φ_{FINE} = 0 Φ_{ANLG} = 110b	7.68MHz, continues or pulsed	N_x = ÷32 N_S = ÷16 Φ_{WIDE} = 49, Φ_{FINE} = 0 Φ_{ANLG} = 110b

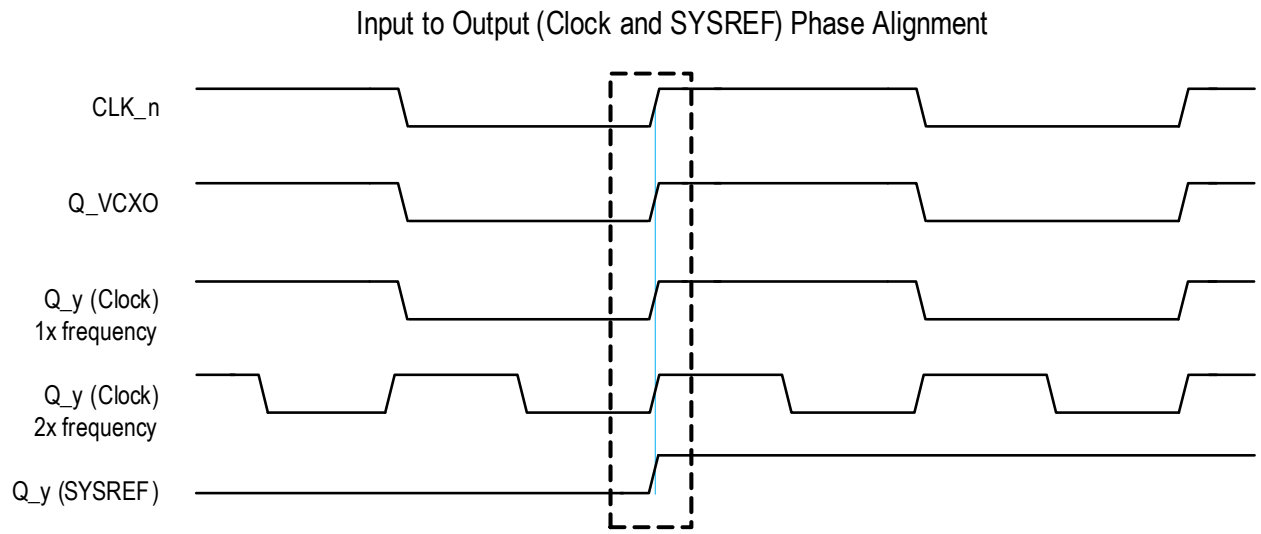


Figure 13. Input-to-Output Phase Alignment

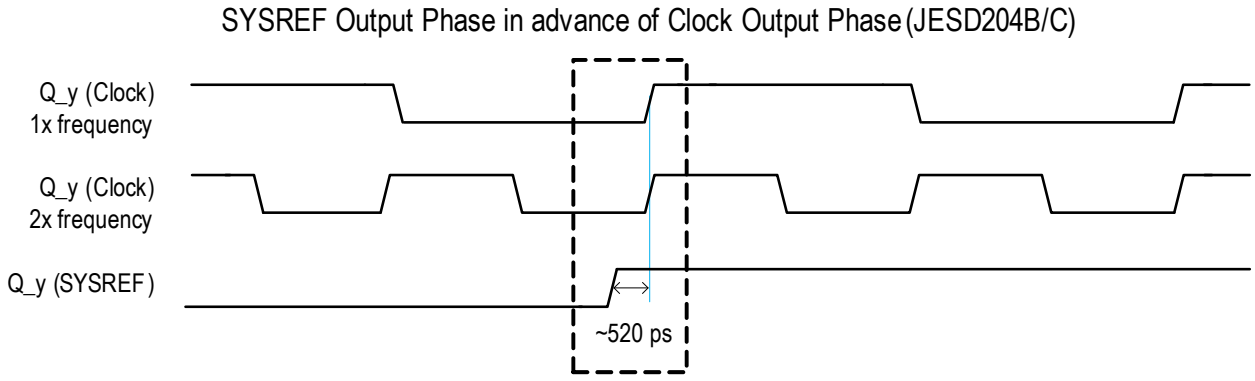


Figure 14. Output Phase Alignment for JESD204B/C

4.7 General Purpose Input/Outputs (GPIO_[1:0])

The GPIOs are intended to provide the user with a flexible method to manage the control and status of the part via pins without providing dedicated pins for each possible function of the device. Each GPIO pin (GPIO_0, GPIO_1) can be individually configured to operate in one of the following modes:

- General Purpose Input – The GPIO pin will act as an input whose logic level controls a specific function of the device.
- General Purpose Output – The GPIO pin will act as an output that is driven by an internal register state or output of a specific function.

GPIO pins, in the role of a status indicator, have the same polarity as the corresponding register status bit. The GPIO_POL register bit, when set to 1, inverts the GPIO output state for both GPIO_0 and GPIO_1 pins configured as output. A GPIO input replaces its corresponding register bit or function. For example, if a GPIO pin is configured as PLL-0 Force Holdover, the internal control bit FCV0 has no function.

If the GPIO pins are configured to “Manual input clock selection”, the GPIO pins take precedence over the clock input selection by the nM/A[1:0] register bits. If the GPIO_0 and GPIO_1 pins are configured to the same input function with conflicting GPIO_0, GPIO_1 states, the behavior will be undefined.

4.7.1 GPIO Pin Configuration

GPIO pins are all powered off a separate voltage supply that supports 1.8V operation.

Table 22. GPIO Register Functions

Register	GPIO_0 and GPIO_1 Pins		
GPIO[7:4], GPIO[3:0][1]	**Role**	**Function**	**Description**
0000	Reserved		
0001	Input	PLL-0 Force Holdover	0 = PLL-0 attempts to lock to the selected reference 1 = Forces the device into holdover state
0010	Input	PLL-0 Control Voltage Force	0 = PLL-0 attempts to lock or is locked, PLL-0 control voltage is “free”. 1 = Forces the control voltage of PLL-0 to V_{DDC33_V} / 2, will unlock PLL-0
0011-0110	Reserved		
GPIO[3:0] = 0111[2] GPIO[7:4] = xxxx	Input	Manual input clock selection	The GPIO_[1:0] pins specify the clock input to select in manual mode 00 = CLK_0 01 = CLK_1 10 = Reserved 11 = Reserved
1000	Output	PLL-0 lock detect	0 = PLL-0 is not locked 1 = PLL-0 is locked
1001	Output	PLL-1 lock detect	0 = PLL-1 is not locked 1 = PLL-1 is locked
1010	Output	PLL-0 and PLL-1 lock detect	0 = PLL-0 or PLL-0 is not locked 1 = PLL-0 and PLL-1 are both locked
1011	Output	Input Activity Alarm	0 = An input activity monitor alarm (LOS) occurred on any enabled CLK_n input. Input enable/disable is controlled by DIS_CLKn. 1 = No input activity alarm

Table 22. GPIO Register Functions (Cont.)

Register	GPIO_0 and GPIO_1 Pins		
GPIO[7:4], GPIO[3:0][1]	**Role**	**Function**	**Description**
1100	Output	Holdover State	0 = The device is in the holdover state 1 = No holdover state
1101	Output	Interrupt	0 = No interrupt occurred 1 = Any of the non-masked status bit has change state to “set” indicating an alarm condition
1110	Reserved		
GPIO[3:0] = 1111[3] GPIO[7:4] = xxxx	Output	Selected clock	The GPIO_[1:0] pins indicate the currently selected clock signal 00 = CLK_0 01 = CLK_1 10 = Reserved 11 = Reserved

1. GPIO[7:4] defines the function of the GPIO_1 pin; GPIO[3:0] defines the function of the GPIO_0 pin.
2. GPIO[3:0] = 0111 configures *both* GPIO pins to manual clock selection inputs. The state of GPIO[7:4] does not matter.
3. GPIO[3:0] = 1111 configures *both* GPIO pins to clock selection status outputs. The state of GPIO[7:4] does not matter.

4.7.2 GPIO Pin Configuration at Startup

Both GPIO pins are sampled at the rising edge of the internal reset signal and are used in setting the initial configuration. Table 23 shows which pins are used to control what aspects of the initial configuration. All of these register settings can be over-written later via serial port accesses.

Table 23. GPIO_0 Pin Configuration At Startup

Register Default	GPIO_0	
	Role	**Function**
GPIO[3:0] = 1011	Output	Input activity alarm

Table 24. GPIO_1 Pin Configuration At Startup

Register Default	GPIO_1	
	Role	**Function**
GPIO[7:4] = 1010	Output	PLL-0 and PLL-1 lock detect

4.8 Status Conditions and Interrupts

The device has an interrupt output to signal changes in status conditions. Settings for status conditions can be accessed in the Status registers. The device has several conditions that can indicate faults and status changes in the operation of the device. These are shown in Table 25 and can be monitored directly in the status registers. Status bits (named: ST_*condition*) are read-only and reflect the momentary device status at the time of read-access. Several status bits are also copied into latched bit positions (named: LS_*condition*). The latched version is controlled by the corresponding fault and status conditions and remains set (“sticky”) until reset by the user by writing 1 to the status register bit.

The reset of the status condition has an effect only if the corresponding fault condition is removed; otherwise, the status bit will set again. Setting a status bit on several latched registers can be programmed to generate an interrupt signal via settings in the Interrupt Enable bits (named: INTEN_*condition*). A setting of 0 in any of these bits will mask the corresponding latched status bit from affecting the GPIO configured as an interrupt pin. Setting

all INTEN_*condition* bits to 0 has the effect of disabling interrupts from the device. Interrupts are cleared by resetting the appropriate bit(s) in the latched register after the underlying fault condition has been resolved. When all valid interrupt sources have been cleared in this manner, this will release the GPIO output until the next unmasked fault.

Table 25. Status Bit Functions

Status Bit		Function				
			Status if Bit is:		Interrupt signal on selected GPIO	
Momentary	Latched	Description	1	0	Enable Bit Name	Reporting
ST_CLK0	LS_CLK0	CLK 0 input loss of signal	Active	Loss of signal (LOS)	INTEN_CLK0	1 = Loss of CLK0
ST_CLK1	LS_CLK1	CLK 1 input loss of signal			INTEN_CLK1	1 = Loss of CLK1
ST_CLK2	LS_CLK2	CLK 2 input loss of signal			INTEN_CLK2	1 = Loss of CLK2
ST_CLK3	LS_CLK3	CLK 3 input loss of signal			INTEN_CLK3	1 = Loss of CLK3
ST_PLL0_LOCK	LS_PLL0_LOCK	PLL-0 lock state	Locked	Loss of lock (LOL)	INTEN_PLL0_LOCK	1 = PLL-0 Loss of lock
ST_PLL1_LOCK	LS_PLL1_LOCK	PLL-1 lock state			INTEN_PLL1_LOCK	1 = PLL-1 Loss of lock
ST_PLL0_HOLD	LS_PLL0_HOLD	Holdover	PLL-0 not in holdover	PLL-0 in holdover	INTEN_PLL0_HOLD	1 = PLL-0 went into holdover
ST_PLL0_REF	LS_PLL0_REF	PLL-0 reference status	Valid reference	Reference lost[1]	INTEN_PLL0_REF	1 = Selected input lost reference
—	LS_HOLD_DAC[14:0]	PLL-0 Holdover value	Binary Coding		—	—
ST_BIT_D0[8:0]	—	PLL-1 Band Selection	Binary Coding		—	—
ST_REF[1:0]	—	Clock input selection	00 = CLK_0 01 = CLK_1 10 = Reserved 11 = Reserved		—	—
ST_FCV0	—	Status of forced mid for PLL-0	Forced to mid level	Normal PLL lock	—	—
ST_RCOSC_INITCLK	—	Completion of output divider synchronization	Not completed	Completed	—	—

1. “Manual” mode: 0 indicates if the reference selected by SEL[1:0] is lost.
   “Automatic (no holdover)” mode: 0 indicates if all reference clocks are lost or inactive (by DIS_CLKn bit).
   “Short-term holdover” and Automatic with holdover” modes: 0 indicates the reference is lost and still in holdover.

4.9 Power-Down Features

Applications now using all functional blocks of the device can use power-down settings to reduce power consumption and to minimize on-chip crosstalk (see Table 26).

Table 26. Power-Down Settings

Operation/Block	Power-Down Setting	
Unused outputs	Set PD_y = 1 and PD_SYSREF_y = 1	Individual output power down, channel remains powered up
Unused output channel	Set PD_x = 1	Channel with all associated outputs, frequency divider, and delay circuits is powered down (overwrites PD_y = 1, PD_SYSREF_y setting)
Output channel used as clock output	Set PD_SYSREF_y = 1	Power down SYSREF signal path and associated Φ_{FINE} and Φ_{ANLG} delay circuits
Unused Q_VCXO output	Set PD_Q_VCXO	Q_VCXO output power down
Unused input	Set DIS_CLKn	Disable individual, unused inputs
Dual PLL mode, internal VCO	Set PD_M1 = 1	If FBSEL_PLL_0 = 0 and no input monitoring (LOS) is used, M_1 can be powered down
Dual PLL mode	Set PD_M1 = 1	If FBSEL_PLL_0 = 0 and no input monitoring (LOS) is used, M_1 can be powered down
Single PLL mode (PLL-0 only)	Set PD_M1 = 1 Set PD_M2 = 1	If no input monitoring (LOS) is used, M_1 can be powered down
Single PLL mode (PLL-1 only)	Set PD_M0 = 1 Set PD_M1 = 1	If no input monitoring (LOS) is used, M_1 can be powered down
PLL bypass mode	Set PD_M0 = 1 Set PD_M1 = 1 Set PD_M2 = 1	
SYSREF operation when not actively generating SYSREF signals	PD_x (of SYSREF channels) PD_SYSREF_y	Applicable to the channels generating SYSREF signals

4.10 Device Startup, Reset, and Synchronization

At startup, an internal POR (power-on reset) resets the device and sets all register bits to its default value. The device forces the VCXO control voltage at the ICP_0 pin to half of the power supply voltage (about 50% of VDD33_CP0) to center the VCXO-frequency. Clear the FCV0 register bit in or release the VCXO-PLL and it will attempt lock to the input frequency.

In the default configuration the Q_y outputs are disabled at startup.

4.10.1 Recommended Configuration Sequence (In Order)

1. (Optional) Set the values of the CPOL, LSBIT_1ST, SDO_ACT, and ASC_ON register bits to define the SPI read mode, bit order, and the SPI 3/4-wire mode. If no bits are set, the device will be in 3-wire mode, data output on falling SCLK edge, bit order is MSB first, and addresses are auto-incremented.
2. Configure all PLL settings, output divider, and delay circuits as well as other device configurations.
   a. FBSEL_PLL_0, BYP_0, FD_1, SRC and (optional) P2_SEL for the desired PLL operation mode and configure the PLL and input dividers RN, P_0, M_0, M_1, M_2, and P_1 as required to achieve PLL lock on both PLLs.
   b. Charge pump currents and control bits for both PLLs (I_CP0/1_PD, I_CP0/1_SINK_EN, I_CP0/1, CP0_POL, FCV0, and I_CP0/1_OFFSET).

c. (Optional) CP[0,1]_OFFSET for PLL static phase offset.

d. LOCK_TH and LOCK_GOOD_COUNT[1:0] for the desired PLL-0 lock characteristics.

e. nC/S_SEL_*x*, EXT_VCO_SEL_*y* for the channel operation and the dividers N_x0, N_*x*1, N_S for output frequency generation incl. SYSREF.

f. Output features such as the desired output amplitude, style, power-down state, BIAS_TYPE_x and nBIAS_x for SYSREF outputs

g. Desired input selection and monitoring modes: This involves nM/A and SEL for input selection. In any of the automatic modes, configure PRIO[1:0]_n, BLOCK_LOR, and REVS. Configure the CNTH and CNTR counters for the desired holdover characteristics and CNTV[1:0] for input revalidation if applicable to the operation mode.

h. Set the individual delay registers Φ_{FB}, Φ_{WIDE_x},Φ_{FINE_y}, and Φ_{ANLG_y} for the desired phase alignment.

i. (Optional) Configure the interrupt enable configuration bits IE_status_condition, as desired for fault reporting.

j. (Optional) Configure the desired GPIO function.

k. Additional SYSREF operation settings: SRG, SRO, and SRPC, SRWC according to the desired SYSREF operation.

3. Write a logic 1 to INIT_CLK to synchronize output dividers, then wait at least 1 ms. Do not combine steps 4 and 5 in a single SPI write cycle.
4. Write a logic 1 to RELOCK, then wait at least 1ms for PLL-1 to lock (if SRC = 00, 10, or 11, skip this step). Write logic 0 to FCV0: Release the VCXO control voltage; VCXO-PLL will attempt to lock to the input clock signal starting from its center frequency.
5. Clear the status flags.
6. Enable the outputs as desired by accessing the output-enable registers.
7. (Optional) For SYSREF pulse generation, write a logic 1 to RS to enable pulse generation. Do not combine this step with step 3, 4, or 5.

4.10.2 Changing Frequency Dividers and Phase Delay Values

4.10.2.1 Clock Frequency Divider and Delay

1. (Optional) Set the values of the CPOL, LSBIT_1ST, SDO_ACT, and ASC_ON register bits to define the SPI read mode, bit order and the SPI 3/4-wire mode. If no bits are set, the device will be in 3-wire mode, data output on falling SCLK edge, bit order is MSB first and addresses are auto-incremented.
2. Re-configure all PLL settings, output divider, and delay circuits as well as other device configurations as desired.

   For any changes in a clock output channel (clock divider and delay), write a logic 1 to INIT_CLK to synchronize output dividers, then wait at least 1ms.Changing SYSREF delay does not require to set INIT_CLK.

4.10.2.2 SYSREF Frequency Divider, Delay, and Starting/Re-Starting SYSREF Pulse Sequences

SRG = 000 and SRG = 001 (EXT_SYS input buffered to SYSREF outputs)

1. Apply the external EXT_SYS signal edge.
2. To end SYSREF pulse generation, change SRG to a different configuration.

   To re-start after SYSREF has ended, set the SRG bits again and go to step 1.

SRG = 010 and SRO = 00 or 01 (externally triggered SYSREF mode)

1. Configure the desired number of pulses.
2. Write 1 to RS.

3. Apply the external EXT_SYS signal.
4. SYSREF pulses are generated until completion of number of programmed pulses.

   To re-start with the same number of pulses, go to step 3. To change the number of pulses, go to step 1).

SRG = 010 and SRO = 10 or 11 (externally triggered SYSREF mode)

1. Write 1 to RS, then apply the external EXT_SYS signal.
2. Rising (falling) EXT_SYS signal edge starts pulse generation.
3. Falling (rising) EXT_SYS signal edge stops pulse generation.

   To re-start, go to step 2.

SRG = 011 and SRO = 00 (internally triggered SYSREF mode, pulsed)

1. Configure the desired number of pulses.
2. Write 1 to RS.
3. SYSREF pulses are generated and end as configured.

   To re-start with the same number of pulses, go to step 2. To change the number of pulses, go to step 1.

SRG = 011 and SRO = 01 (internally triggered SYSREF mode, pulsed with auto-repeat)

1. Configure the desired number of pulses.
2. Write 1 to RS.
3. SYSREF pulses are generated.

   To end pulse generation, set SRG = 111.

   To re-start, set SRG = 011 and go to step 1.

SRG = 100 (continuous SYSREF mode)

1. Write 1 to RS.
2. SYSREF pulses are generated.
3. To end SYSREF pulse generation, set SRG = 111.

   To re-start after SYSREF has ended, set the SRG = 100 and go to step 1.

4.11 SPI Interface

The 8V19N882 has a configurable 3-wire/4-wire serial control port capable of responding as a slave in an SPI configuration to allow read and write access to any of the internal registers for device programming or read back. The SPI interface consists of the SCLK (clock), SDAT (serial data input and output in 3-wire mode, input in 4-wire mode), MISO (serial data output in 4-wire mode), and nCS (chip select) pins. After power-up, the SPI interface is in 3-wire mode. A data transfer consists of a direction bit, 15-bit address bits any integer multiple of 8 data bits and is always initiated by the SPI master on the bus. Internal register data is organized in SPI bytes of 8-bit each.

If nCS is at logic high, the SDAT data I/O is in high-impedance state and the SPI interface of the device is disabled.

In a write operation, data on SDAT will be clocked into the 8V19N882 on the rising edge of SCLK. In a read operation, data on SDAT / MISO will be clocked out of the 8V19N882 on the falling or rising edge of SCLK depending on the CPOL setting (CPOL = 0: output data changes on the falling edge [SPI master will capture data on the rising edge of SCLK]; CPOL = 1: output data changes on the rising edge [SPI master will capture data on the falling edge of SCLK]).

SPI 4 wire configuration: Use the register bits SDO_ACT and <SDO_ACT> to configure the interface to 4-wire if desired. On startup, the device is on 3-wire mode. In 4-wire mode, the MISO pin is designated for SPI data outputs. In 3-wire mode, SDAT is the data output (shared with data input).

Starting a data transfer requires nCS to set and hold at logic low level during the entire transfer. Setting nCS = 0 will enable the SPI interface with SDAT in data input mode. The master must initiate the first 8-bit transfer. The first bit presented by the SPI master in each transfer is the MSB (most significant bit). The first bit presented to the slave is the slave address bits A[15:1] pointing to an internal register in the address space 0 to 127, followed by the direction bit R/nW (1 = Read, 0 = Write)

Read operation from an internal register to the data output (pin SDAT in 3-wire, pin MISO in 4-wire mode): a read operation starts with a 16-bit transfer from the master to the slave: SDAT (input) is clocked on the *rising* edge of SCLK. First presented on the slave is the address, designated by bits A[15:1], pointing to and internal register in the address space 0 to 127, followed by the direction bit R/nW = 1 to indicate a read transfer. After the first 16 bits are clocked into SDAT, the register content addressed by A[15:1] are loaded into the shift register and the next 8 SCLK *falling* (CPOL=1) clock cycles will then present the loaded register data on the SPI data output and transfer these to the master. In SPI 3-wire mode, the SDAT I/O changes to output.

Transfers must be completed by de-asserting nCS after any multiple 8 SCLK cycles. If nCS is de-asserted at any other number of SCLKs, the SPI behavior is undefined. SPI byte (8 bit) and back-to-back read transfers of multiple registers are supported with an address auto-increment. During multiple transfers, nCS must stay at logic low level and SDAT will present multiple registers (A), (A+1), (A+2), etc. with each 8 SCLK cycles. During SPI Read operations, the user can continue to hold nCS low and provide further bytes of data for up to a total of 0xA7 bytes in a single block read.

Write operation to a device register: During a write transfer, a SPI master transfers one or more bytes of data into the internal registers of the device. A write transfer starts by asserting nCS to low logic level. The first bit presented by the master must set the direction bit R/nW to 0 (Write) and the 15 address bits A[1:15] must contain the 15-bit register address. Bits D0 to D7 contain 8 bits of payload data, which is written into the register addressed by A[1:15] at the end of an 8-bit write transfer. Multiple, subsequent register transfers from the master to the slave are supported by holding nCS asserted at logic low level during write transfers. The 15-bit register address will auto-increment. Transfers must be completed with de-asserting nCS after any multiple 8 SCLK cycles. If nCS is de-asserted at any other number of SCLKs, the SPI behavior is undefined.

End of transfer: After nCS is de-asserted to logic 1, the SPI bus is available to transfers to other slaves on the SPI bus. See also the READ diagram (Figure 15) and WRITE (Figure 16) displaying the transfer of two bytes of data from and into registers.

Registers 0xA8 to 0xFF. Registers in the address range 0xA8 to 0xFF should not be used. Do not write into any registers in the 0xA8 to 0xFF range.

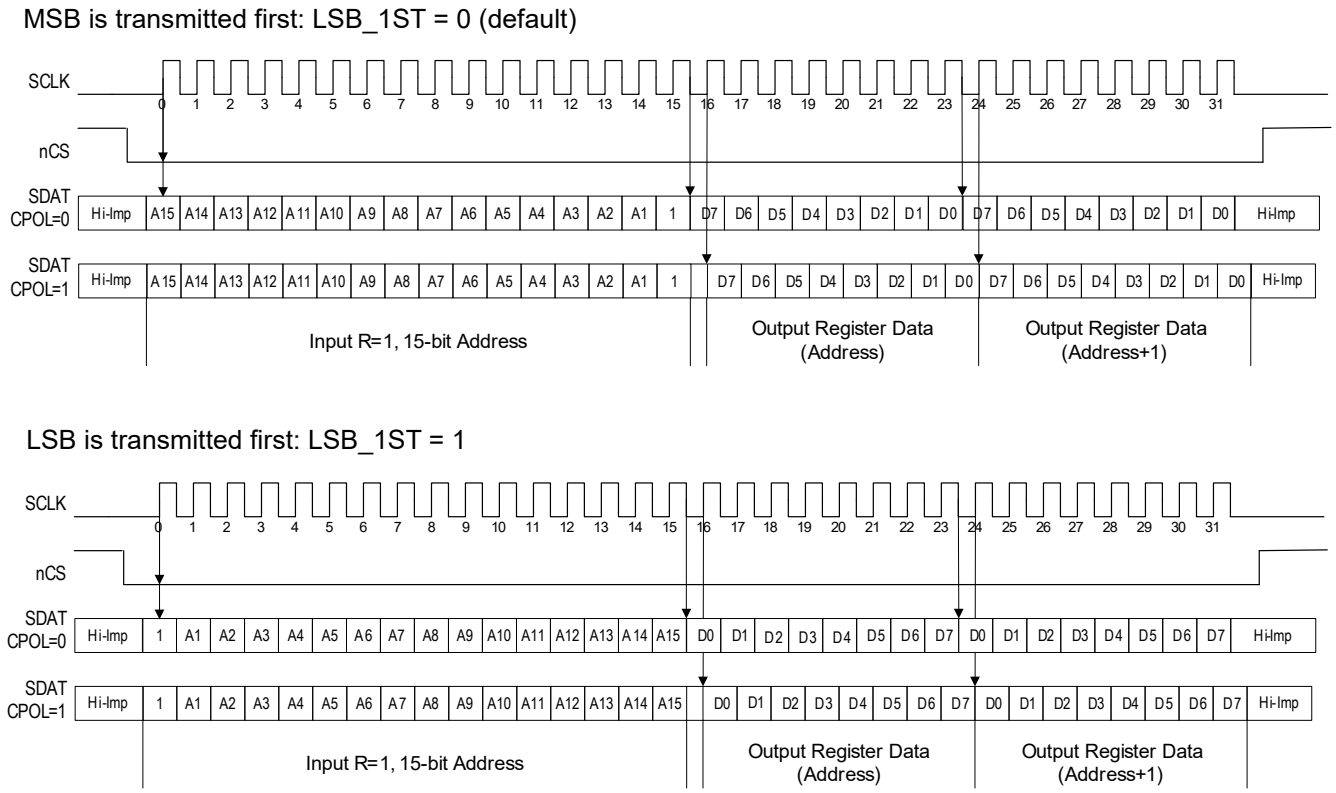


Figure 15. Logic Diagram: SPI 3-wire READ Data from Registers for CPOL = 0 and CPOL = 1

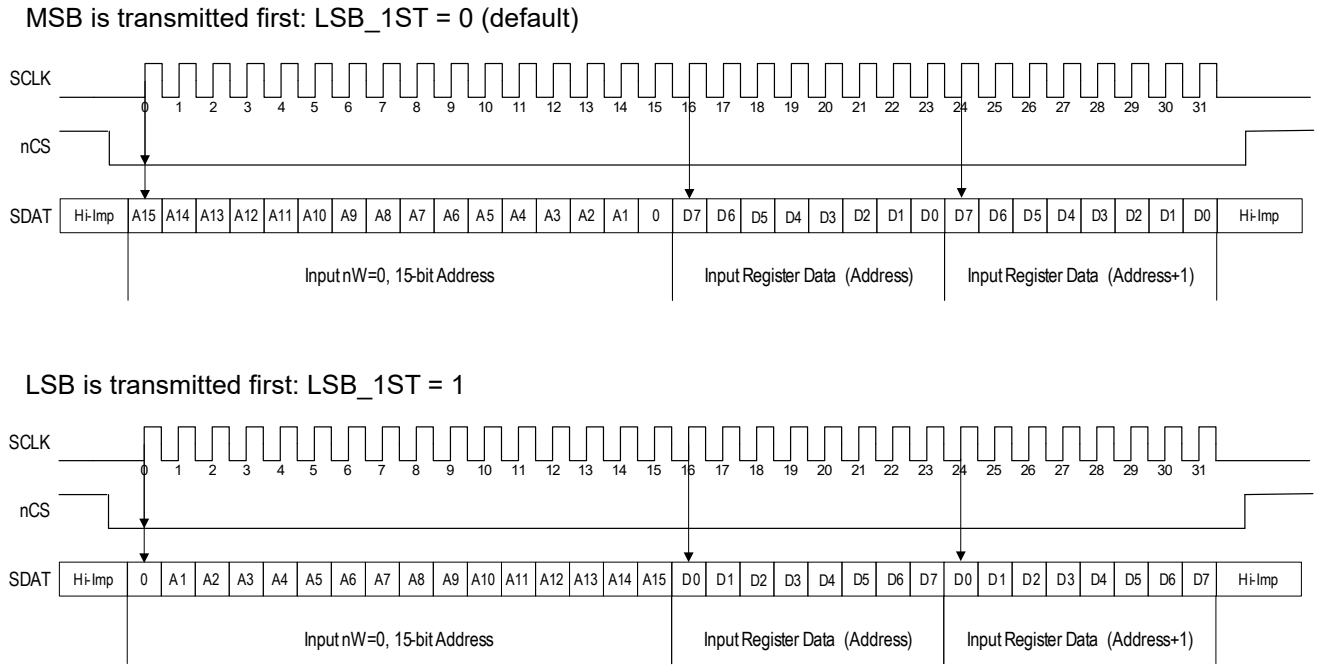


Figure 16. Logic Diagram: SPI 3/4-wire WRITE Data into Registers

Table 27. SPI Read / Write Cycle Timing Parameters

Symbol	Parameter	Test Condition	Minimum	Maximum	Unit
f_{SCLK}	SCLK frequency			20	MHz
t_{S1}	Setup time, nCS (falling) to SCLK (rising)		5		ns
t_{S2}	Setup time, SDAT (input) to SCLK (rising)		5		ns
t_{S3}	Setup time, nCS (rising) to SCLK (rising)		5		ns
t_{H1}	Hold time, SCLK (rising) to SDAT (input)		5		ns
t_{H2}	Hold time, SCLK (falling) to nCS (rising)		5		ns
t_{PD1F}	Propagation delay, SCLK (falling) to SDAT or to MISO	CPOL=0		12	ns
t_{PD1R}	Propagation delay, SCLK (rising) to SDAT or to MISO	CPOL=1		12	ns
t_{PD2}	Propagation delay, nCS to SDAT disable			12	ns

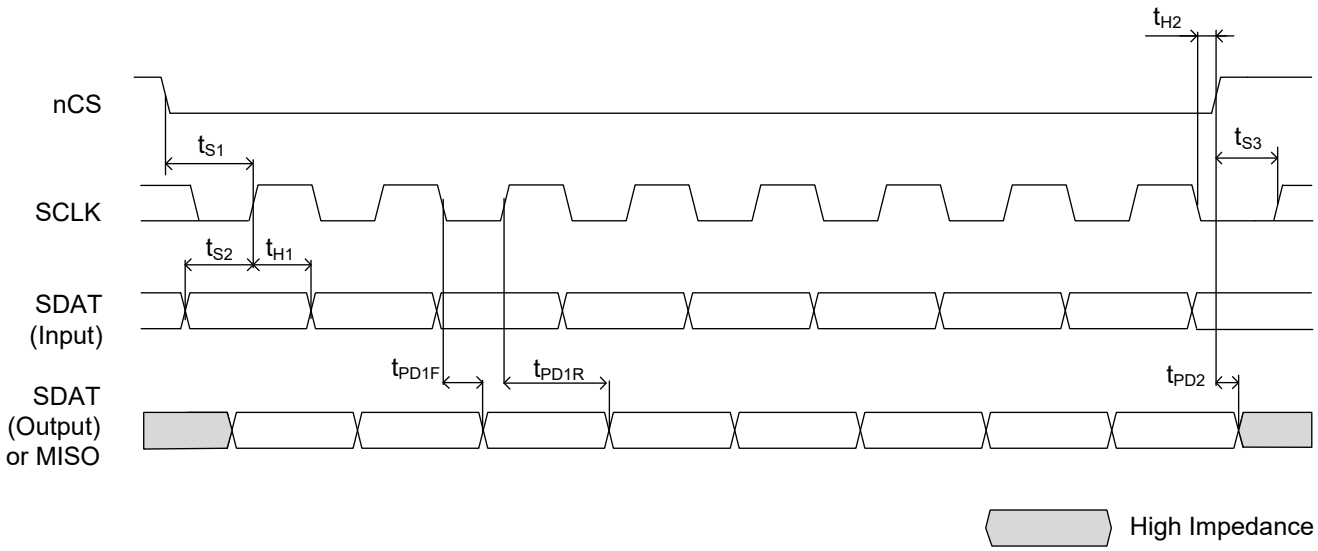


Figure 17. SPI Timing Diagram

5. Register Descriptions

5.1 Register Map

Table 28. Register Map

Register Address	Register Description
Device Configuration Registers	
0x00-0x01	SPI Configuration and Soft Reset
0x03	Device Type
0x04-0x05	Device Identifier
0x06	Device Version
0x0C-0x0D	Vendor Identifier
Input, PLL-0 Frequency Divider and Control Registers	
0x10-0x11	PLL-0 Input Divider P_0
0x12	CLK_n Input Divider R_N
0x13	PLL-0 Lock Detect Control, CLK_n Disable
0x14-0x15	PLL-0 Feedback Divider
0x16-0x17	PLL-0 Lock Detect Threshold
0x18-0x19	PLL-0/-1 Feedback Divider M_1
0x1A-0x1B	PLL-0/-1 Feedback Delay and M_1 Power Down
PLL-0 Charge Pump Control Registers	
0x1C-0x1D	PLL-0 Charge pump settings
PLL-1 Input and Bypass Control Registers	
0x20	Frequency Doubler, PLL-1 Pre-Divider
0x21	PLL-1 Bypass controls
PLL-1 Charge Pump Control Registers	
0x28-0x29	PLL-1 Charge pump settings
PLL-1 Feedback Control Registers	
0x2C	PLL-1 Feedback Divider
0x2D	M_2 Power Down, PLL-1 Feedback Divider
Reference Switching Registers	
0x34	Input switch priority
0x35	Block LOR, input switch modes, input manual select and switch control
0x36	Automatic with holdover counter period
0x37	Re-validation Count, Automatic with Holdover divide
SYSREF Control Registers	
0x38	SYSREF frequency/pulse rate divider
0x3A	SYSREF pulse wait counter SRWC
0x3B	SYSREF pulse counter SRPC
0x3D	SYSREF pulse generation control

Table 28. Register Map (Cont.)

Register Address	Register Description
Output Channel Registers	
0x40-0x43	Channel A: N_A Frequency Divider, Delay (Wide), Power Down, Clock/SYSREF Selector, Amplitude/1.8V control, BIAS_TYPE and nBIAS
0x44-0x47	Channel B: N_B Frequency Divider, Delay (Wide), Power Down, Clock/SYSREF Selector, Amplitude/1.8V control, BIAS_TYPE and nBIAS
0x48-0x4B	Channel C: N_C Frequency Divider, Delay (Wide), Power Down, Clock/SYSREF Selector, Amplitude/1.8V control, EXT_VCO_SEL
0x4C-0x4F	Channel D: N_D Frequency Divider, Delay (Wide), Power Down, Clock/SYSREF Selector, Amplitude/1.8V control, EXT_VCO_SEL
0x50-0x53	Channel E: N_E Frequency Divider, Delay (Wide), Power Down, Clock/SYSREF Selector, Amplitude/1.8V control, BIAS_TYPE and nBIAS
0x54-0x57	Channel F: N_F Frequency Divider, Delay (Wide), Power Down, Clock/SYSREF Selector, Amplitude/1.8V control, BIAS_TYPE and nBIAS
0x58-0x5B	Channel G: N_G Frequency Divider, Delay (Wide), Power Down, Clock/SYSREF Selector, Amplitude/1.8V control, BIAS_TYPE and nBIAS
0x5C-0x5F	Channel H: N_H Frequency Divider, Delay (Wide), Power Down, Clock/SYSREF Selector, Amplitude/1.8V control, BIAS_TYPE and nBIAS
Output Registers	
0x60-0x61	Output Q_A0 State: power down, LVDS/LVPECL style, amplitude, SYSREF phase
0x62-0x63	Reserved
0x64-0x65	Output Q_B0 State: power down, LVDS/LVPECL style, amplitude, SYSREF phase
0x66-0x67	Output Q_B1 State: power down, LVDS/LVPECL style, amplitude, SYSREF phase
0x68-0x69	Output Q_C0 State: power down, amplitude, SYSREF phase
0x6A-0x6B	Output Q_C1 State: power down, amplitude, SYSREF phase
0x6C-0x6D	Output Q_D0 State: power down, amplitude, SYSREF phase
0x6E-0x6F	Output Q_D1 State: power down, amplitude, SYSREF phase
0x70-0x71	Output Q_E0 State: power down, LVDS/LVPECL style, amplitude, SYSREF phase
0x72-0x73	Output Q_E1 State: power down, LVDS/LVPECL style, amplitude, SYSREF phase
0x74-0x75	Output Q_E2 State: power down, LVDS/LVPECL style, amplitude, SYSREF phase
0x76-0x77	Output Q_F0 State: power down, LVDS/LVPECL style, amplitude, SYSREF phase
0x78-0x79	Output Q_F1 State: power down, LVDS/LVPECL style, amplitude, SYSREF phase
0x7A-0x7B	Output Q_G0 State: power down, LVDS/LVPECL style, amplitude, SYSREF phase
0x7C-0x7D	Reserved
0x7E-0x7F	Output Q_H0: power down, LVDS/LVPECL style, amplitude, SYSREF phase
0x80-0x81	Output Q_H1: power down, LVDS/LVPECL style, amplitude, SYSREF phase
0x82-0x83	Output Q_H2: power down, LVDS/LVPECL style, amplitude, SYSREF phase
0x84	Output Q_VCXO power down, LVDS/LVPECL style
GPIO and Status Registers	
0x88	GPIO control
0x89	GPIO output signal polarity

Table 28. Register Map (Cont.)

Register Address	Register Description
Output Enable Registers	
0x8C	Interrupt enable control
Output Enable Registers	
0x90-0x92	Latch status bits
0x94-0x97	Momentary status bits
Synchronization Control Registers	
0x98-0x99, 0x9B	Synchronization bits
0x9C-0x9E	Output Enable
0xA8-0xFF	Reserved. Do not write into this register address range

5.2 Register Descriptions

This section contains all addressable registers, sorted by function, followed for a detailed description of each bit field for each register. Several functional blocks with multiple instances in this device have individual registers controlling their settings, but since the registers have an identical format and bit meaning, they are described only once, with an additional table to indicate their addresses and default values. All writable register fields will start up with default values as indicated in the (Factory) Default column unless altered by values loaded from non-volatile storage during the initialization sequence.

Fixed read-only bits will have defaults as indicated in their specific register descriptions. Read-only status bits will reflect valid status of the conditions they are designed to monitor once the internal power-up reset has been released. Unused registers and bit positions are Reserved. Reserved bit fields may be used for internal debug test and debug functions.

Note: All default values in the register tables are binary.

5.2.1 Device Configuration Registers

Table 29. Device Configuration Register Bit Field Locations

Register Address	Bit Field Location							
	D7	D6	D5	D4	D3	D2	D1	D0
0x00	SRESET	LSBIT_1ST	ACS_ON	SDO_ACT	<SDO_ACT>	<ACS_ON>	<LSBIT_1ST>	<SRESET>
0x01	Reserved							CPOL
0x03	DEV_TYPE[7:0]							
0x04	DEV_ID[7:0]							
0x05	DEV_ID[15:8]							
0x06	DEV_VER[7:0]							
0x0C	VENDOR_ID[7:0]							
0x0D	VENDOR_ID[15:8]							

Table 30. Device Configuration Register Descriptions

Register Description			
Bit Field	**Field Type**	**Default**	**Description**
SRESET <SRESET>	R/W Auto-Clear	0 Value: not reset	Soft Reset: 0 = Normal operation. 1 = Register reset. The device loads the default values into the registers 0x02-0xA7. The content of the register addresses 0x00 and 0x01 and the SPI engine are not reset. SRESET bit D7 is mirrored with <SRESET> in bit position D0. Register reset requires to set both SRESET and <SRESET> bits.
LSBIT_1ST <LSBIT_1ST>	R/W	0 Value: MSB first	Least Significant Bit Position: Defines the bit transmitted first in SPI transfers between slave and master. 0 = The most significant bit (D7) first 1 = The least significant bit (D0) first LSBIT_1ST bit D6 is mirrored with <LSBIT_1ST> in bit position D1. Changing LSBIT_1ST to most significant bit requires to set both LSBIT_1ST and <LSBIT_1ST> bits.
ASC_ON <ASC_ON>	R/W	1 Value: on, addresses auto-increment	Address Ascend on: 0 = Address ascend is off (addresses auto-decrement in streaming SPI mode) 1 = Address ascend is on (addresses auto-increment in streaming SPI mode) The ASC_ON bit specifies whether addresses are incremented or decremented in streaming SPI transfers. ASC_ON bit D5 is mirrored with <ASC_ON> in bit position D2. Changing ASC_ON to “ON” requires to set both ASC_ON and <ASC_ON> bits.
SDO_ACT <SDO_ACT>	R/W	0 Value: SPI-3-wire mode	SPI 3/4 Wire Mode: Selects the unidirectional or bidirectional data transfer mode for the SDAT pin. 0 = SPI 3-wire mode: • SDAT is the SPI bidirectional data I/O pin • MISO pin is not used and is in static low state 1 = SPI 4-wire mode • SDAT is the SPI data input pin • MISO is the SPI data output pin SDO_ACT bit D4 is mirrored with <SDO_ACTIVE> in bit position D3. Changing SDO_ACT to SPI 4-wire mode requires to set both SDO_ACT and <SDO_ACT> bits.
CPOL	R/W	0 Value: data output at falling SCLK edge	SPI Read Operation SCLK Polarity: 0 = Data bits on SDAT are output at the falling edge of SCLK edge (SPI master will capture data on the rising edge of SCLK) 1 = Data bits on SDAT are output at the rising edge of SCLK edge (SPI master will capture data on the falling edge of SCLK)
DEV_TYP[7:0]	R only	0000 0110 Value: RF-PLL	Device (Chip) Type: Reads 0x06 (RF-PLL) after power-up and reset.
DEV_ID[15:0]	R only	0x04: 0100 1000 0x05: 0000 0000 Value: 0x0048	Device Identifier: Device is composed of registers 0x04 (low byte) and register 0x08 (high byte). Reads 0x0048 after power-up and reset.

Table 30. Device Configuration Register Descriptions (Cont.)

Register Description			
Bit Field	**Field Type**	**Default**	**Description**
DEV_VER[7:0]	R only	0000 1011 Value: 0x0B	Device Version: Reads the device version 0x0B after power-up and reset.
VENDOR_ID	R only	0x0C: 0010 0110 0x0D: 0000 0100 Value: 0x0426	Vendor Identifier: 0x0426 (Integrated Device Technology, IDT/Renesas). Reads 0x0426 (IDT/Renesas) after power-up and reset.

5.2.2 Input, PLL-0 Frequency Divider and Control Registers

Table 31. Input, PLL-0 Frequency Divider, and Control Register Bit Field Locations

Register Address	Bit Field Location							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0x10	P0[7:0]							
0x11	Reserved	P0[14:8]						
0x12	Reserved				R1[1:0]		R0[1:0]	
0x13	Reserved		LOCK_GOOD_COUNT[1:0]		Set to 1	Set to 1	DIS_CLK1	DIS_CLK0
0x14	M0[7:0]							
0x15	PD_M0	M0[14:8]						
0x16	LOCK_TH[7:0]							
0x17	Reserved	LOCK_TH[14:8]						
0x18	M1[7:0]							
0x19	FBSEL_PLL0	Reserved	M1[13:8]					
0x1A	ΦFB[7:0]							
0x1B	PD_M1	Reserved			ΦFB[11:8]			

Table 32. Input, PLL-0 Frequency Divider and Control Register Descriptions

Register Description			
Bit Field	**Field Type**	**Default**	**Description**
P0[14:0]	R/W	000 0010 0000 0000 Value: ÷512	PLL-0 Input Frequency Pre-Divider Register: The value of the frequency divider P_0 (binary coding) Range: ÷1 to ÷32,767.
Rn[1:0]	R/W	00 Value for Rn: ÷1	Input Frequency Divider for inputs CLK*n* (n = 0 to 1) Use ÷1 if the input frequency at the CLK*n* input is less than 250MHz, otherwise, use a higher divider value to scale the frequency into the P_0 divider to ≤ 250MHz. 00 = ÷1 01 = ÷2 10 = ÷4 11 = ÷8

Table 32. Input, PLL-0 Frequency Divider and Control Register Descriptions (Cont.)

Register Description				
Bit Field	**Field Type**	**Default**	**Description**	
LOCK_GOOD_COUNT[1:0]	R/W	00	PLL-0 Lock indicator counter. The device reports PLL-0 lock when the phase difference between both signals into the phase detector PLL-0 is lower than or equal to the phase difference set by LOCK_TH[14:0] for more than the number of clock cycles (of the M_0 divider output) set in this register. 00 = 10,000 clock cycles (default) 01 = 100,000 clock cycles 10 = 1,000,000 clock cycles 11 = 10,000,000 clock cycles	
DIS_CLK*n*	R/W	0 Value: Enabled	Input Disable for inputs CLK*n* (n=0 to 1) Set to 1 to disable any CLK*n* input, applicable for cases where inputs are not connected. 0 = Input CLK*n* and the associated clock input Divider Rn is enabled 1 = Input CLK*n* and the associated clock input Divider Rn is disabled	
M0[14:0]	R/W	000 0010 0000 0000 Value: ÷512	PLL-0 Feedback Divider: The value of the frequency divider M_0 (binary coding). Range: ÷1 to ÷32,767. The input frequency to the M_0 divider (output frequency of the FBSEL_PLL_0 multiplexer) must not exceed 250MHz.	
PD_M0	R/W	0 (M0 Power up)	PLL-0 Feedback divider M_0 power down state 0 = M_0 is powered up 1 = M_0 is powered down	
LOCK_TH[14:0]	R/W	000 0001 0000 0000 Value: 256	PLL-0 Lock Detect Phase Window Threshold: The device reports PLL-0 lock when the phase difference between both signals into the phase detector PLL-0 is lower than or equal to the phase difference set by LOCK_TH[14:0] for more than the number of clock cycles (of the M_0 divider output) set in LOCK_GOOD_COUNT. Requires $M_0 \geq 4$. Set LOCK_TH[14:0] < ($M_0 \div 2$). PLL-0 phase detector frequencies are: ▪ $f_{CLK} \div (Rn \times P_0)$ ▪ $f_{VCXO} \div (M_0$ [× 2 if P3_SEL = 1]) is the internal output of the M_0 divider	
M1[13:0]	R/W	00 0000 001 1 0010 Value = ÷50	PLL-0/-1 Feedback-Divider. The value of the frequency divider (binary coding) Range: ÷1 to ÷16,383 If the input frequency to M_1 is > 1GHz, use M_1 settings of ÷8 and higher.	
FBSEL_PLL0	R/W	1 Value: PLL-0 feedback through $M_1 \times M_0$ dividers	Feedback path selector for PLL-0. Controls the routing of the PLL-0 feedback path applicable to dual PLL mode. FBSEL_PLL0 = 0	FBSEL_PLL0 = 1 (preferred)
			Independent PLL feedback: PLL-0 feedback path through the M_0 divider (and through an additional ÷2 if P3_SEL = 1).	Preferred feedback configuration for achieving deterministic delay from input to the outputs. PLL-0 feedback path through the $M_1 \times M_0$ dividers.

Table 32. Input, PLL-0 Frequency Divider and Control Register Descriptions (Cont.)

Register Description			
Bit Field	**Field Type**	**Default**	**Description**
ΦFB[11:0]	R/W	0000 0000 0000 Value: 0ns	PLL feedback phase delay. Inserts the specified phase delay to achieve an input-to-output phase alignment in dual PLL mode. ΦFB[11:0]
			PLL Feedback Phase Delay in ps = ΦFB × 254ps (4096 steps) 0000 0000 0000 = 0ns … 1111 1111 1111 = 1,041.41ns
PD_M1	R/W	0	PLL-0/PLL-1 feedback divider M_1 power down state 0 = Feedback divider M1 is powered up. 1 = Feedback divider M1 is powered down PD_M1 must be set to 0 (power up) for using the device function: input monitoring.

5.2.3 PLL-0 Charge Pump Control Registers

Table 33. PLL-0 Charge Pump Control Register Bit Field Locations

Register Address	Bit Field Location							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0x1C	I_CP0_PD	Reserved	I_CP0_SINK_EN	I_CP0_X2	I_CP0[3:0]			
0x1D	CP0_POL	FCV0	I_CP0_OFFSET[5:0]					

Table 34. PLL-0 Charge Pump Control Register Descriptions

Register Description				
Bit Field	**Field Type**	**Default**	**Description**	
I_CP0_PD	R/W	0 Value: Power up	PLL-0 Charge pump power state 0 = Power up 1 = Power down and disabled	
I_CP0_SINK_EN	R/W	1 Value: Enabled	PLL-0 Enable charge pump sink current 0 = Disabled 1 = Enabled sink current, sink and source currents are equal	
I_CP0_X2	R/W	1	PLL-0 Charge pump current multiplier. 0 = 1x (100µA current steps for I_CP0[3:0]) 1 = 2x (200µA current steps for I_CP0[3:0])	
I_CP0[3:0]	R/W	0000 Value: 1.6mA	PLL-0 Charge pump gain control. Sets the PLL-0 charge pump current. Current is programmable up to 3mA in 100(200)µA steps depending on the I_CP0_X2 bit setting.	
			I_CP0_X2 = 0 100µA steps	I_CP0_X2 = 1 200µA steps
			PLL-0 charge pump current: I_CP0 = I_CP0[3] × 800µA + I_CP0[2] × 400µA + I_CP0[1] × 200µA + I_CP0[0] × 100µA.	PLL-0 charge pump current: I_CP0 = 1600µA + I_CP0[2] × 800µA + I_CP0[1] × 400µA + I_CP0[0] × 200µA.

Table 34. PLL-0 Charge Pump Control Register Descriptions (Cont.)

Register Description			
Bit Field	**Field Type**	**Default**	**Description**
CP0_POL	R/W	0	PLL-0 control voltage polarity 0 = Positive (use with VCXOs that have a positive control voltage curve) 1 = Negative (use with VCXOs that have a negative control voltage curve)
FCV0	R/W	1 Value: ICP_0 voltage is set to 50% of	PLL-0 Force ICP_0 control voltage 0 = Normal operation (PLL-0 can lock) 1 = Forces the voltage at the ICP_0 pin (VCXO control voltage) to 50% of VDD33_CP0. PLL-0 unlocks and the VCXO is forced to its mid-point frequency. FCV0 = 1 is the default setting at startup to center the VCXO frequency. FCV0 must be cleared after startup to enable the PLL to lock to the reference frequency.
I_CP0_OFFSET[5:0]	R/W	00 0000	CP0 (Charge pump of PLL-0) programmable charge pump offset output current. I_CP0_OFFSET is an additive current applied to the ICP_0 output effectively introducing a phase offset into PLL-0. Use I_CP0_OFFSET to improve charge pump linearity and PLL-0 phase noise. Programmable in 12.5µA steps, range is 0µA to 487.5µA. I_CP0_OFFSET = I_CP0_OFFSET[5] × 200µA + I_CP0_OFFSET[4] × 100µA + I_CP0_OFFSET[3] × 100µA + I_CP0_OFFSET[2] × 50µA + I_CP0_OFFSET[1] × 25µA + I_CP0_OFFSET[0] × 12.5µA

5.2.4 PLL-1 Input and Bypass Control Registers

Table 35. PLL-1 Input and Bypass Control Register Bit Field Locations

Register Address	Bit Field Location							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0x20	FD_1	P1[6:0]						
0x21	P3_SEL	P2_SEL	SRC[1:0]		BYP_0	Reserved		

Table 36. PLL-1 Frequency Divider and Control Register Descriptions

Register Description			
Bit Field	**Field Type**	**Default**	**Description**
FD_1	R/W	0	The input frequency of PLL-1 (2nd stage) is: 0 = The output signal of the BYP_0 multiplexer, divided by the P_1 divider. 1 = The output signal of the BYP_0 multiplexer, doubled in frequency. Use this setting to improve phase nose. The P_1 divider has no effect if FD_1 = 1.
P1[6:0]	R/W	000 0001 Value: ÷1	PLL-1 Pre-Divider: The value of the frequency divider (binary coding). Range: ÷1 to ÷127. 000 0001 = P_1 is bypassed
P3_SEL	R/W	1 Value: ÷2	PLL-0 Feedback Frequency Limiting Divider Select. Set to 1 (selects a ÷2 divider) if the VCXO frequency is > 250MHz 0 = Ext. VCXO frequencies is ≤ 250MHz. PLL-0 feedback is M_0 1 = Ext. VCXO frequency is > 250MHz. The VCXO-frequency is pre-divided by ÷2 before the M_0 divider. The total PLL-0 feedback is 2 × M_0.
P2_SEL	R/W	0 Value: ÷1	External VCO Frequency Limiting Divider Select. Set to 1 (selects a ÷2 divider) if the external VCO frequency is > 4000MHz. 0 = Ext. VCO frequency is ≤ 4000MHz. 1 = Ext VCO components > 4000MHz. External VCO frequency is divided by 2.

Table 36. PLL-1 Frequency Divider and Control Register Descriptions (Cont.)

Register Description			
Bit Field	**Field Type**	**Default**	**Description**
SRC[1:0]	R/W	01 Value: PLL-1	Output Channel Source Selector 00 = External VCO 01 = Internal PLL-1 10 = Internal PLL-0 11 = Selected CLK*n* input (when BYP_0 = 1)
BYP_0		0 Value = Dual PLL Mode	PLL Frequency Generation Mode 0 = Dual PLL Mode 1 = Frequency Synthesizer Mode (PLL-0 is bypassed)

5.2.5 PLL-1 Charge Pump Control Registers

Table 37. PLL-1 Charge Pump Control Register Bit Field Locations

Register Address	Bit Field Location							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0x28	I_CP1_PD	Reserved	I_CP1_SINK_EN	I_CP1_X2	I_CP1[3:0]			
0x29	Reserved	Reserved	I_CP1_OFFSET[5:0]					

Table 38. PLL-1 Frequency Divider and Control Register Descriptions

Register Description			
Bit Field	**Field Type**	**Default**	**Description**
I_CP1_PD	R/W	0 Value: Power up	PLL-1 Charge pump power state 0 = Power up 1 = Power down and disabled
I_CP1_SINK_EN	R/W	1 Value: Enabled	PLL-1 Enable charge pump sink current 0 = Disabled 1 = Enabled sink current; sink and source currents are equal
I_CP1_X2	R/W	1	PLL-0 Charge pump current multiplier. 0 = 1x (100µA current steps for I_CP1[3:0]) 1 = 2x (200µA current steps for I_CP1[3:0])

Table 38. PLL-1 Frequency Divider and Control Register Descriptions (Cont.)

Register Description				
Bit Field	**Field Type**	**Default**	**Description**	
I_CP1[3:0]	R/W	0000 Value: 1.6mA	PLL-1 Charge pump gain control. Sets the PLL-1 charge pump current. Current is programmable up to 3mA in 100(200)µA steps depending on the I_CP1_X2 bit setting.	
			I_CP1_X2 = 0 100µA steps	I_CP1_X2 = 1 200µA steps
			PLL-1 charge pump current: I_CP1 = I_CP1[3] × 800µA + I_CP1[2] × 400µA + I_CP1[1] × 200µA + I_CP1[0] × 100µA.	PLL-1 charge pump current: I_CP1 = 1600µA + I_CP1[2] × 800µA + I_CP1[1] × 400µA + I_CP1[0] × 200µA.
I_CP1_OFFSET[5:0]	R/W	00 0000	CP1 (Charge pump of PLL-1) programmable charge pump offset output current. I_CP1_OFFSET is an additive current applied to the ICP_1 output effectively introducing a phase offset into PLL-1. Use I_CP1_OFFSET to improve charge pump linearity and PLL-1 phase noise. Programmable in 12.5µA steps, range is 0µA to 487.5µA. I_CP1_OFFSET = I_CP1_OFFSET[5] × 200µA + I_CP1_OFFSET[4] × 100µA + I_CP1_OFFSET[3] × 100µA + I_CP1_OFFSET[2] × 50µA + I_CP1_OFFSET[1] × 25µA + I_CP1_OFFSET[0] × 12.5µA	

5.2.6 PLL-1 Feedback Control Registers

Table 39. PLL-1 Feedback Register Bit Field Locations

Register Address	Bit Field Location							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0x2C	M2[7:0]							
0x2D	PD_M2	Reserved	Reserved	Reserved	Reserved	Reserved	M2[9:8]	

Table 40. PLL-1 Frequency Divider and Control Register Descriptions

Register Description			
Bit Field	**Field Type**	**Default**	**Description**
M2[9:0]	R/W	00 0010 0000 Value: ÷32	PLL-1 feedback divider M_2 The value of the M_2 frequency divider (binary coding).
PD_M2	R/W	0 Value: Power up	PLL-1 feedback divider M_2 power down state 0 = PLL-1 (M_2) feedback divider is powered up. 1 = PLL-1 (M_2) feedback divider is powered down.

5.2.7 Reference Switching Registers

The content of the reference switching registers controls the input monitors and auto/manual input switching functions.

Table 41. Reference Switching Register Bit Field Locations

Register Address	Bit Field Location							
	D7	D6	D5	D4	D3	D2	D1	D0
0x34	PRIO_0[1:0]		PRIO_1[1:0]		Reserved			
0x35	Reserved	BLOCK_LOR	REVS	Reserved	nM/A[1:0]		SEL[1:0]	
0x36	CNTH[7:0]							
0x37	CNTR[1:0]		Reserved				CNTV[1:0]	

Table 42. Reference Switching Register Descriptions

Bit Field Location			
Bit Field	**Field Type**	**Default**	**Description**
PRIO_*n*[1:0]	R/W	CLK_0: 11 CLK_1: 10	Controls the auto-selection priority of the clock input CLK_*n* (*n*=0…1). If multiple inputs have equal priority, the order within that priority is from CLK_0 (highest) to CLK_1 (lowest). 00 = Priority 0 (lowest). Input is not selected by the switch logic. 01 = Priority 1 10 = Priority 2 11 = Priority 3 (highest)
BLOCK_LOR	R/W	0	Controls which event(s) set the PLL-0 lock status bits ST_PLL0_LOCK and LS_PLL0_LOCK BLOCK_LOR = 0: ▪ PLL-0 loss of lock, or ▪ Inactivity of the selected reference clock BLOCK_LOR = 1: ▪ Only PLL-0 loss of lock BLOCK_LOR = 1 will also block an loss-of-reference event from triggering a failure on the GPIO output pins (when selected).
REVS	R/W	0 Value: Disabled	Revertive Switching The revertive input switching setting is only applicable to the two automatic selection modes shown in Table 18. If nM/A[1:0] = X0, the REVS setting has no meaning. 0 = Disabled: Re-validation of a non-selected input clock has no impact on the clock selection. 1 = Enabled: Re-validation of any non-selected input clock(s) will cause an new input selection according to the pre-set input priorities (revertive switch). An input switch is only done if the re-validated input has a higher priority than the current PLL-0 reference clock. Default setting is revertive switching turned off.

Table 42. Reference Switching Register Descriptions (Cont.)

<table>
<tr><th colspan="6">Bit Field Location</th></tr>
<tr><th>Bit Field</th><th>Field Type</th><th>Default</th><th colspan="3">Description</th></tr>
<tr><td>nM/A[1:0]</td><td>R/W</td><td>00
Value: Manual Selection</td><td colspan="3">Reference Input Selection Mode.
In any of the manual selection modes (nM/A[1:0] = 00 or 10), the PLL-0 reference input is selected by SEL[1:0]. In any of the automatic selection modes, the PLL-0 reference input is selected by an internal state machine according to the input LOS states and the priorities in the input priority registers
00 = Manual selection.
01 = Automatic selection (no holdover)
10 = Short-term holdover
11 = Automatic selection with holdover
GPIO input clock selection takes precedence over the selection by the nM/A[1:0] bits.</td></tr>
<tr><td>SEL[1:0]</td><td>R/W</td><td>00
Value: CLK_0 selected</td><td colspan="3">PLL-0 Input Reference Selection
Controls the selection of the reference input in manual selection modes. In automatic selection modes (nM/A[1:0] = X1), SEL[1:0] has no meaning.
00 = CLK_0
01 = CLK_1
10 = Reserved
11 = Reserved</td></tr>
<tr><td>CNTH[7:0]</td><td>R/W</td><td>1000 0000 (value: 136ms)</td><td colspan="3">Holdover, hold-off counter period. Applicable to automatic with holdover mode, nM/A = 11.
The device initiates a clock failover switch upon counter expiration (zero transition). The counters start to counts backwards after a LOS event is detected. The hold-off counter period is determined by the binary number of PLL-0 output pulses divided by CNTR[1:0]. With a VCXO frequency of 122.88MHz and CNTR[1:0] = 10, the counter has a period of (1.066 ms × binary setting). After each zero-transition, the counter automatically re-loads to the setting in this register. The default setting is 136ms (VCXO = 122.88MHz: 1/122.88MHz × 2^{17} × 128)</td></tr>
<tr><td rowspan="6">CNTR[1:0]</td><td rowspan="6">R/W</td><td rowspan="6">00
(Value: 2^{15})</td><td colspan="4">Holdover reference divider. Applicable to automatic with holdover mode, nM/A=11.</td></tr>
<tr><td>CNTR[1:0]</td><td colspan="3">CNTH frequency (period; range)</td></tr>
<tr><td></td><td>38.4MHz VCXO P3_SEL=0</td><td>122.88MHz VCXO P3_SEL=0</td><td>245.76MHz VCXO P3_SEL=0</td><td>491.52MHz VCXO P3_SEL=1</td></tr>
<tr><td>00 = f_{VCXO} ÷ 215</td><td>1171Hz (0.853ms; 0-217.6ms)</td><td>3750Hz (0.266ms; 0-68ms)</td><td>7500Hz (0.133ms; 0-34ms)</td><td>7500Hz (0.133ms; 0-34ms)</td></tr>
<tr><td>01 = f_{VCXO} ÷ 2^{16}</td><td>585Hz (1.706ms; 0-435.2ms)</td><td>1875Hz (0.533ms; 0-136ms)</td><td>3750Hz (0.266ms; 0-68ms)</td><td>3750Hz (0.266ms; 0-68ms)</td></tr>
<tr><td>10 = f_{VCXO} ÷ 2^{17}</td><td>292Hz (3.412ms; 0-870.4ms)</td><td>937.5Hz (1.066ms; 0-272ms)</td><td>1875Hz (0.533ms; 0-136ms)</td><td>1875Hz (0.533ms; 0-136ms)</td></tr>
<tr><td>11 = f_{VCXO} ÷ 2^{18}</td><td>146Hz (6.826ms; 0-1740.8)</td><td>468Hz (0.213ms; 0-544ms)</td><td>937.5Hz (1.066ms; 0-272ms)</td><td>937.5Hz (1.066ms; 0-272ms)</td></tr>
</table>

Table 42. Reference Switching Register Descriptions (Cont.)

Bit Field Location						
Bit Field	**Field Type**	**Default**	**Description**			
CNTV[1:0]	R/W	00 (Value: 2 for R_N = ÷1)	Controls the number of required consecutive, valid input reference pulses for clock re-validation on CLK_*n* (n = 0…1), in number of input periods after the R_N input divider. At a LOS event, the re-validation counter loads this setting from the register and counts down by one with every valid, consecutive input signal period. Missing input edges (for one input period) will cause this counter to re-load its setting. An input is re-validated when the counter transitions to zero and the corresponding LOS flag is reset. R_N = 00 (÷1) R_N = 01 (÷2) R_N = 10 (÷4) R_N = 11 (÷8)			
			00 = 2 (shortest) 01 = 16 10 = 32 11 = 64	00 = 4 01 = 32 10 = 64 11 = 128	00 = 8 01 = 64 10 = 128 11 = 256	00 = 16 01 = 128 10 = 256 11 = 512

5.2.8 SYSREF Control Registers

The content of the SYSREF registers controls generation of synchronization signals for JESD204B/C.

Table 43. SYSREF Control Register Bit Field Locations

Register Address	Bit Field Location							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0x38	N_S[3:0]				Reserved			
0x3A	SRWC[7:0]							
0x3B	SRPC[7:0]							
0x3D	Reserved			SRO[1:0]		SRG[2:0]		

Table 44. SYSREF Control Register Descriptions

Bit Field Location			
Bit Field	**Field Type**	**Default**	**Description**
N_S[3:0]	R/W	0000 Value = ÷1	SYSREF Frequency Divider N_S. Sets the SYSREF frequency/pulse rate in conjunction with the output divider N_x. This setting is applicable to all channels configured for SYSREF operation. Divider value = $÷2^{NS[3:0]}$. Configure the N_x channel divider to not exceed a N_S input frequency of 250MHz. N_S[3:0] N_S Divider Value 0000 ÷1 0001 ÷2 0010 $÷2^2$ 0011 $÷2^3$ 0100 $÷2^4$ 0101 $÷2^5$ 0110 $÷2^6$ 0111 $÷2^7$ 1000 $÷2^8$ 1001 $÷2^9$ 1010 $÷2^{10}$ 1011 $÷2^{11}$ 1100 $÷2^{12}$ (÷4096) 1101-1111 Reserved
SRWC[7:0]	R/W	0 (value: 0)	SYSREF pulse wait count Binary value of the number of pulses the SYSREF generator waits before generating the next series of SYSREF pulses. Allows a wait of 1 to 255 pulses before the next series of pulses is generated.
SRPC[7:0]	R/W	0000 0001 (value: 1)	SYSREF pulse count Binary value of the number of SYSREF pulses generated and output at all enabled SYSREF outputs. Allows 1 to 255 pulses to be generated.
SRG[2:0]	R/W	011 Value: Internally triggered	SYSREF Generation Mode (see Table 19) SRG[2:0] SYSREF Operation 000 EXT_SYS input is fanout to SYSREF outputs (no internal sync.) 001 EXT_SYS input is synchronized and fanout to SYSREF outputs 010 Externally triggered SYSREF generation mode 011 Internally triggered SYSREF mode 100 Continuous mode (SYSREF is a clock signal) 101, 110 Reserved 111 Terminate continuous SYSREF generation
SRO[1:0]	R/W	00	SYSREF Pulse Generation (see Table 19) SRO[1:0] SYSREF Operation 00 SRG = 010: Pulsed, rising edge triggered SRG = 011: Pulsed 01 SRG = 010: Pulsed, falling edge triggered SRG = 011: Pulsed with auto repeat 10 Rising edge starts pulse, falling edge stops pulse (SRG = 010) 11 Falling edge starts pulse, rising edge stops pulse (SRG = 010)

5.2.9 Output Channel Registers

The content of the channel registers set the channel state, the clock divider, the clock phase delay.

Table 45. Output Channel Register Bit Field Locations

Register Address	Bit Field Location							
	D7	D6	D5	D4	D3	D2	D1	D0
0x40	Reserved	N_*A*[6:0]						
0x41	ΦWIDE_*A*[8:1]							
0x42	PD_A	1P8_700MV_A	Reserved		RETIME_DIV1_A	Reserved	nC/S_SEL_A	ΦWIDE_*A*[0]
0x43	Reserved						BIAS_TYPE_A	nBIAS_A
0x44	Reserved	N_*B*[6:0]						
0x45	ΦWIDE_*B*[8:1]							
0x46	PD_B	1P8_700MV_B	Reserved		RETIME_DIV1_B	Reserved	nC/S_SEL_B	ΦWIDE_*B*[0]
0x47	Reserved						BIAS_TYPE_B	nBIAS_B
0x48	Reserved	N_*C*[6:0]						
0x49	ΦWIDE_*C*[8:1]							
0x4A	PD_C	Reserved			RETIME_DIV1_C	EXT_VCO_SEL_C	nC/S_SEL_C	ΦWIDE_*C*[0]
0x4B	Reserved							
0x4C	Reserved	N_*D*[6:0]						
0x4D	ΦWIDE_*D*[8:1]							
0x4E	PD_D	Reserved			RETIME_DIV1_D	EXT_VCO_SEL_D	nC/S_SEL_D	ΦWIDE_*D*[0]
0x4F	Reserved							
0x50	Reserved	N_*E*[6:0]						
0x51	ΦWIDE_*E*[8:1]							
0x52	PD_E	1P8_700MV_E	Reserved		RETIME_DIV1_E	Reserved	nC/S_SEL_E	ΦWIDE_*E*[0]
0x53	Reserved						BIAS_TYPE_E	nBIAS_E
0x54	Reserved	N_*F*[6:0]						
0x55	ΦWIDE_*F*[8:1]							
0x56	PD_F	1P8_700MV_F	Reserved		RETIME_DIV1_F	Reserved	nC/S_SEL_F	ΦWIDE_*F*[0]
0x57	Reserved						BIAS_TYPE_F	nBIAS_F
0x58	Reserved	N_*G*[6:0]						
0x59	ΦWIDE_*G*[8:1]							
0x5A	PD_G	1P8_700MV_G	Reserved		RETIME_DIV1_G	Reserved	nC/S_SEL_G	ΦWIDE_*G*[0]

Table 45. Output Channel Register Bit Field Locations (Cont.)

Register Address	Bit Field Location							
	D7	D6	D5	D4	D3	D2	D1	D0
0x5B	Reserved						BIAS_TYPE_G	nBIAS_G
0x5C	Reserved	N_*H*[6:0]						
0x5D	ΦWIDE_*H*[8:1]							
0x5E	PD_H	1P8_700MV_H	Reserved		RETIME_DIV1_H	Reserved	nC/S_SEL_H	ΦWIDE_*H*[0]
0x5F	Reserved						BIAS_TYPE_H	nBIAS_H

Table 46. Output Channel Register Descriptions[1]

Bit Field Location						
Bit Field	**Field Type**	**Default**	**Description**			
Nx[6:0]	R/W	0001 011 Value = ÷2 × ÷4 = ÷8	Output Frequency Divider Nx. Sets the output frequency. The output divider N_x consists of two serial dividers. The effective output divider is the product of N_x0 and N_x1. N_x0 uses the register bits N_x[2:0] and N_x1 uses N_x[6:3]. The setting N_x0 = 000 will bypass N_x1. The smallest N_x divider value is ÷1, the largest value is 20,480 (N_x0 = 5, N_x1 = 4096). When multiple Nx_0, Nx_1 combination are available to achieve a desired, total N_x divider: use the highest possible Nx_0 divider value.			
			N_x1[6:3]	Divider Value (N_x1)	N_x0[2:0]	Divider Value (N_x0)
			0000	$\div 2^0$	000	÷1 (also bypasses N_x1)
			0001	$\div 2^1$	001	÷2
			0010	$\div 2^2$	010	÷3
			0011	$\div 2^3$	011	÷4
			0100	$\div 2^4$	100	÷5
			0101	$\div 2^5$	101-111	Reserved
			0110	$\div 2^6$		
			0111	$\div 2^7$		
			1000	$\div 2^8$		
			1001	$\div 2^9$		
			1010	$\div 2^{10}$		
			1011	$\div 2^{11}$		
			1100	$\div 2^{12}$		
			1101	Reserved		
			1110	Reserved		
			1111	Reserved		

Table 46. Output Channel Register Descriptions[1] (Cont.)

Bit Field Location			
Bit Field	**Field Type**	**Default**	**Description**
ΦWIDE_*x*[8:0]	R/W	0000 0000 0	Channel *x* wide phase delay. Sets the phase delay common to all outputs in the channel. Delay in ps = ΦWIDE_*x* × 127ps (512 steps). Values are for using the internal VCO. The input frequency to the ΦWIDE_*x* circuit should not exceed 4GHz. ΦWIDE_*x*[8:0]
			0000 0000 0 = 0ps 0000 0000 1 = 0.127 0000 0001 0 = 0.254 … 1 1111 1111 = 64.977ns
PD_*x*	R/W	0 Value: Power up	Channel Power Up State 0 = Channel *x* is powered up. 1 = Channel *x* is powered down. Output, divider and delay circuits are powered down. This bit has precedence over output power-down settings. Powered down outputs should not be terminated with a DC path to GND.
1P8_700MV_*x*	R/W	0	Channel Amplitude 700mV at V_{DDO18} = 1.8V for channels A, B and E - H 0 = Default setting 1 = Set this bit when any output y in channel x is configured to an amplitude of 700mV (A_y[1:0] = 11) and the corresponding supply voltage is V_{DDO18} = 1.8V
RETIME_DIV_*x*	R/W	0	Controls the delay step of the ΦFINE_*y* and ΦWIDE_*x* in a channel operating in SYSREF mode. RETIME_DIV_x has no impact on channels operating in clock mode. When the internal VCO or ext. VCO ≥ 2GHz is used, set RETIME_DIV_*x* = 0 When an external of VCO < 2GHz is used, RETIME_DIV_x can be set to 1 (or to 0). RETIME_DIV_*x* = 0 RETIME_DIV_*x* = 1
			ΦFINE_*y*: delay step: 1 ÷ f_{VCO} (254ps for internal VCO) | ΦFINE_*y*: delay step: 1 ÷ $2f_{VCO}$
			ΦWIDE_*x*: delay step: 1 ÷ f_{VCO} (127ps for internal VCO) Valid settings are 0, 1, 4, 5, 8, 9, … (4n) and (4n+1) Valid delay values: 0 = 0ps 1 = 1 ÷ f_{VCO} (127ps) 2 = Invalid 3 = Invalid 4 = 4 ÷ f_{VCO} (509ps) 5 = 5 ÷ f_{VCO} (636ps) … 252 = 32.043ns 253 = 32.171ns 254 = Invalid 255 = Invalid | ΦWIDE_*x*: delay step: 1 ÷ f_{VCO} Valid settings are 0, 1, 2, 3, 4,…, 255 Valid delay values: 0 = 0ps 1 = 1 ÷ $2f_{VCO}$ 2 = 2 ÷ $2f_{VCO}$ 3 = 3 ÷ $2f_{VCO}$ 4 = 4 ÷ $2f_{VCO}$ 5 = 5 ÷ $2f_{VCO}$ … 252 = 252 ÷ $2f_{VCO}$ 253 = 253 ÷ $2f_{VCO}$ 254 = 254 ÷ $2f_{VCO}$ 255 = 255 ÷ $2f_{VCO}$
nC/S_SEL_*x*	R/W	0	Channel x Clock/SYSREF Select. Setting affects all outputs in the channel. 0 = Channel *x* is a clock channel: output frequency is controlled by N_x divider 1 = Channel *x* is a SYSREF channel: SYSREF output states, frequency/pulse count are defined by the N_x and N_S dividers and SRG, SRO registers.

Table 46. Output Channel Register Descriptions[1] (Cont.)

Bit Field Location			
Bit Field	**Field Type**	**Default**	**Description**
BIAS_TYPE_x	R/W	1	SYSREF Output Voltage Bias Type Applicable to channel outputs in SYSREF operation. Defines the output voltage before and after a SYSREF operation. The output must be set to LVDS. 0 = Q_y outputs are static low before and after a SYSREF event 1 = Q_y output voltage is the signal cross point before and after a SYSREF event This bit is not available for the LVPECL-only outputs of channel C and D.
nBIAS_*x*	R/W	0	Q_y Output Bias Voltage Force Applicable to channel outputs in SYSREF operation. See BIAS_TYPE_x. The output must be set to LVDS. 0 = Q_y During a SYSREF event, the output channel x switches for the defined number of pulses 1 = Q_y During a SYSREF event, the output channel x is static (output voltage defined by BIAS_TYPE) This bit is not available for the LVPECL-only outputs of channel C and D.
EXT_VCO_SEL_*x* x = C, D only	R/W	0	Source (VCO) selector for outputs Q_C0, Q_C1, Q_D0, Q_D1 0 = Both outputs in channel x use the channel logic, frequency divider, and delay circuits. Use for operation with the internal PLL-0, PLL-1 and output frequencies up to 4GHz. 1 = Both outputs in channels x buffers the OSC_1 signal. Channel logic and frequency division is not used. Use for operation with an external oscillator up to 6GHz.

1. *x* = A, B, C, D, E, F, G, H

5.2.10 Output Registers

The content of the output register set the individual output state and phase delay.

Table 47. Clock Output Register Bit Field Locations

Register Address	Bit Field Location							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0x60	PD_*A0*	PD_SYSREF_A0	Reserved		INV_SYSREF_A0	STYLE_*A0*	A_*A0*[1:0]	
0x61	Reserved			ΦFINE_*A0*[1:0]		ΦANLG_*A0*[2:0]		
0x62	Set to 1	Set to 1	Reserved					
0x64	PD_B0	PD_SYSREF_B0	Reserved		INV_SYSREF_B0	STYLE_B0	A_B0[1:0]	
0x65	Reserved			ΦFINE_*B0*[1:0]		ΦANLG_*B0*[2:0]		
0x66	PD_B1	PD_SYSREF_B1	Reserved		INV_SYSREF_B1	STYLE_B1	A_B1[1:0]	
0x67	Reserved			ΦFINE_*B1*[1:0]		ΦANLG_*B1*[2:0]		
0x68	PD_C0	PD_SYSREF_C0	Reserved		INV_SYSREF_C0	Reserved	A_C0[1:0]	
0x69	Reserved			ΦFINE_*C0*[1:0]		ΦANLG_*C0*[2:0]		
0x6A	PD_C1	PD_SYSREF_C1	Reserved		INV_SYSREF_C1	Reserved	A_C1[1:0]	
0x6B	Reserved			ΦFINE_*C1*[1:0]		ΦANLG_*C1*[2:0]		

Table 47. Clock Output Register Bit Field Locations (Cont.)

Register Address	Bit Field Location							
	D7	D6	D5	D4	D3	D2	D1	D0
0x6C	PD_D0	PD_SYSREF_D0	Reserved		INV_SYSREF_D0	Reserved	A_D0[1:0]	
0x6D	Reserved			ΦFINE_*D0*[1:0]		ΦANLG_*D0*[2:0]		
0x6E	PD_D1	PD_SYSREF_D1	Reserved		INV_SYSREF_D1	Reserved	A_D1[1:0]	
0x6F	Reserved			ΦFINE_*D1*[1:0]		ΦANLG_*D1*[2:0]		
0x70	PD_E0	PD_SYSREF_E0	Reserved		INV_SYSREF_E0	STYLE_E0	A_E0[1:0]	
0x71	Reserved			ΦFINE_*E0*[1:0]		ΦANLG_*E0*[2:0]		
0x72	PD_E1	PD_SYSREF_E1	Reserved		INV_SYSREF_E1	STYLE_E1	A_E1[1:0]	
0x73	Reserved			ΦFINE_*E1*[1:0]		ΦANLG_*E1*[2:0]		
0x74	PD_E2	PD_SYSREF_E2	Reserved		INV_SYSREF_E2	STYLE_E2	A_E2[1:0]	
0x75	Reserved			ΦFINE_*E2*[1:0]		ΦANLG_*E2*[2:0]		
0x76	PD_F0	PD_SYSREF_F0	Reserved		INV_SYSREF_F0	STYLE_F0	A_F0[1:0]	
0x77	Reserved			ΦFINE_*F0*[1:0]		ΦANLG_*F0*[2:0]		
0x78	PD_F1	PD_SYSREF_F1	Reserved		INV_SYSREF_F1	STYLE_F1	A_F1[1:0]	
0x79	Reserved			ΦFINE_*F1*[1:0]		ΦANLG_*F1*[2:0]		
0x7A	PD_G0	PD_SYSREF_G0	Reserved		INV_SYSREF_G0	STYLE_G0	A_G0[1:0]	
0x7B	Reserved			ΦFINE_*G0*[1:0]		ΦANLG_*G0*[2:0]		
0x7C	Set to 1	Set to 1	Reserved					
0x7E	PD_H0	PD_SYSREF_H0	Reserved		INV_SYSREF_H0	STYLE_H0	A_H0[1:0]	
0x7F	Reserved			ΦFINE_*H0*[1:0]		ΦANLG_*H0*[2:0]		
0x80	PD_H1	PD_SYSREF_H1	Reserved		INV_SYSREF_H1	STYLE_H1	A_H1[1:0]	
0x81	Reserved			ΦFINE_*H1*[1:0]		ΦANLG_*H1*[2:0]		
0x82	PD_H2	PD_SYSREF_H2	Reserved		INV_SYSREF_H2	STYLE_H2	A_H2[1:0]	
0x83	Reserved			ΦFINE_*H2*[1:0]		ΦANLG_*H2*[2:0]		
0x84	PD_VCXO	Reserved				STYLE_*VCXO*	Reserved	

Table 48. Clock Output Register Descriptions[1]

Bit Field Location				
Bit Field	**Field Type**	**Default**	**Description**	
PD_*y*	R/W	0 Value: Power up	Q_*y* Output Power Down State 0 = Output is powered up (if the corresponding channel is powered up: see channel control bit PD_*x*) 1 = Output is powered down. STYLE, EN_y and A[1:0] settings have no effect. Output should not have a DC path to GND in powered-down state.	
PD_SYSREF_y	R/W	1	Individual output delay circuits ΦFINE_*yx* and ΦANLG_*yx* power-down state. Powers down the entire signal path. 0 = Powered up. Use in SYSREF operation for individual output delay and activity. 1 = Power down of all ΦFINE_*yx* and ΦANLG_*yx* delay circuits and the output buffer itself in output y. Preferred to power down when the channel is configured as clock channel (nC/S_SEL_x = 0) and for the lowest output noise floor.	
INV_SYSREF_y	R/W	0	Individual SYSREF output inversion. Use in SYSREF operation for individual output phase inversion. 0 = Normal output polarity. 1 = SYSREF output is inverted (180°).	
STYLE_y	R/W	1 Value: LVPECL	Q_*y* Output format and termination 0 = 100Ω output termination (LVDS-style termination). 1 = 50Ω output termination of to the specified recommended termination voltage (LVPECL style termination). For LVPECL termination voltages (V_{TT}), see Table 17.	
A_*y*[1:0] y = A0, B0-1, E0-2, F0-1, G0, H0-2	R/W	11 Value: 700mV	Q_*y* Output amplitude	
			Setting for STYLE_*y* = 0 (LVDS)	Setting for STYLE_*y* = 1 (LVPECL)
			A[1:0] = 00: 350mV A[1:0] = 01: 350mV A[1:0] = 10: 500mV A[1:0] = 11: 500mV Termination: 100Ω across	A[1:0] = 00: 300mV A[1:0] = 01: 400mV A[1:0] = 10: 550mV A[1:0] = 11: 700mV Termination: 50Ω to V_{TT} For LVPECL termination voltages (V_{TT}), see Table 17.
A_*y*[1:0] Q_C0, Q_C1, Q_D0, Q_D1 6GHz capable	R/W	11 Value: 700mV	Q_*y* Output amplitude	
			Setting for STYLE_*y* = 0 (LVDS)	Setting for STYLE_*y* = 1 (LVPECL)
			Not supported. Use LVPECL for the outputs Q_C0, Q_C1, Q_D0, Q_D1.	A[1:0] = 00: 300mV A[1:0] = 01: 400mV A[1:0] = 10: 550mV A[1:0] = 11: 700mV Termination: 50Ω to V_{TT} For LVPECL termination voltages (V_{TT}), see Table 17.

Table 48. Clock Output Register Descriptions[1] (Cont.)

Bit Field Location				
Bit Field	**Field Type**	**Default**	**Description**	
ΦFINE_*y*[1:0]	R/W	00	Q_y Output fine phase delay in ps. The delay step is a function of the SYSREF_RETIME_DIV1 bit in the respective channel *x* and is a function of the VCO period. Channel Phase Delay in ns.	
			Setting for internal VCO (3932.16MHz) SYSREF_RETIME_DIV1_*x* = 0: ΦFINE_*y* × 254ps (4 steps). 00 = 0ns 01 = 0.254ns 10 = 0.507ns 11 = 0.763ns	Use for external VCO frequencies < 2GHz SYSREF_RETIME_DIV1_*x* = 1: ΦFINE_*y* × (1 ÷ 2f_{VCO}) ps (4 steps). 00 = 0 ns 01 = 0.509ns 10 = 1.017ns 11 = 1.526ns Example delay value for an external VCO frequency of 983.04MHz
ΦANLG_*y*[2:0]	R/W	000	Q_y Output analog phase delay in ps = ΦANLG_*y* × 30ps (8 steps) Insert a SYSREF analog (buffer delay) phase delay in ps (8 steps) in addition to the delay value in ΦFINE_y. The ΦANLG_*y* delay value varies over PVT by about 20%. 000 = 0ps 001 = 30ps … 111 = 0.210ns	
PD_VCXO	R/W	0	Power down Q_VCXO 0 = Output Q_VCXO power up 1 = Output Q_VCXO power down	
STYLE_VCXO	R/W	0	Q_VCXO Output format and termination 0 = 100Ω output termination (LVDS symmetric termination). Output amplitude is 350mV. 1 = 50Ω output termination of to the specified recommended termination voltage (LVPECL style termination). Output amplitude is 700mV. For LVPECL termination voltages (V_{TT}), see Table 17.	

1. y = A0, B0-1, E0-2, F0-1, G0, H0-2

5.2.11 GPIO and Status Registers

Table 49. Status Register Bit Field Locations

Register Address	Bit Field Location							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0x88	GPIO[7:4]				GPIO[3:0]			
0x89	Reserved							GPIO_POL
0x8C	INTEN_CLK0_LOS	INTEN_CLK1_LOS	Reserved		INTEN_PLL0_LOCK	INTEN_PLL1_LOCK	INTEN_PLL0_HOLD	INTEN_PLL0_REF
0x90	LS_CLK0	LS_CLK1	Reserved		LS_PLL0_LOCK	LS_PLL1_LOCK	LS_PLL0_HOLD	LS_PLL0_REF

Table 49. Status Register Bit Field Locations (Cont.)

Register Address	Bit Field Location							
	D7	D6	D5	D4	D3	D2	D1	D0
0x94	ST_CLK0	ST_CLK1	Reserved		ST_PLL0_LOCK	ST_PLL1_LOCK	ST_PLL0_HOLD	ST_PLL0_REF
0x96	ST_FCV0	Reserved	ST_REF[1:0]		Reserved		Reserved	Reserved
0x97	Reserved	Reserved	Reserved	Reserved	Reserved	ST_RCOSC_INITREF	Reserved	Reserved

Table 50. General Control Register Descriptions

Register Description			
Bit Field	**Field Type**	**Default**	**Description**
GPIO[3:0]	R/W	1011	Configures the function of pin GPIO_0 0000 = Reserved 0001 = PLL-0 Force Holdover (Input) 0010 = PLL-0 Force Control Voltage to V_{DDC33_V} / 2 (Input) 0011-0110 = Reserved 0111 = GPIO_0 and GPIO_1 are input select pins (Input) 1000 = PLL-0 detect (Output) 1001 = PLL-1 Lock detect (Output) 1010 = PLL-0 & PLL-1 Lock detect (Output) 1011 = Input activity alarm (Output) 1100 = Holdover state (Output) 1101 = Interrupt (Output) 1110 = Reserved 1111 = GPIO_0 and GPIO_1 indicate the selected input (Output)
GPIO[7:4]	R/W	1010	Configures the function of pin GPIO_1 0000 = Reserved 0001 = PLL-0 Force Holdover (Input) 0010 = PLL-0 Force Control Voltage to V_{DDC33_V} / 2 (Input) 0011-0110 = Reserved 0111 = Reserved 1000 = PLL-0 Lock detect (Output) 1001 = PLL-1 Lock detect (Output) 1010 = PLL-0 & PLL-1 Lock detect (Output) 1011 = Input activity alarm (Output) 1100 = Holdover state (Output) 1101 = Interrupt (Output) 1110 = Reserved 1111 = Reserved
GPIO_POL	R/W	0	GPIO_0, GPIO_1 Output polarity 0 = Pin polarity normal 1 = Pin polarity inverted. All GPIO outputs report status information with inverted polarity.

Table 50. General Control Register Descriptions (Cont.)

Register Description			
Bit Field	**Field Type**	**Default**	**Description**
INTEN_*alert*	R/W	0	Enables the failure indicator *alert* to trigger an interrupt signal through a GPIO pin configured to interrupt (output) 0 = Interrupt is masked (no interrupt will be triggered) 1 = Alert triggers an interrupt signal through a GPIO pin *alert*: CLK0_LOS: CLK_0 LOS input failure CLK1_LOS: CLK_1 LOS input failure PLL0_LOCK: PLL-0 loss of lock PLL1_LOCK: PLL-1 loss of lock PLL0_HOLD: PLL-0 went into holdover PLL0_REF: No valid reference at PLL-0
LS_CLK*n*	R/W	-	Input CLK_*n* status (latched status of ST_CLK*n*) Read 0 = one or more LOS events detected on CLK_*n* after the last LS_CLK*n* clear Read 1 = No loss-of-signal detected on CLK_*n* input after the last LS_CLK*n* clear Write 1 = Clear LS_CLK*n* status latch (clears pending LS_CLK*n* interrupts on a GPIO)
ST_CLK*n*	R	-	Input CLK_*n* status (momentary) 0 = LOS detected on CLK_*n* 1 = No LOS detected, CLK_*n* input is active
LS_PLL0_LOCK LS_PLL1_LOCK	R/W R/W	- -	PLL-0/1 Lock Status (latched status of ST_PLL0/1_LOCK) Read 0 = One or more unlock events detected after the last LS_PLL0/1 clear Read 1 = No unlock events detected after the last LS_PLL0/1 clear Write 1 = Clear LS_PLL0/1_LOCK status latch (clears pending PLL-0/1 unlock interrupts on a GPIO)
ST_PLL0_LOCK ST_PLL1_LOCK	R R	- -	PLL-0/1 Lock Status (momentary) 0 = Not locked 1 = Locked
LS_PLL0_HOLD	R/W	-	PLL-0 Holdover Status (latched status of ST_PLL0_HOLD) Read 0 = One or more holdover events detected after the last LS_PLL0_HOLD clear Read 1 = No holdover events detected after the last LS_PLL0_HOLD clear Write 1 = Clear LS_PLL0_HOLD status latch (clears pending LS_PLL0_HOLD interrupts on a GPIO)
ST_PLL0_HOLD	R	-	PLL-0 Holdover Status 0 = PLL-0 in holdover 1 = PLL-0 not in holdover
LS_PLL0_REF	R/W	-	Input reference status (latched status of ST_PLL0_REF) Read 0 = Reference to PLL-0 is lost since last reset of this status bit. Read 1 = Reference to PLL-0 is valid since last reset of this status bit. Write 1 = Clear LS_PLL0_REF status latch (clears pending reference status interrupts on a GPIO)
ST_PLL0_REF	R	-	Input reference status 0 = No input reference present to PLL-0 1 = Input reference is present at the clock input (to PLL-0)

Table 50. General Control Register Descriptions (Cont.)

Register Description			
Bit Field	**Field Type**	**Default**	**Description**
ST_FCV0	R	-	Status of PLL-0 Control Voltage forced to VDD33 / 2 0 = Control voltage Vc is not forced to VDD33 / 2 (normal Operation) 1 = Control voltage Vc is forced to VDD33 / 2 either through register configuration or by using a GPIO pin
ST_REF[1:0]	R	-	Current PLL-0 Input Reference Selection Indicates the input selected by the device. The selected input may differ from the input selected by the SEL[1:0] control bits. 00 = CLK_0 01 = CLK_1 10 = Reserved 11 = Reserved
ST_RCOSC_INIT REF	R	-	0 = SYSREF Continuous/ Pulse with auto-repeat mode is not initialized 1 = SYSREF Continuous/Pulse with auto repeat mode is initialized (Continuous mode can be terminated with writing SRG = 111)

5.2.12 Synchronization Control Registers

Table 51. Synchronization Control Bit Field Locations

Register Address	Bit Field Location							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0x98	RELOCK	Reserved						
0x99	INIT_CLK	Reserved						
0x9B	RS	Reserved						

Table 52. General Control Register Descriptions

Register Description			
Bit Field	**Field Type**	**Default**	**Description**
RELOCK	W only Auto-Clear	X	Setting this bit to 1 will force PLL-1 to calibrate and to lock.
INIT_CLK	W only Auto-Clear	X	Set INIT_CLK = 1 to reset/synchronize divider and activate the phase delay functions. Required as part of the startup procedure and before Relock and SYSREF operation is started by RS = 1.
RS	W only Auto-Clear	X	Set RS = 1 to initiate the SYSREF pulse generation. Powers up the SYSREF circuitry and releases the SYSREF pulse(s) as configured by SRG and SRO. Setting RS to 1 should be the last operation, after the frequency dividers are synchronized by setting (INIT_CLK = 1).

5.2.13 Output Enable Registers

Table 53. Output Enable Register Bit Field Locations

Register Address	Bit Field Location							
	D7	D6	D5	D4	D3	D2	D1	D0
0x9C	EN_QD1	EN_QD0	EN_QC1	EN_QC0	EN_QB1	EN_QB0	Reserved	EN_QA0
0x9D	EN_QH0	Reserved	EN_QG0	EN_QF1	EN_QD0	EN_QE2	EN_QE1	EN_QE0
0x9E	Reserved						EN_QH2	EN_QH1
0x9F	Reserved	Reserved	Reserved					

Table 54. Output Enable Register Descriptions

Register Description			
Bit Field	**Field Type**	**Default**	**Description**
EN_*y*	R/W	0	Q_*y* Output enable (asynchronous) 0 = Output is disabled at the logic low state 1 = Output is enabled QC, QD outputs disable to static high state when driven by an external VCO (EXT_VCO_SEL_y = 1).

6. Electrical Characteristics

6.1 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 8V19N882 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 55. Absolute Maximum Ratings

Item	Rating
Supply Voltage, V_{DD_V}	3.6V
Inputs	-0.5V to V_{DD_V} +0.5V
Outputs, V_O (LVCMOS)	-0.5V to V_{DD_V} +0.5V
Outputs, I_O (LVPECL) Continuous Current Surge Current	 50mA 100mA
Outputs, I_O (LVDS) Continuous Current Surge Current	 50mA 100mA
Junction Temperature, T_J	150°C
Storage Temperature, T_{STG}	-65°C to 150°C
ESD - Human Body Model[1]	2000V
ESD - Charged Device Model[1]	750V

1. According to JEDEC JS-001-2012/JESD22-C101.

6.2 Recommended Operating Conditions

Table 56. Recommended Operating Conditions

Item	Rating
Core Supply Voltage, V_{DDC18_V}	1.8V
Core Supply Voltage, V_{DDC33_V}	3.3V
Output Supply Voltage, V_{DDO18_V}	1.8V, 2.5V, 3.3V
Output Supply Voltage, V_{DDO33_V}	3.3V
Operating Junction Temperature, T_J[1]	≤ 125°C
Board Temperature, T_B	Table 75

1. 125°C/10year lifetime is based on the evaluation of intrinsic wafer process technology reliability metrics. The limiting wafer level reliability factor for this technology with respect to high temperature operation is electromigration. The device is verified to the maximum operating junction temperature through simulation.

6.3 Pin Characteristics

Table 57. Pin Characteristics, V_{DDC18_V} = 1.8V±0.1V. V_{DDO18_V} = (1.8V, 2.5V, 3.3V)±0.1V, V_{DDC33_V} = V_{DDO33_V} = 3.3V±0.1V, T_A = -40°C to +105°C (Case)

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
C_{IN}[1]	Input Capacitance	OSC_0, nOSC_0, OSC_1, nOSC_1		2	4	pF
		other inputs		2	4	pF
R_{PU}	Input Pull-Up Resistor	SDAT, nCS nCLK_n, nOSC_0		50 25		kΩ kΩ
R_{PD}	Input Pull-Down Resistor	EXT_SYS, SCLK, CLK_n, OSC_0, GPIO_0, GPIO_1		50		kΩ
R_{OUT}	LVCMOS Output Impedance	MISO, SDAT, GPIO_0, GPIO_1 (when output)		25		Ω

1. Guaranteed by design.

6.4 DC Characteristics

6.4.1 Supply Voltage and Power Consumption

Table 58. Power Supply DC Characteristics, T_A = -40°C to +105°C (Case)[1]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
V_{DDC18_V}	Core Supply Voltage		1.7	1.8	1.9	V
V_{DDO18_V}	Output Supply Voltage		1.7 2.4 3.2	1.8 2.5 3.3	1.9 2.6 3.4	V V V
V_{DDC33_V}	Core Supply Voltage		3.2	3.3	3.4	V
V_{DDO33_V}	Output Supply Voltage		3.2	3.3	3.4	V

1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

Table 59. Current and Power Consumption Characteristics, V_{DDC18_V} = 1.8V ±0.1V. V_{DDO18_V} = (1.8V, 2.5V, 3.3V) ±0.1V, V_{DDC33_V} = V_{DDO33_V} = 3.3V ±0.1V, T_A = -40°C to +105°C (Case)[1]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
I_{DD}	Power Supply Current			690	754	mA
P_{TOT}	Power Consumption	Note[2]		1.83	2	W

1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
2. Input = 122.88MHz, Q_B0, Q_B1, Q_E0-2: 550 mV LVDS, Q_VCXO: 350mV LVDS; Q_A = Q_F = Q_G = OFF; Q_C: 550mV LVPECL; Q_D = OFF Unterminated, N_x = ÷4, Q_H0-2 = 15.36MHz and 350mV LVDS as SYSREF (Internally Triggered Pulse Mode)

Table 60. Typical Power Consumption Characteristics, T_A = 25°C[1]

Symbol	Power Supply Current		Test Case				Unit
			1[2]	2[3]	3[4]	4[5]	
-	Clock outputs	Number (active)	8 + Q_VCXO	8 + Q_VCXO	7 + Q_VCXO	8 + Q_VCXO	—
		Style	LVPECL	LVPECL	LVPECL	LVPECL	—
		Amplitude	550	550	700	700	mV
	SYSREF outputs	Number (active)	8	0	6	8	—
		Style	LVDS	Power down	LVPECL	LVPECL	—
		Amplitude	500	Power down	700	700	mV
I_{DD_A}	Current through VDDO_QA pin		79	0	67	66	mA
I_{DD_B}	Current throughVDDO_QB pin		72	72	72	72	mA
I_{DD_C}	Current throughVDDO33_QC pin		124	124	82	125	mA
I_{DD_D}	Current throughVDDO33_QD pin		124	124	0	125	mA
I_{DD_E}	Current throughVDDO_QE pin		125	0	164	163	mA
I_{DD_F}	Current throughVDDO_QF pin		98	98	98	129	mA
I_{DD_G}	Current throughVDDO_QG pin		79	0	68	66	mA
I_{DD_H}	Current throughVDDO_QH pin		125	0	164	163	mA
I_{DD_CP0}	Current throughVDD33_CP0 pin		24	24	24	22	mA
I_{DD_CP1}	Current throughVDD33_CP1 pin		28	28	28	20	mA
I_{DD_OSC0}	Current throughVDD_OSC0 pin		58	58	43	58	mA
I_{DD_OSC1}	Current throughVDD33_OSC1 pin		78	78	78	78	mA
I_{DD_VCO}	Current throughVDD33_VCO pin		108	107	109	62	mA
$I_{DD\_SPI+INP}$	Current throughVDD_SPI + VDD_INPUT pin		24	22	22	24	mA
I_{DD_GPIO}	Current throughVDD_GPIO pin		1	1	1	1	mA
I_{DD_PLL1}	Current throughVDD_PLL1 pin		83	84	92	73	mA
I_{DD_TOT18}	Total Current	1.8V	744	335	158	156	mA
I_{DD_TOT33}	Total Current	3.3V	486	485	954	1091	mA
P_{TOT}	Power Consumption	Device	2.619	1.879	2.817	3.054	W
P_{TOT}	Power Consumption	System[6]	2.943	2.204	3.433	3.881	W

1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
2. V_{DDC18_V} = 1.8V, V_{DDC33_V} = 3.3V, V_{DDO18_V} = 1.8V, V_{DDO33_V} = 1.8V, f_{CLKn} = 245.76MHz, f_{VCXO} = 122.88MHz, Q_A0, Q_E0-2, Q_G0, Q_H0-2 outputs SYSREF 7.68MHz, Q_B0-1 outputs: 491.52MHz, Q_C0-1, Q_D0-1 outputs: 983.04MHz, Q_F0-1 outputs: 245.76MHz, Q_VCXO = 122.88MHz LVPECL 700mV; Dual PLL mode and internal VCO.
3. V_{DDC18_V} = 1.8V, V_{DDC33_V} = 3.3V, V_{DDO18_V} = 1.8V, V_{DDO33_V} = 1.8V, f_{CLKn} = 245.76MHz, f_{VCXO} = 122.88MHz, Q_B0-1, Q_F0-1 outputs: 491.52MHz, Q_C0-1, Q_D0-1 outputs: 983.04MHz, Q_A0, Q_E0-2, Q_G0, Q_H0-2 outputs power down, Q_VCXO = 122.88MHz LVPECL 700mV; Dual PLL mode and internal VCO.

4. V_{DDC18_V} = 1.8V, V_{DDC33_V} = 3.3V, V_{DDO18_V} = 3.3V, V_{DDO33_V} = 3.3V, f_{CLKn} = 1.92MHz, f_{VCXO} = 122.88MHz, Q_A0: 245.76MHz, Q_B0-1, Q_F0-1 outputs: 491.52MHz, Q_C0: 983.04MHz, Q_G0: 122.88MHz, Q_D0-1 outputs: power down, Q_E0-2, Q_H0-2 outputs SYSREF 7.68MHz, Q_VCXO = 122.88MHz LVDS; Dual PLL mode and internal VCO.
5. V_{DDC18_V} = 1.8V, V_{DDC33_V} = 3.3V, V_{DDO18_V} = 3.3V, V_{DDO33_V} = 3.3V, f_{CLKn} = 491.52MHz, f_{VCXO} = 245.76MHz, Q_A0, Q_B0-1, Q_C0-1, Q_D0-1, Q_G0 outputs: 491.52MHz, Q_E0-2, Q_F0-1, Q_H0-2 outputs: SYSREF 7.68MHz, Q_VCXO = 122.88MHz LVPECL 700mV; Dual PLL mode and external VCO at 5898.24MHz.
6. Includes device power consumption and power dissipated in the external output termination components.

6.4.2 LVCMOS I/O Characteristics

Table 61. LVCMOS DC Characteristics, V_{DDC18_V} = 1.8V±0.1V. V_{DDO18_V} = (1.8V, 2.5V, 3.3V)±0.1V, V_{DDC33_V} = V_{DDO33_V} = 3.3V±0.1V, T_A = -40°C to +105°C (Case)[1]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Unit
Inputs EXT_SYS, GPIO_0, GPIO_1 (1.8V logic)							
V_{IH}	Input High Voltage			1.17		V_{DDC18_V}	V
V_{IL}	Input Low Voltage			-0.3		0.63	V
I_{IH}	Input High Current	Input with pull-down resistor	V_{DDC18_V} = 1.9V, V_{IN} = 1.8V			150	µA
I_{IL}	Input Low Current		V_{DDC18_V} = 1.9V, V_{IN} = 0V	-5			µA
SPI inputs SDAT, SCLK, nCS (1.8V logic)							
V_{IH}	Input High Voltage			1.17		V_{DDC18_V}	V
V_{IL}	Input Low Voltage			-0.3		0.63	V
I_{IH}	Input High Current	Input with pull-down resistor	V_{DDC18_V} = 1.9V, V_{IN} = 1.8V			150	µA
I_{IL}	Input Low Current		V_{DDC18_V} = 1.9V, V_{IN} = 0V	-5			µA
I_{IH}	Input High Current	Input with pull-up resistor	V_{DDC18_V} = 1.9V, V_{IN} = 1.8V			5	µA
I_{IL}	Input Low Current		V_{DDC18_V} = 1.9V, V_{IN} = 0V	-150			µA
Outputs GPIO_0, GPIO_1, SDAT, MISO (1.8V logic)							
V_{OH}	Output High Voltage		I_{OH} = -4mA	1.35			V
V_{OL}	Output Low Voltage		I_{OL} = 4mA			0.45	V

1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

6.5 Differential I/O Characteristics

Table 62. Differential Input DC Characteristics, V_{DDC18_V} = 1.8V±0.1V. V_{DDO18_V} = (1.8V, 2.5V, 3.3V)±0.1V, V_{DDC33_V} = V_{DDO33_V} = 3.3V±0.1V, T_A = -40°C to +105°C (Case)[1]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Unit
I_{IH}	Input High Current	Inputs with pull-down resistor[2]	V_{DDC18_V} = V_{IN} = 1.9V			150	µA
		Input with pull-down/pull-up resistor[3]				150	µA
I_{IL}	Input Low Current	Input with pull-down resistor[2]	V_{DDC18_V} = 1.9V, V_{IN} = 0V	-5			µA
		Input with pull-down/pull-up inputs[3]		-150			µA

1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
2. Non-Inverting inputs: CLK_n, OSC_0
3. Inverting inputs: nCLK_n, nOSC_0

Table 63. LVPECL DC Characteristics, V_{DDC18_V} = 1.8V±0.1V. V_{DDO18_V} = (1.8V, 2.5V, 3.3V)±0.1V, V_{DDC33_V} = V_{DDO33_V} = 3.3V±0.1V, T_A = -40°C to +105°C (Case)[1][2]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Unit
V_{OH}	Output High Voltage	3.3V outputs Q_C, Q_D	300mV Amplitude Setting	V_{DDO33_V} - 0.98		V_{DDO33_V} - 0.75	V
			400mV Amplitude Setting	V_{DDO33_V} - 1.03		V_{DDO33_V} - 0.72	V
			550mV Amplitude Setting	V_{DDO33_V} - 1.10		V_{DDO33_V} - 0.68	V
			700mV Amplitude Setting	V_{DDO33_V} - 1.18		V_{DDO33_V} - 0.63	V
		3.3V outputs Q_A, Q_B, Q_E, Q_F, Q_G, Q_H	300mV Amplitude Setting	V_{DDO18_V} - 1.37		V_{DDO18_V} - 0.51	V
			400mV Amplitude Setting	V_{DDO18_V} - 1.36		V_{DDO18_V} - 0.55	V
			550mV Amplitude Setting	V_{DDO18_V} - 1.35		V_{DDO18_V} - 0.59	V
			700mV Amplitude Setting	V_{DDO18_V} - 1.35		V_{DDO18_V} - 0.63	V
		2.5V outputs Q_A, Q_B, Q_E, Q_F, Q_G, Q_H	300mV Amplitude Setting	V_{DDO18_V} - 1.12		V_{DDO18_V} - 0.72	V
			400mV Amplitude Setting	V_{DDO18_V} - 1.13		V_{DDO18_V} - 0.74	V
			550mV Amplitude Setting	V_{DDO18_V} - 1.17		V_{DDO18_V} - 0.73	V
			700mV Amplitude Setting	V_{DDO18_V} - 1.21		V_{DDO18_V} - 0.73	V
		1.8V outputs Q_A, Q_B, Q_E, Q_F, Q_G, Q_H	300mV Amplitude Setting	V_{DDO18_V} - 1.04		V_{DDO18_V} - 0.79	V
			400mV Amplitude Setting	V_{DDO18_V} - 1.09		V_{DDO18_V} - 0.76	V
			550mV Amplitude Setting	V_{DDO18_V} - 1.17		V_{DDO18_V} - 0.70	V
			700mV Amplitude Setting	V_{DDO18_V} - 1.22		V_{DDO18_V} - 0.67	V
		1.8V output Q_VCXO	700mV Amplitude Setting	V_{DDC18_V} - 1.22		V_{DDC18_V} - 0.67	V

Table 63. LVPECL DC Characteristics, V_{DDC18_V} = 1.8V±0.1V. V_{DDO18_V} = (1.8V, 2.5V, 3.3V)±0.1V, V_{DDC33_V} = V_{DDO33_V} = 3.3V±0.1V, T_A = -40°C to +105°C (Case)[1][2]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Unit
V_{OL}	Output Low Voltage	3.3V outputs Q_C, Q_D	300mV Amplitude Setting	V_{DDO33_V} - 1.25		V_{DDO33_V} - 1.05	V
			400mV Amplitude Setting	V_{DDO33_V} - 1.43		V_{DDO33_V} - 1.17	V
			550mV Amplitude Setting	V_{DDO33_V} - 1.66		V_{DDO33_V} - 1.31	V
			700mV Amplitude Setting	V_{DDO33_V} - 1.88		V_{DDO33_V} - 1.42	V
		3.3V outputs Q_A, Q_B, Q_E, Q_F, Q_G, Q_H	300mV Amplitude Setting	V_{DDO18_V} - 1.55		V_{DDO18_V} - 0.82	V
			400mV Amplitude Setting	V_{DDO18_V} - 1.65		V_{DDO18_V} - 0.92	V
			550mV Amplitude Setting	V_{DDO18_V} - 1.80		V_{DDO18_V} - 1.09	V
			700mV Amplitude Setting	V_{DDO18_V} - 1.95		V_{DDO18_V} - 1.20	V
		2.5V outputs Q_A, Q_B, Q_E, Q_F, Q_G, Q_H	300mV Amplitude Setting	V_{DDO18_V} - 1.55		V_{DDO18_V} - 0.97	V
			400mV Amplitude Setting	V_{DDO18_V} - 1.65		V_{DDO18_V} - 1.07	V
			550mV Amplitude Setting	V_{DDO18_V} - 1.80		V_{DDO18_V} - 1.22	V
			700mV Amplitude Setting	V_{DDO18_V} - 1.95		V_{DDO18_V} - 1.33	V
		1.8V outputs Q_A, Q_B, Q_E, Q_F, Q_G, Q_H	300mV Amplitude Setting	V_{DDO18_V} - 1.49		V_{DDO18_V} - 1.09	V
			400mV Amplitude Setting	V_{DDO18_V} - 1.62		V_{DDO18_V} - 1.17	V
			550mV Amplitude Setting	GND		V_{DDO18_V} - 1.31	V
			700mV Amplitude Setting	GND		V_{DDO18_V} - 1.30	V
		1.8V output Q_VCXO	700mV Amplitude Setting	GND		V_{DDC18_V} - 1.30	V

1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
2. LVPECL outputs terminated according to Table 17.

Table 64. LVDS DC Characteristics, V_{DDC18_V} = 1.8V±0.1V. V_{DDO18_V} = (1.8V, 2.5V, 3.3V)±0.1V, V_{DDC33_V} = V_{DDO33_V} = 3.3V±0.1V, T_A = -40°C to +105°C (Case)[1]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Unit
V_{OS}	Offset Voltage[2]	V_{DDO18_V} = 3.3V	350mV Amplitude Setting		2.25	2.65	V
			500mV Amplitude Setting		2.15	2.55	V
		V_{DDO18_V} = 2.5V	350mV Amplitude Setting		1.45	1.90	V
			500mV Amplitude Setting		1.35	1.80	V
		V_{DDO18_V} = 1.8V	350mV Amplitude Setting		0.75	1.20	V
			500mV Amplitude Setting		0.65	1.05	V
ΔV_{OS}	V_{OS} Magnitude Change				18	50	mV

1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
2. V_{OS} changes with V_{DDO18_V}

6.6 AC Characteristics

Table 65. AC Characteristics, V_{DDC18_V} = 1.8V±0.1V. V_{DDO18_V} = (1.8V, 2.5V, 3.3V)±0.1V, V_{DDC33_V} = V_{DDO33_V} = 3.3V±0.1V, T_A = -40°C to +105°C (Case)[1][2]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
Inputs						
f_{CLK}	Input Frequency[3]	CLK_*n* (R_N=÷8)			2000	MHz
		CLK_*n* (R_N=÷1)			250	MHz
		OSC_0			500	MHz
		OSC_1			6000	MHz
V_{IN}	Input Voltage Amplitude[4]	CLK_*n*, OSC_0	0.3		1.2	V
		OSC_1	0		6	dBm[5]
V_{CMR}	Common Mode Input Voltage	CLK_*n*	1.0		V_{DDC18_V} - (V_{IN}/2)	V
		OSC_0	1.0		V_{DDC18_V} - (V_{IN}/2)	V
		OSC_1	0		V_{DDC33_V}	V
PLL-0						
f_{VCXO}	VCXO Frequency		15	122.88	500	MHz
f_{PFD-0}	Phase Detector Frequency				250	MHz
$f_{P0, M0}$	Input Frequency to P_0 and M_0 divider				250	MHz
f_{M1}	Input Frequency to M_1 divider	M_1 = ÷1…÷7 M_1 > ÷7			1000 4000	MHz
f_{3dB}	Loop Bandwidth	Supported range	20		100	Hz
$t_{D, LOS}$	LOS state detected (measured in input reference periods)[6]	f_{CLK} = 122.88MHz or 245.76MHz			2	T_{IN}
$\Delta_{t, RES}$	PLL Lock Acquisition Time Error	f_{CLK} = 122.88MHz or 245.76MHz Steady-state time error after $t_{D, LOCK}$ = 300ms. Initial frequency error < 200 ppm.			±20	ns
$t_{D, LOCK}$	PLL-0 Lock Detect	Until valid and stable. Measured from the end of the last configuration write (nCS going high) to lock detect at GPIO pin.[7]			60	ms
$t_{D, RES-H}$	Holdover Residual Error	Measured 50ms after the reference clock re-appeared in a holdover scenario. Reference point: final value of clock output phase after all phase transitions settled. Holdover duration up to 200ms.			±8.138	ns
Δ_{fp}	Static Frequency Error	f_{CLK} = 0pbb frequency deviation		0		ppb
Δ_{frms}	Dynamic Frequency Error RMS[8]	f_{CLK} = 0ppb frequency deviation		0		ppb

Table 65. AC Characteristics, V_{DDC18_V} = 1.8V±0.1V. V_{DDO18_V} = (1.8V, 2.5V, 3.3V)±0.1V, V_{DDC33_V} = V_{DDO33_V} = 3.3V±0.1V, T_A = -40°C to +105°C (Case)[1][2] (Cont.)

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
Δ_{fp}	Peak Frequency Deviation during PLL-0 relock	Max. frequency deviation during the relock period after a short-term holdover.			±5	ppm
Δf_{HOLD}	Holdover accuracy	Max. frequency deviation during holdover			±5	ppm
	Charge Pump Leakage	During Holdover			5	nA
PLL-1						
f_{VCO}	VCO Frequency	Internal VCO		3932.16		MHz
		External VCO	700		6000	MHz
f_{PFD-1}	Phase Detector Frequency				500	MHz
f_{M2}	Input Frequency to M2 Divider	Internal VCO (M2 > ÷7)			3932.16	MHz
		External VCO[9]			2949.12	
V_{CP}	ICP_1 Tuning Voltage Range	External VCO	0.3		3.0	V
Outputs						
f_{OUT}	Output Frequency	Q_*y* (C0, C1, D0, D1) EXT_VCO_SEL_*y* = 1			6000	MHz
		Q_*y* (C0, C1, D0, D1) EXT_VCO_SEL_*y* = 0			4000	MHz
		Q_*y* (A0-B1, E0-H2)			4000	MHz
		Q_VCXO			500	MHz
Δ_{fp}	Static Frequency Error at any Q_*y* output	f_{CLK} = 0pbb frequency deviation		0		ppb
Δ_{frms}	Dynamic Frequency Error RMS[10]	f_{CLK} = 0ppb frequency deviation		0		ppb
odc	Output Duty Cycle	Q_*y*, N_x = ÷1, AC coupled[11]	45	50	55	%
		Q_*y*, $N_x \neq$ ÷1, DC coupled	47	50	53	%
t_R / t_F	Output Rise/Fall Time, Differential	Q_*y* (LVPECL), 20% to 80%			280	ps
		Q_y (LVDS), 20% to 80%			330	ps
	Output Rise/Fall Time	LVCMOS outputs, 20%-80%			1	ns
$V_{O(PP)}$[12]	LVPECL Output Amplitude Q_C0-1, Q_D0-1 outputs at V_{DDO33_V}=3.3V, Peak-to-peak, 5898.24MHz	300mV Amplitude Setting	215	244		mV
		400mV Amplitude Setting	318	352		mV
		550mV Amplitude Setting	434	487		mV
		700mV Amplitude Setting	559	613		mV
$V_{O(PP)}$[13]	LVPECL Output Amplitude Q_A, Q_B, Q_E, Q_F, Q_G, Q_H outputs at V_{DDO18_V}=1.8V, Peak-to-peak, 3932.16MHz	300mV Amplitude Setting	247	353		mV
		400mV Amplitude Setting	311	430		mV
		550mV Amplitude Setting	415	580		mV
		700mV Amplitude Setting	466	607		mV

Table 65. AC Characteristics, V_{DDC18_V} = 1.8V±0.1V. V_{DDO18_V} = (1.8V, 2.5V, 3.3V)±0.1V, V_{DDC33_V} = V_{DDO33_V} = 3.3V±0.1V, T_A = -40°C to +105°C (Case)[1][2] (Cont.)

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Unit
V_{OD}[14]	LVDS Output Amplitude Q_A, Q_B, Q_E, Q_F, Q_G, Q_H outputs at V_{DDO18_V}=1.8V, Peak-to-peak, 3932.16MHz		350mV Amplitude Setting	244	322		mV
			500mV Amplitude Setting	370	471		mV
Device Timing							
Δt_{PD}	Propagation delay variation between reference input and any Q_y output (PLL modes)		Measured after phase delay circuits configured	-200		+200	ps
			Temperature drift			1	ps/°C
t_{PD}	Propagation delay		Clock (PLL bypass)[15]	0.79	0.982	1.175	ns
			SYSREF: EXT_SYS to Q_y (SRG=000)[16] Q_A, B, E, F, G, H outputs Q_C, Q_D outputs	 1.69 1.89		 2.79 2.68	 ns ns
*t*sk(o)	Output Skew; NOTE[17] [18] All delays set to 0; all output driven from the same source		Q_*y* (excluding Q_C, Q_D banks)			100	ps
			Bank skew within Q_C, Q_D banks		36	60	ps
			Q_*y* - all outputs at 3.3V		82	120	ps
			Q_*y* (SYSREF)		67	120	ps
			Q_*y* (SYSREF) to Q_*y* (incident rising Q_y edge, excluding Q_C, Q_D banks)		49	100	ps
			Q_*y* (SYSREF) to Q_*y* (incident rising Q_y edge)		79	164	ps
			Q_VCXO to Q_y (Clock) (incident rising edge)			±500	ps
Δ*t*sk(o)	Output to output skew variation (drift) over temperature		Any Q_y to any other Q_y (clock and SYSREF)			1	ps/°C
Δt_S	PLL Feedback Delay Variation		f_{VCO} = 3932.16MHz	-26	0	26	ps
	Q_y Wide Phase Delay Variation		f_{VCO} = 3932.16MHz	-32	0	32	ps
	Q_y Fine Phase Delay Variation		f_{VCO} = 3932.16MHz	-38	0	38	ps
	Q_y Analog Phase Delay Variation		Reference: nominal value	-20	0	+20	%
t_H	Hold Time	EXT_SYS to CLK_n[19]	SRG = 001	6			ns
t_S	Setup Time	EXT_SYS to CLK_n[19]	SRG = 001	-1			ns
t_W	Pulse Width	EXT_SYS[20]	SRG = 001	4Nx ÷ f_{VCO}[20]			ns
			SRG = 010 or 100	4			ns

1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
2. PLL-0 bandwidth = 100Hz.
3. In the PLL modes, the minimum input frequency is determined by achieving PLL lock with the specific external VCXO or VCO components. Minimum input frequency in PLL bypass (fanout buffer) mode is 0Hz. For information for the supported frequency range of the monitor and lock detect circuits, see PLL-0 (VCXO-PLL) Lock Detect, PLL-1 Lock Detect and Monitoring and LOS of Input Signal.
4. V_{IL} should not be less than -0.3V and V_{IH} should not be greater than V_{DD_V}.
5. Measured as single-ended sin-wave, 50Ω terminated, AC coupled.
6. LOS state is detected within two input frequency periods ($f_{CLK} \div P$). Signaling LOS state at a GPIO with a small additional propagation delay.
7. PLL-0 loop bandwidth = 100Hz, f_{CLK_n} = 122.88MHz, f_{PFD} (PLL-0) = 3.84MHz, LOCK_GOOD_COUNT = 100.000 cycles, LOCK_TH = 15, Dual PLL mode.
8. RMS frequency error, measured at any Q_*y* output, caused by Gaussian noise. Weighted with a 1ms low pass time window filter.
9. For external VCO frequencies > 2949.12MHz, set P2_SEL = 1 to pre-divide the VCO frequency by ÷2.
10. RMS frequency error, measured at any Q_*y* output, caused by Gaussian noise. Weighted with a 1ms low pass time window filter.
11. Use AC-coupling when Nx = ÷1. DC-coupled outputs are supported when Nx = ÷1 but duty cycle may degrade to ~65%.
12. Measured single-ended RF output amplitudes are based on after de-embedding the trace and cable losses. For LVPECL termination voltages (V_{TT}), see Table 17.
13. Measured single-ended RF output amplitudes are based on after de-embedding the trace and cable losses. For LVPECL termination voltages (V_{TT}), see Table 17.
14. Measured single-ended RF output amplitudes are based on after de-embedding the trace and cable losses. LVDS outputs terminated 100Ω across terminals
15. PLL bypass: BYP_0 =1, FD_1 = 0 and SRC = 11; Dividers N_x = ÷1, R_N = ÷1 and P_1 = ÷1.
16. Delay values in SYSREF path set to 0.
17. This parameter is defined in accordance with JEDEC standard 65.
18. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points
19. Configuration for SYSREF ext. trigger modes SRG=001: BYP_0 = 0, FBSEL_PLL-0 = 1 (PLL feedback through M_0 and M_1), P_0 = ÷1024, M_0 = ÷1024, M_1 = ÷32, Nx = ÷ 32, N_S = ÷16, f_{CLK} = 122.88MHz, delay stages set to 0. For setup and hold time definition, see Figure 18.
20. Determined by Nx divider in the SYSREF channel: EXT_SYS signal should be sampled at least 4 times by f_{VCO}/Nx. Example: if Nx = ÷32 and using the internal VCO (3932.16MHz), min EXT_SYS pulse width is 32.55ns (4 periods of 122.88MHz).

Table 66. Clock Phase Noise Characteristics, V_{DDC18_V} = 1.8V±0.1V, V_{DDO18_V} = (1.8V, 2.5V, 3.3V)±0.1V, V_{DDC33_V} = V_{DDO33_V} = 3.3V±0.1V, T_A = -40°C to +105°C (Case) [1][2]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Unit
Q_A - Q_H Clock Outputs driven in dual PLL mode, internal VCO							
*t*jit(Ø)	Clock RMS Phase Jitter (Random)		Integration Range: 1kHz - 76.8MHz f_{out} = 983.04MHz f_{out} = 491.52MHz f_{out} = 245.76MHz		 79 94 113	 85 103 132	 fs fs fs
			Integration Range: 12kHz - 20MHz f_{out} = 983.04MHz f_{out} = 491.52MHz f_{out} = 245.76MHz		 67 74 85	 72 80 97	 fs fs fs
L(10Hz)	Clock single-side band phase noise	983.04MHz	10Hz offset [3]		-70	-63	dBc/Hz
L(100Hz)			100Hz offset [3]		-83	-79	dBc/Hz
L(500Hz)			500Hz offset from Carrier		-102	-100	dBc/Hz
L(1kHz)			1kHz offset from Carrier		-108	-107	dBc/Hz
L(10kHz)			10kHz offset from Carrier		-122	-121	dBc/Hz
L(60kHz)			60kHz offset from Carrier		-126	-124	dBc/Hz
L(100kHz)			100kHz offset from Carrier		-127	-126	dBc/Hz
L(200kHz)			200kHz offset from Carrier		-130	-123	dBc/Hz
L(800kHz)			800kHz offset from Carrier		-138.4	-138	dBc/Hz
L(5MHz)			5MHz offset from Carrier		-151	-150.4	dBc/Hz
L(≥10MHz)			≥ 10MHz offset from Carrier and Noise Floor		-152.1	-151.6	dBc/Hz
L(10Hz)	Clock single-side band phase noise	491.52MHz[4]	10Hz offset [3]		-76	-69	dBc/Hz
L(100Hz)			100Hz offset [3]		-89	-85	dBc/Hz
L(500Hz)			500Hz offset from Carrier		-108	-105	dBc/Hz
L(1kHz)			1kHz offset from Carrier		-115	-113	dBc/Hz
L(10kHz)			10kHz offset from Carrier		-128	-126	dBc/Hz
L(60kHz)			60kHz offset from Carrier		-131	-130	dBc/Hz
L(100kHz)			100kHz offset from Carrier		-132.6	-131.4	dBc/Hz
L(200kHz)			200kHz offset from Carrier		-135.6	-134.8	dBc/Hz
L(800kHz)			800kHz offset from Carrier		-144.7	-144	dBc/Hz
L(5MHz)			5MHz offset from Carrier		-154.3	-153.2	dBc/Hz
L(≥10MHz)			≥ 10MHz offset from Carrier and Noise Floor		-154.8	-153.7	dBc/Hz

Table 66. Clock Phase Noise Characteristics, V_{DDC18_V} = 1.8V±0.1V, V_{DDO18_V} = (1.8V, 2.5V, 3.3V)±0.1V, V_{DDC33_V} = V_{DDO33_V} = 3.3V±0.1V, T_A = -40°C to +105°C (Case) [1][2] (Cont.)

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Unit
L(10Hz)	Clock single-side band phase noise	245.76 MHz	10Hz offset[3]		-82	-76	dBc/Hz
L(100Hz)			100Hz offset[3]		-95	-92	dBc/Hz
L(500Hz)			500Hz offset from Carrier		-114	-111	dBc/Hz
L(1kHz)			1kHz offset from Carrier		-121	-119	dBc/Hz
L(10kHz)			10kHz offset from Carrier		-134	-132	dBc/Hz
L(60kHz)			60kHz offset from Carrier		-137	-135	dBc/Hz
L(100kHz)			100kHz offset from Carrier		-138	-137	dBc/Hz
L(200kHz)			200kHz offset from Carrier		-141.4	-140.5	dBc/Hz
L(800kHz)			800kHz offset from Carrier		-150.4	-150	dBc/Hz
L(5MHz)			5MHz offset from Carrier		-157.1	-155.2	dBc/Hz
L(≥10MHz)			≥ 10MHz offset from Carrier and Noise Floor		-157.4	-155.4	dBc/Hz

1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
2. f_{VCXO} = 122.88MHz, phase noise characteristics: 10Hz: -65dBc/Hz, 100Hz: -99dBc/Hz, 1kHz: -126dBc/Hz, 10kHz: -148dBc/Hz, 100kHz: -152dBc/Hz.
3. Determined by the input reference clock and the VCXO.
4. PLL-1 loop bandwidth: 190kHz.

Table 67. Clock Phase Noise Characteristics (External VCO), V_{DDC18_V} = 1.8V±0.1V, V_{DDO18_V} = (1.8V, 2.5V, 3.3V)±0.1V, V_{DDC33_V} = V_{DDO33_V} = 3.3V±0.1V, T_A = -40°C to +105°C (Case)[1][2]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Unit
Q_C, Q_D Clock Outputs driven in dual PLL mode, external VCO, EXT_VCO_SEL_y = 1							
tjit(Ø)	Clock RMS Phase Jitter (Random)		Integration Range: 1kHz - 76.8MHz f_{out} = 983.04MHz		46		fs
			Integration Range: 12kHz - 20MHz f_{out} = 983.04MHz		21		fs
L(10Hz)	Clock single-side band phase noise	983.04MHz	10Hz offset [3]		-50.8		dBc/Hz
L(100Hz)			100Hz offset [3]		-78.0		dBc/Hz
L(500Hz)			500Hz offset from Carrier		-101.3		dBc/Hz
L(1kHz)			1kHz offset from Carrier		-109		dBc/Hz
L(10kHz)			10kHz offset from Carrier		-128.1		dBc/Hz
L(60kHz)			60kHz offset from Carrier		-145.5		dBc/Hz
L(100kHz)			100kHz offset from Carrier		-149		dBc/Hz
L(200kHz)			200kHz offset from Carrier		-151.8		dBc/Hz
L(800kHz)			800kHz offset from Carrier		-154.2		dBc/Hz
L(5MHz)			5MHz offset from Carrier		-154.3		dBc/Hz
L(≥10MHz)			≥ 10MHz offset from Carrier and Noise Floor		-154.4		dBc/Hz

1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
2. f_{VCXO} = 491.52MHz, phase noise characteristics: phase noise characteristics: 10Hz: -67dBc/Hz, 100Hz: -101dBc/Hz, 1kHz: -124dBc/Hz, 10kHz: -145dBc/Hz, 100kHz: -153dBc/Hz
3. Determined by the input reference clock and the VCXO.

Table 68. SYSREF Phase Noise, Spurious and Isolation Characteristics, V_{DDC18_V} = 1.8V±0.1V. V_{DDO18_V} = (1.8V, 2.5V, 3.3V)±0.1V, V_{DDC33_V} = V_{DDO33_V} = 3.3V±0.1V, T_A = -40°C to +105°C (Case)[1][2]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Unit
Q_A - Q_H SYSREF Outputs driven in dual PLL mode, internal VCO							
tjit(Ø)	Clock RMS Phase Jitter (Random)		Integration Range: 12kHz - 3.84MHz f_{out} = 7.68MHz		1	1.2	ps
L(500)	SYSREF single-side band phase noise	30.72MHz	500Hz offset		-131	-130	dBc/Hz
L(1kHz)			10kHz offset from Carrier		-150	-149	dBc/Hz
L(60kHz)			60kHz offset from Carrier		-153	-151	dBc/Hz
L(800kHz)			800kHz offset from Carrier		-159	-156	dBc/Hz
L(≥3M)			≥ 3MHz offset from Carrier and Noise Floor		-160	-156	dBc/Hz

Table 68. SYSREF Phase Noise, Spurious and Isolation Characteristics, V_{DDC18_V} = 1.8V±0.1V. V_{DDO18_V} = (1.8V, 2.5V, 3.3V)±0.1V, V_{DDC33_V} = V_{DDO33_V} = 3.3V±0.1V, T_A = -40°C to +105°C (Case)[1][2]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Unit
L(500Hz)	SYSREF single-side band phase noise	15.36MHz	500Hz offset		-136	-134	dBc/Hz
L(10kHz)			10kHz offset from Carrier		-155	-153	dBc/Hz
L(60kHz)			60kHz offset from Carrier		-157	-155	dBc/Hz
L(800kHz)			800kHz offset from Carrier		-161	-156	dBc/Hz
L(≥3MHz)			≥ 3MHz offset from Carrier and Noise Floor		-161	-156	dBc/Hz
L(500Hz)	SYSREF single-side band phase noise	7.68MHz	500Hz offset		-142	-139	dBc/Hz
L(10kHz)			10kHz offset from Carrier		-158	-155	dBc/Hz
L(60kHz)			60kHz offset from Carrier		-160	-156	dBc/Hz
L(800kHz)			800kHz offset from Carrier		-162	-155	dBc/Hz
L(≥3MHz)			≥ 3MHz offset from Carrier and Noise Floor		-162	-155	dBc/Hz

1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
2. f_{VCXO} = 122.88MHz, phase noise characteristics: 10Hz: -65dBc/Hz, 100Hz: -99dBc/Hz, 1kHz: -126dBc/Hz, 10kHz: -148dBc/Hz, 100kHz: -152dBc/Hz

Table 69. Spurious and Isolation Characteristics, V_{DDC18_V} = 1.8V±0.1V. V_{DDO18_V} = (1.8V, 2.5V, 3.3V)±0.1V, V_{DDC33_V} = V_{DDO33_V} = 3.3V±0.1V, T_A = -40°C to +105°C (Case)

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Unit
Q_A - Q_H Clock Outputs driven in dual PLL mode, internal VCO							
L	Spurious signals[1] (Q_y)	983.04MHz	100Hz - 300Hz		-82	-81	dB
			300Hz - 100kHz		-103	-97	dB
			100kHz - 100MHz		-94	-88	dB
			122.88MHz spurious		-88	-84	dB
			245.76MHz spurious		-75	-72	dB
			491.52MHz spurious		-74	-72	dB
		491.52MHz	100Hz - 300Hz		-90	-85	dB
			300Hz - 100kHz		-98	-92	dB
			100kHz - 100MHz		-99	-97	dB
			122.88MHz spurious		-96	-92	dB
			245.76MHz spurious		-84	-77	dB
		245.76MHz	100Hz - 300Hz		-96	-93	dB
			300Hz - 100kHz		-111	-106	dB
			100kHz - 100MHz		-102	-99	dB
			122.88MHz spurious		-96	-93	dB

Table 69. Spurious and Isolation Characteristics, V_{DDC18_V} = 1.8V±0.1V. V_{DDO18_V} = (1.8V, 2.5V, 3.3V)±0.1V, V_{DDC33_V} = V_{DDO33_V} = 3.3V±0.1V, T_A = -40°C to +105°C (Case)

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Unit
Q_C, Q_D Clock Outputs driven in dual PLL mode, external VCO (5898.24MHz), EXT_VCO_SEL_y = 0							
L	Spurious signals (Q_y)	5898.24MHz	100Hz - 300Hz		-59		dB
			300Hz - 100kHz		-79		dB
			100kHz - 100MHz		-109		dB
			122.88MHz spurious		-84		dB
			245.76MHz spurious		-86		dB
			491.52MHz spurious		-78		dB
Q_A - Q_H SYSREF Outputs driven in dual PLL mode, internal VCO							
L	Spurious signals[2]	30.72MHz	> 500Hz		-71	-69	dB
		15.36MHz	> 500Hz		-71	-68	dB
		7.68MHz	> 500Hz		-73	-71	dB
Output Isolation							
ΔL	Output isolation between any neighboring clock output		f_{OUT} = 983.04MHz	72			dB
			f_{OUT} = 491.52MHz	76			dB
			f_{OUT} = 245.76MHz	93			dB
ΔL	Output isolation between any Q_*y* (clock) and Q_*y* (SYSREF[3]) output		Both SYSREF and clock signals active	68			dB

1. Measured differentially with output delay circuits set to 0ns. Q_G delay circuits should be set to greater than zero to minimize spurious signals coupling into neighboring Q_F outputs.
2. Measured as sum of all spurious amplitudes in one side band in the offset frequency range above 500Hz, excluding the harmonics of the fundamental frequency of n × f_{SYSREF} (e.g., n × 7.68MHz)).
3. SYSREF frequencies: 30.72, 15.36, 7.68MHz

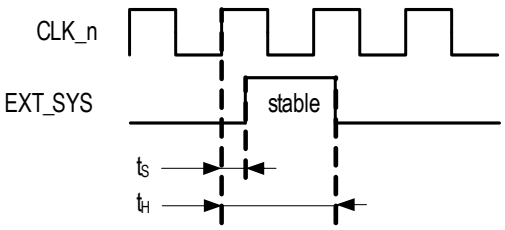


Figure 18. Setup And Hold Time Definition for SRG = 001

7. Clock Phase Noise Characteristics

Measurement conditions for phase noise characteristics:

- f_{VCXO} = 122.88MHz, phase noise characteristics: 10Hz: -65dBc/Hz, 100Hz: -99dBc/Hz, 1kHz: -126dBc/Hz, 10kHz: -148dBc/Hz, 100kHz: -152dBc/Hz
- Input frequency: 122.88MHz
- PLL-0 bandwidth: 100Hz
- PLL-1 bandwidth: 190kHz

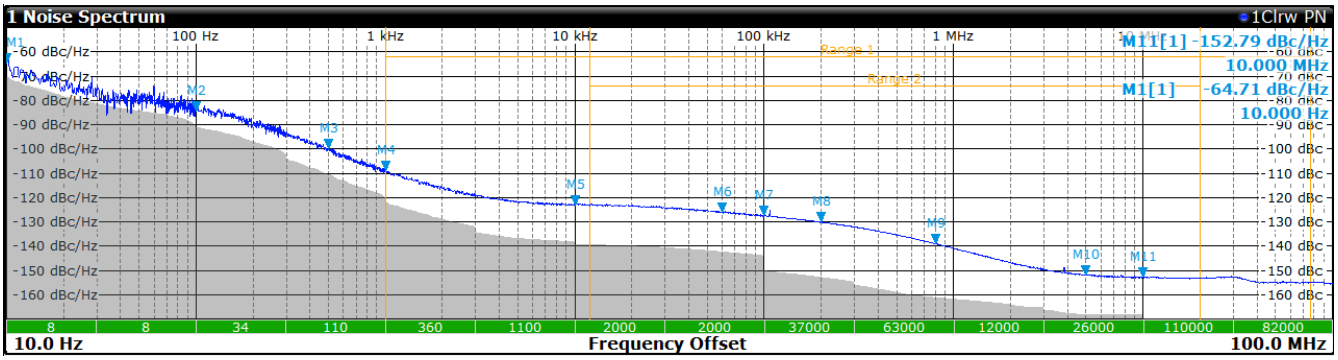


Figure 19. 983.04MHz Output Phase Noise

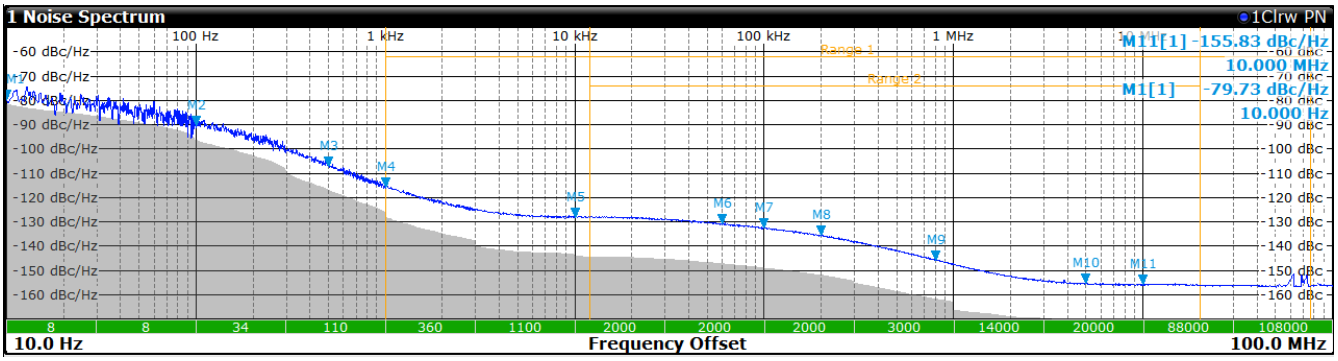


Figure 20. 491.52MHz Output Phase Noise

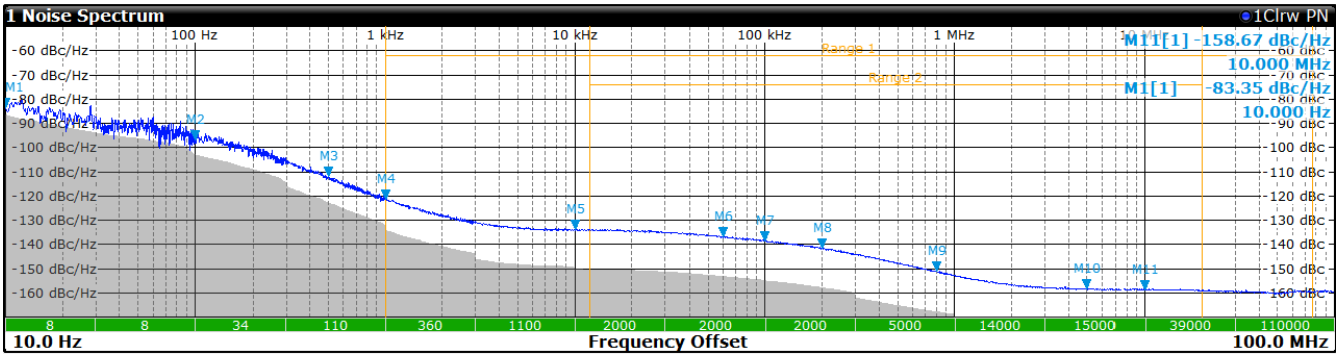


Figure 21. 245.76MHz Output Phase Noise

8. Application Information

8.1 OSC_1 Input Termination (External VCO)

The differential OSC_1/nOSC_1 input is used in applications with an external VCO as oscillator for PLL-1. For signal termination of the external VCO, the OSC_1/nOSC_1 input has two built-in 50Ω termination resistors with its junction connected to the VT_1 pin. The external VCO can have a differential LVPECL, LVDS, or single-ended sinusoidal waveform output driver. For recommended interfaces, see the following figures.

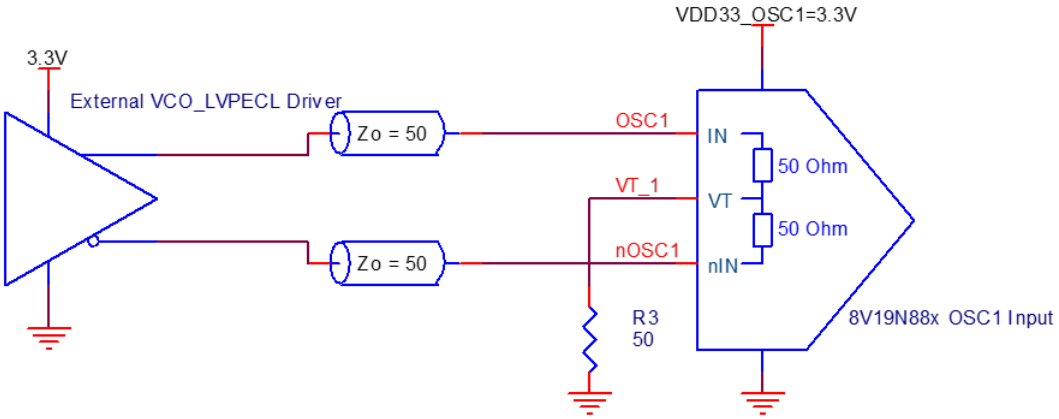


Figure 22. External VCO 3.3V LVPECL Driver to OSC_1/nOSC_1 Input Interface

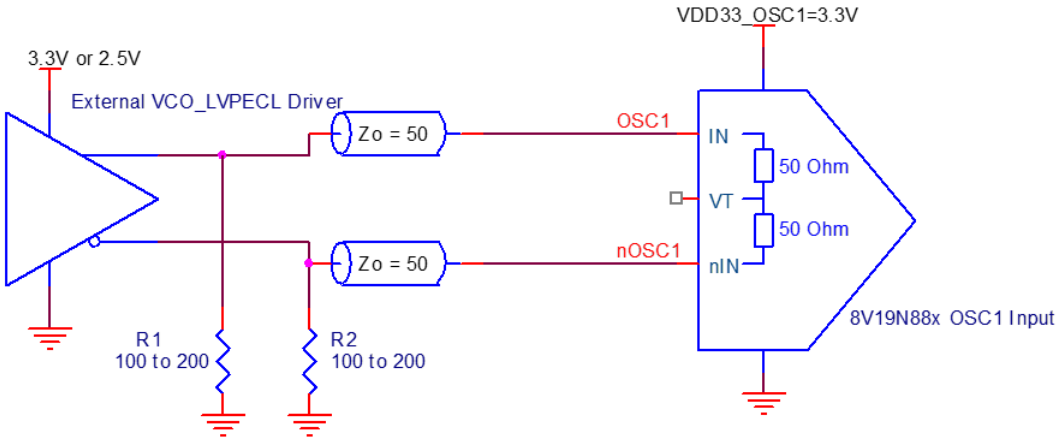


Figure 23. External VCO 3.3V LVPECL Driver to OSC_1/nOSC_1 input, Alternative Interface

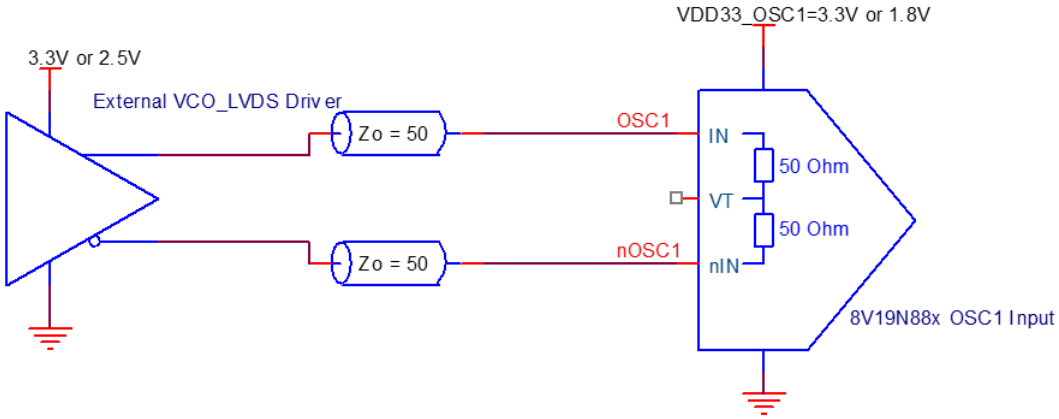


Figure 24. External VCO LVDS Driver to OSC_1/nOSC_1 Input Interface

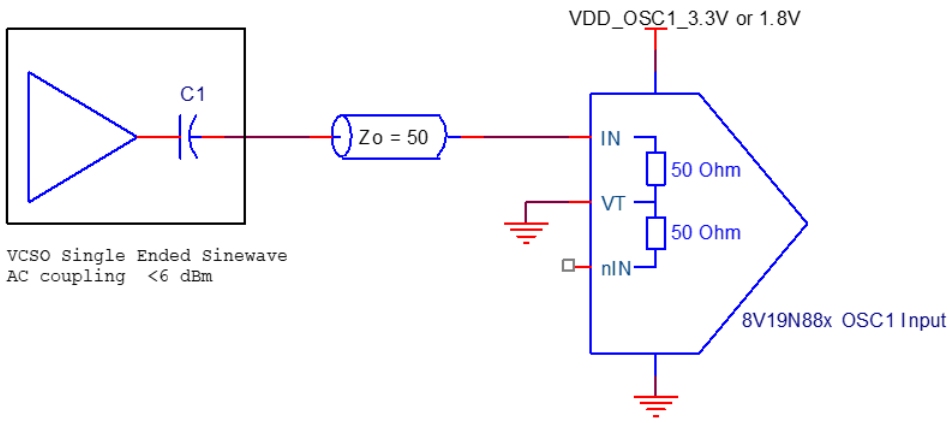


Figure 25. External VCO Single-ended Sinusoidal-Driver to OSC_1/nOSC_1 Input Interface

8.2 Termination for Differential Q_y LVPECL Outputs

When the output is configured to LVPECL, the driver is an open-emitter type requiring a DC current path to the termination voltage V_{TT} through the pull-down resistor. Figure 26 shows a standard LVPECL driver termination, while Figure 27 to Figure 29 show alternative terminations. The LVPECL output driver is configurable and the applicable termination voltage V_{TT} depends on the output amplitude setting and output supply voltage V_{DDO_V} (see the V_{TT} and termination resistor value tables below each diagram).

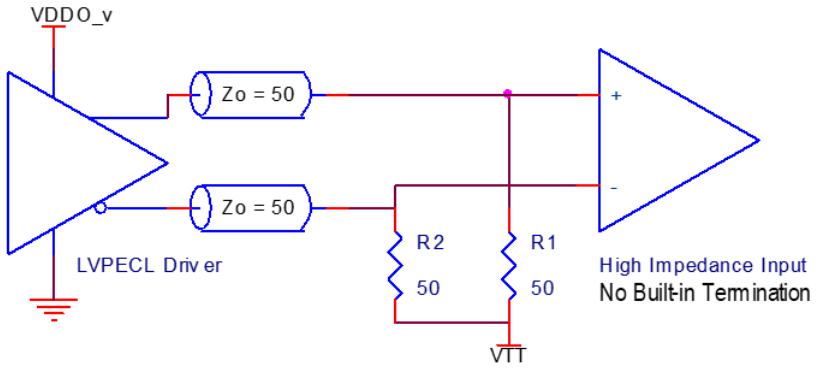


Figure 26. LVPECL Style Termination

Table 70. V_{TT} Values for Output Termination in Figure 26

Output Supply Voltage	Output Amplitude	V_{TT}
V_{DDO_V} = 1.8V	300mV	V_{DDO_v} – 1.55V
	400mV	V_{DDO_v} – 1.65V
	550mV	GND
	700mV	GND
V_{DDO_V} = 2.5V	300mV	V_{DDO_v} – 1.55V
	400mV	V_{DDO_v} – 1.65V
	550mV	V_{DDO_v} – 1.8V
	700mV	V_{DDO_v} – 1.95V

Table 70. V_{TT} Values for Output Termination in Figure 26 (Cont.)

Output Supply Voltage	Output Amplitude	V_{TT}
V_{DDO_V} = 3.3V	300mV	V_{DDO_v} – 1.55V
	400mV	V_{DDO_v} – 1.65V
	550mV	V_{DDO_v} – 1.8V
	700mV	V_{DDO_v} – 1.95V

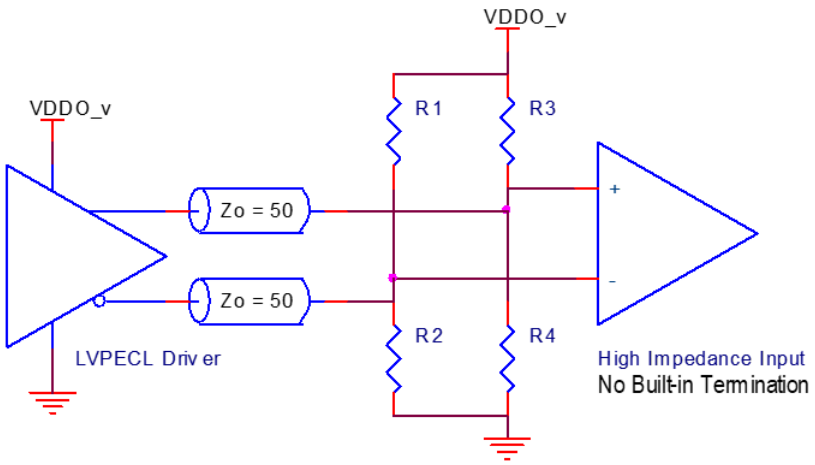


Figure 27. Alternative LVPECL Style Termination

Table 71. Resistor Values for Output Termination in Figure 27

Output Supply Voltage	Output Amplitude	R1, R3	R2, R4
V_{DDO_V} = 1.8V	300mV	360Ω	58.1Ω
	400mV	600Ω	54.5Ω
	550mV	No-pop	50Ω
	700mV	No-pop	50Ω
V_{DDO_V} = 2.5V	300mV	131.6Ω	80.6Ω
	400mV	147.1Ω	75.8Ω
	550mV	178.6Ω	69.4Ω
	700mV	227.3Ω	64.1Ω
V_{DDO_V} = 3.3V	300mV	94.2Ω	106.5Ω
	400mV	100Ω	100Ω
	550mV	110Ω	91.7Ω
	700mV	122.2Ω	84.6Ω

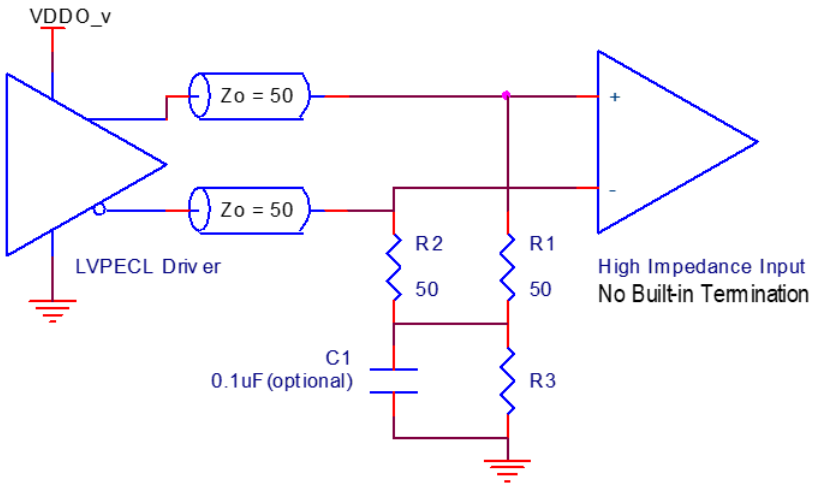


Figure 28. Alternative LVPECL Style Termination

Table 72. Resistor Values for Output Termination in Figure 28

Output Supply Voltage	Amplitude	R3
V_{DDO_V} = 1.8V	300mV	14Ω
	400mV	7.6Ω
	550mV	0Ω
	700mV	0Ω
V_{DDO_V} = 2.5V	300mV	53.1Ω
	400mV	43.8Ω
	550mV	27.9Ω
	700mV	22.4Ω
V_{DDO_V} = 3.3V	300mV	80.6Ω
	400mV	73.3Ω
	550mV	61.2Ω
	700mV	50Ω

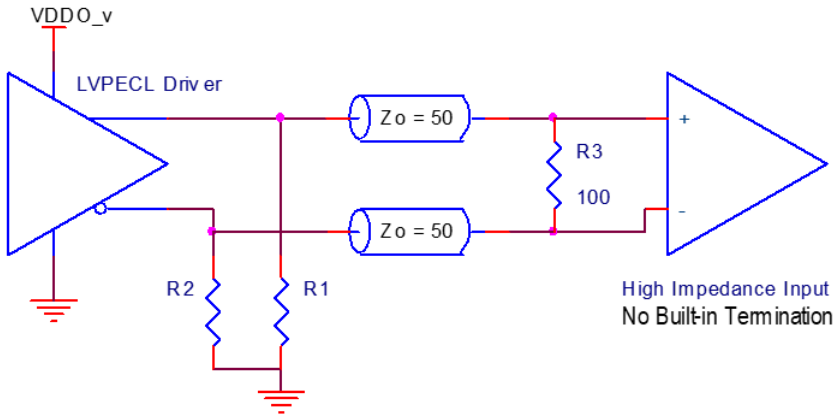


Figure 29. Alternative LVPECL Style Termination

Table 73. Resistor Values for Output Termination in Figure 29

Output Supply Voltage	Amplitude	R1, R2 (Ohm)
V_{DDO_V} = 1.8V	300mV	77.9Ω
	400mV	65.3Ω
	550mV	50Ω
	700mV	50Ω
V_{DDO_V} = 2.5V	300mV	156Ω
	400mV	138Ω
	550mV	116Ω
	700mV	94.9Ω
V_{DDO_V} = 3.3V	300mV	211Ω
	400mV	196Ω
	550mV	172Ω
	700mV	150Ω

8.3 Termination for Differential Q_y LVDS Outputs

Unlike the LVPECL style driver, the LVDS style driver does not require a board-level pull-down resistor. Figure 30 and Figure 31 show typical termination examples with DC coupling for the LVDS style driver. A termination example with AC coupling is shown in Figure 32. All three of the figures are for LVDS receivers with a high-input impedance (no built-in 100Ω termination).

For receivers with built-in 100Ω termination, see footnote [2]. The LVDS termination examples in the figures are independent of the output amplitude setting and the output supply voltage V_{DDO_V}.

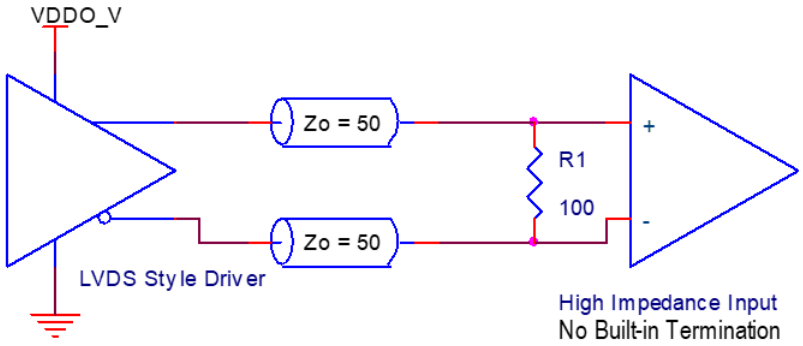


Figure 30. LVDS Style Driver Termination (DC Coupled)

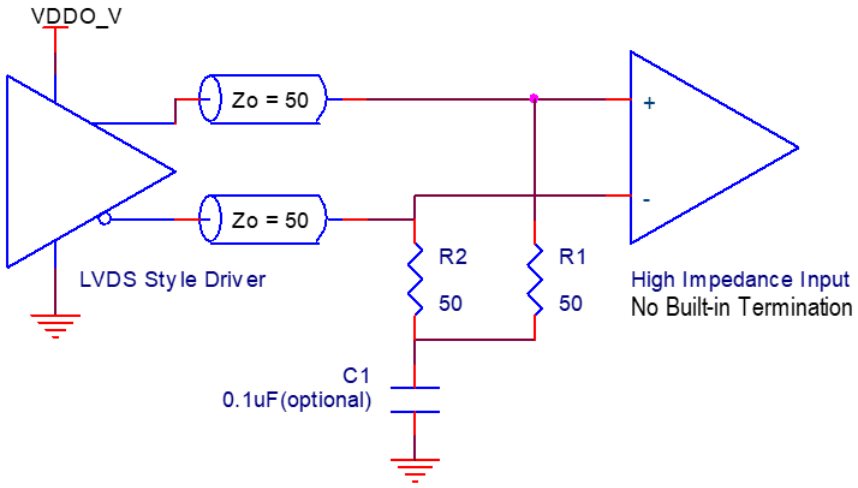


Figure 31. LVDS Style Alternative Driver Termination (DC Coupled)

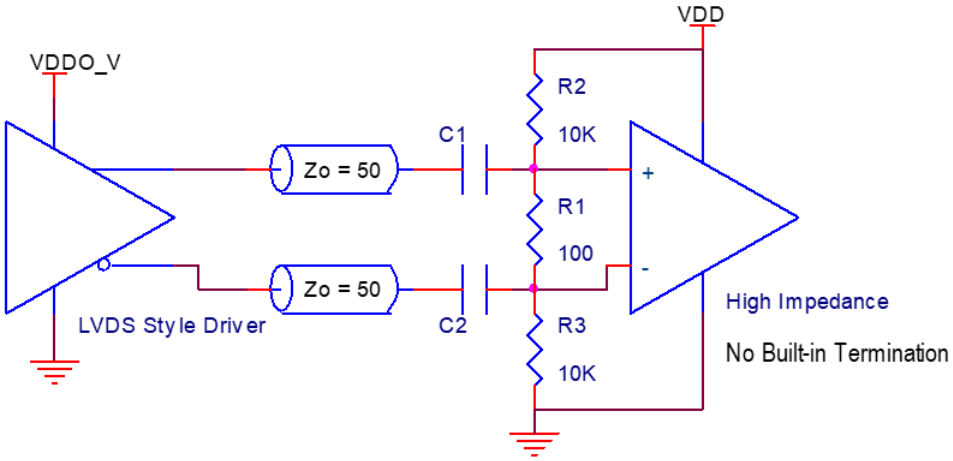


Figure 32. LVDS Style Alternative Driver Termination (AC Coupled)[2]

2. For receivers with built-in 100Ω termination that provides its own DC offset (self-bias): Apply the AC-coupled termination shown in Figure 32 and do not populate the resistors R1, R2, and R3.

9. Thermal Characteristics

Table 74. Thermal Characteristics for the 76 VFQFN Package[1]

Multi-Layer PCB, JEDEC Standard Test Board				
Symbol	**Thermal Parameter**	**Condition**	**Value**	**Unit**
Θ_{JA}	Junction to ambient	0 m/s air flow	22.8	°C/W
		1 m/s air flow	19.3	
		2 m/s air flow	17.7	
		3 m/s air flow	16.9	
Θ_{JC}	Junction to case	-	10	
Θ_{JB}	Junction to board	-	0.3	

1. Standard JEDEC 2S2P multilayer PCB

9.1 Temperature Considerations

The 8V19N882 supports applications in a natural convection environment as long as the junction temperature does not exceed the specified junction temperature, T_J. In applications where the heat dissipates through the PCB, Θ_{JB} is the correct metric to calculate the junction temperature. The following calculation uses the junction-to-board thermal characterization parameter Θ_{JB} to calculate the junction temperature, T_J. Care must be taken to not exceed the maximum allowed junction temperature, T_J, of 125°C.

The junction temperature T_J is calculated using the following equation:

$T_J = T_B + \Theta_{JB} \times P_D$, where

- T_J = Junction temperature at steady state condition in (ºC).
- T_B = Case temperature (Bottom) at steady state condition in (ºC).
- Θ_{JB} = Thermal characterization parameter to report the difference between T_J and T_B
- P_{TOT} = Total power dissipation (W)

8V19N882 Maximum power dissipation scenario: With the maximum allowed junction temperature, the maximum device power consumption and at the maximum supply voltages, the maximum supported board temperature can be determined. In this example, the device is configured as described in test case 4 in Table 60 at VDD = 3.3V.

- Total device power dissipation: P_{TOT} = 3.05W

In this scenario and with the Θ_{JB} thermal model, the maximum supported board temperature is:

- $T_{B, MAX} = T_{J, MAX} - \Theta_{JB} \times P_{TOT}$
- $T_{B, MAX}$ = 125ºC - 0.3ºC/W × 3.05W
- $T_{B, MAX}$ = 124.1ºC

From the above calculation example at the maximum power dissipation, the board temperature must be kept below 124.1ºC. The board layout must have sufficient path for heat release from the package exposed pad through the whole board (e.g., via holes surrounding part that causes exposed pad islands should be avoided). Please refer to the application note for further recommendation. It is recommended to apply a thermal analysis for actual application board.

8V19N882 Application power dissipation scenarios: Applications may use device settings that result in a lower power dissipation than the maximum power scenario. The 8V19N882 is a multi-functional, high-speed device that targets a variety of applications. Since this device is highly programmable with a broad range of settings and configurations, the power consumption will vary as settings and configurations are changed. Table 75 shows the

typical current consumption and total device power consumption along with the junction temperature for the 4 test cases shown in Table 60. The table also displays the maximum board temperature for the Θ_{JB} model.

Table 75. Typical Device Power Dissipation and Junction Temperature

Test Case Table 60	Output Configuration	Device	θ_{JB} Thermal Model	
		P_{TOT}	T_J[1]	$T_{B,MAX}$[2]
		W	ºC	ºC
1	Clocks: LVPECL, 550mV SYSREF: LVDS, 500mV	2.619	105.8	124.2
2	Clocks: LVPECL, 550mV SYSREF: power-down	1.879	105.6	124.4
3	Clocks: LVPECL, 700mV SYSREF: LVPECL, 700mV	2.817	105.8	124.2
4	Clocks: LVPECL, 700mV SYSREF: LVPECL, 700mV	3.054	105.9	124.1

1. Junction temperature for a board temperature of T_B = 105ºC.
2. Maximum board temperature for a junction temperature of T_J < 125ºC.

9.2 Package Exposed Pad Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

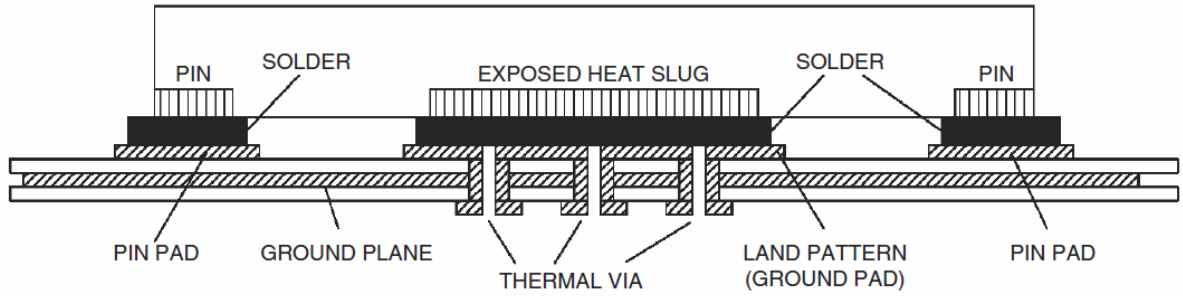


Figure 33. Assembly for Exposed Pad Thermal Release Path - Side View (Drawing not to scale)

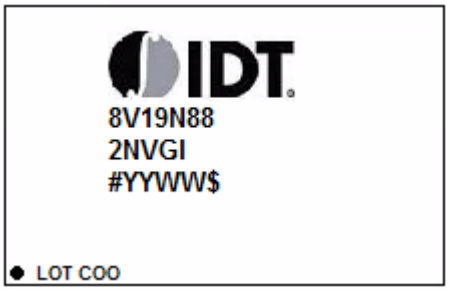
10. Package Outline Drawings

The package outline drawings are located at the end of this document. The package information is the most current data available and is subject to change without revision of this document.

11. Ordering Information

Orderable Part Number	Package	Shipping Packaging	Temperature
8V19N882NVGI	RoHS 6/6 76-VFQFN, 9 x 9 mm²	Tray	-40°C to +95°C
8V19N882NVGI8		Tape & Reel, Pin 1 Orientation: EIA-481-C	
8V19N882NVGI/W		Tape & Reel, Pin 1 Orientation: EIA-481-D/E	

12. Marking Diagram



- Lines 1 and 2 indicate the part number.
- Line 3 indicates the following:
  - "#" denotes stepping.
  - "YY" is the last two digits of the year; "WW" is the work week number when the part was assembled.
  - "$" denotes the mark code.

13. Glossary

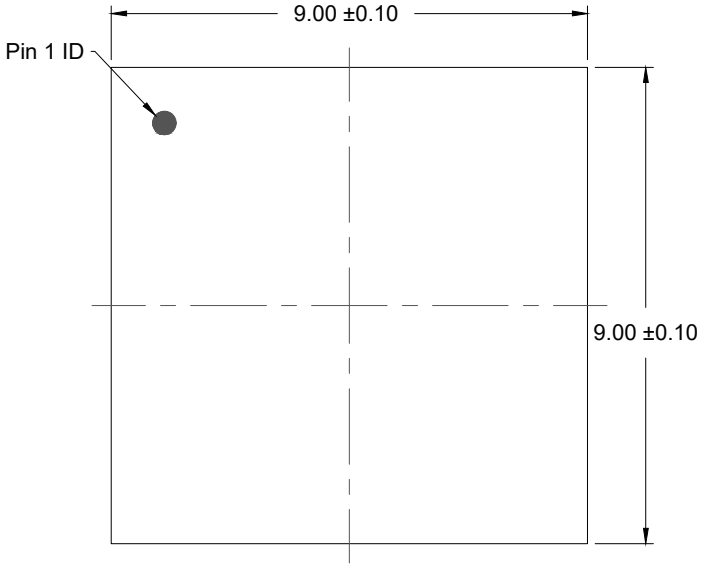
Abbreviation	Description
Index *n*	Denominates a clock input CLK_*n* and associated input frequency divider Rn. Range: 0 to 1.
f_{CLK}	Input frequency to the selected CLK_n input.
f_{REF}	The reference frequency to a PLL (frequency at the phase detector).
Index *x*	Denominates a channel, channel frequency divider, wide channel delay and the associated configuration bits. Range: A, B, C, D, E, F, G, H.
Index y	Denominates an individual output and associated configuration bits. Range: A0, B0, B1, C0, C1, D0, D1, E0, E1, E2, F0, F1, G0, H0, H1, H2.
V_{DD_V}	Denominates all voltage supply pins. Range: V_{DDC18_V}, V_{DDO18_V}, V_{DDC33_V}, V_{DDO33_V}.
V_{DDO_V}	Denominates all output voltage supply pins. Range: V_{DDO18_V} and V_{DDO33_V}.
V_{DDC18_V}	Denominates the 1.8V core voltage supply pins. Range: VDD_INPUT, VDD_OSC0, VDD_PLL1, VDD_GPIO.
V_{DDO18_V}	Denominates the 1.8V, 2.5, 3.3V output supply pins. Range: VDDO_QA, VDDO_QB, VDDO_QE, VDDO_QF, VDDO_QG, VDDO_QH.
V_{DDC33_V}	Denominates the 3.3V core voltage supply pins. Range: VDD33_CP0, VDD33_CP1, VDD33_OSC1, VDD33_VCO.
V_{DDO33_V}	Denominates the 3.3V output supply pins. Range: VDDO33_QC, VDDO33_QD.
[...]	Index brackets describe a group associated with a logical function or a bank of outputs.
{…}	List of discrete values.

14. Revision History

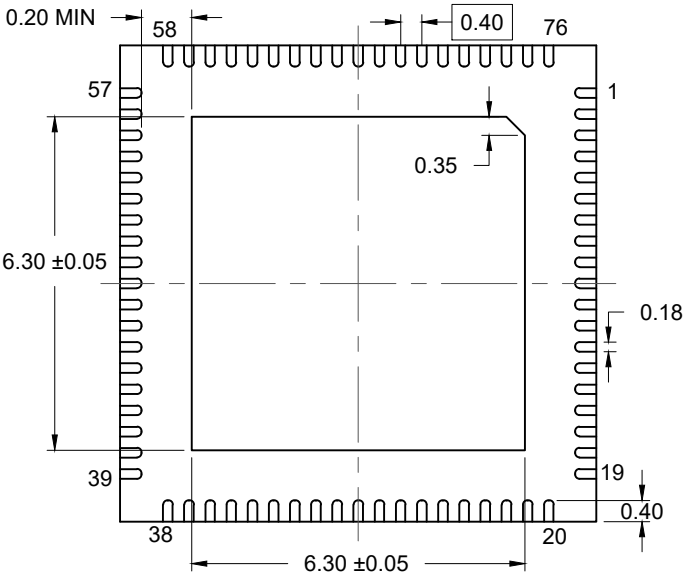
Revision	Date	Description
1.1	Mar 11, 2021	Completed a minor, non-technical update to Table 66.
1.0	Feb 1, 2021	Initial release.

Package Outline Drawing

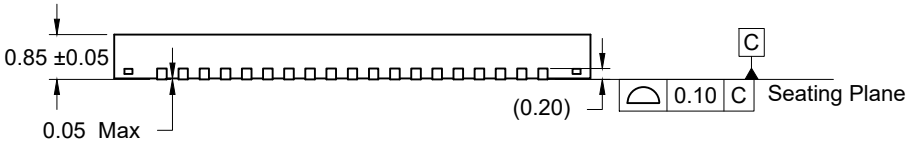
Package Code: NVG76P1
76-VFQFPN 9.0 x 9.0 x 0.85 mm Body, 0.4mm Pitch
PSC-4842-01, Revision: 01, Date Created: Aug 14, 2024



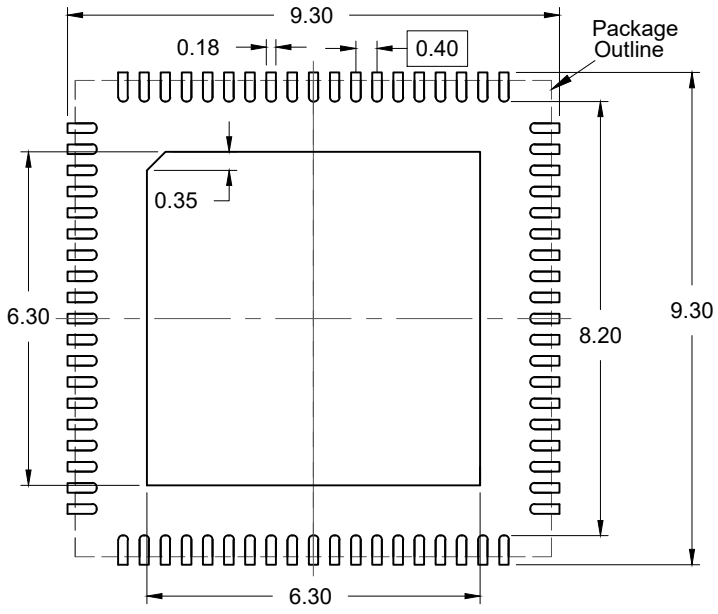
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

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