General Description

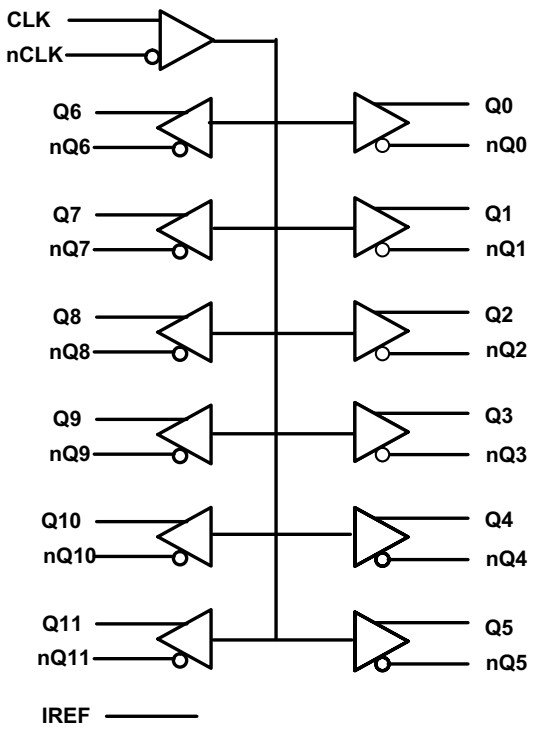
The 8V31012 is a 1-to-12 Differential HCSL Fanout Buffer. The 8V31012 is designed to translate any differential signal levels to differential HCSL output levels. An external reference resistor is used to set the value of the current supplied to an external load/termination resistor. The load resistor value is chosen to equal the value of the characteristic line impedance of 50Ω. The 8V31012 is characterized at an operating supply voltage of 3.3V.

The differential HCSL outputs, accurate crossover voltage and duty cycle make the 8V31012 ideal for interfacing to PCI Express and FBDIMM applications.

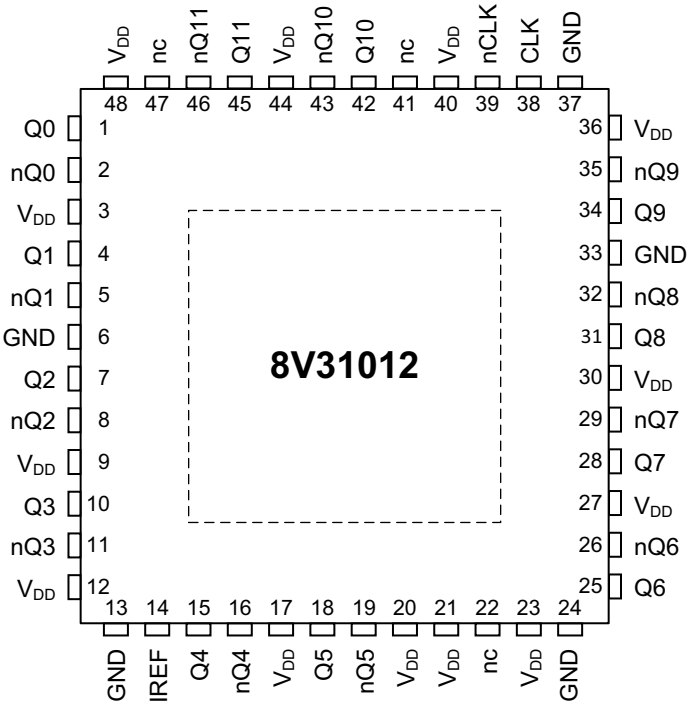
Features

- Twelve differential HCSL outputs
- Translates any differential input signal (LVPECL, LVHSTL, LVDS, HCSL) to HCSL levels without external bias networks
- Maximum output frequency: 250MHz
- Output skew: 265ps (typical)
- $V_{OH:}$ 850mV (maximum)
- Full 3.3V supply voltage
- Available in lead-free (RoHS 6) package
- -40°C to 85°C ambient operating temperature

Block Diagram



Pin Assignment



48-pin, 7mm x 7mm VFQFN Package

Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions

Number	Name	Type	Description
1	Q0	Output	Differential output pair. Differential HCSL interface levels.
2	nQ0	Output	Differential output pair. Differential HCSL interface levels.
3	V_{DD}	Power	Power supply pin.
4	Q1	Output	Differential output pair. Differential HCSL interface levels.
5	nQ1	Output	Differential output pair. Differential HCSL interface levels.
6	GND	Power	Power supply ground.
7	Q2	Output	Differential output pair. Differential HCSL interface levels.
8	nQ2	Output	Differential output pair. Differential HCSL interface levels.
9	V_{DD}	Power	Power supply pin.
10	Q3	Output	Differential output pair. Differential HCSL interface levels.
11	nQ3	Output	Differential output pair. Differential HCSL interface levels.
12	V_{DD}	Power	Power supply pin.
13	GND	Power	Power supply ground.
14	IREF	Input	External fixed precision resistor (950Ω) from this pin to ground provides a reference current used for differential current-mode Qx, nQx clock outputs.
15	Q4	Output	Differential output pair. Differential HCSL interface levels.
16	nQ4	Output	Differential output pair. Differential HCSL interface levels.
17	V_{DD}	Power	Power supply pin.
18	Q5	Output	Differential output pair. Differential HCSL interface levels.
19	nQ5	Output	Differential output pair. Differential HCSL interface levels.
20	V_{DD}	Power	Power supply pin.
21	V_{DD}	Power	Power supply pin.
22	nc	unused	No connect.
23	V_{DD}	Power	Power supply pin.
24	GND	Power	Power supply ground.
25	Q6	Output	Differential output pair. Differential HCSL interface levels.
26	nQ6	Output	Differential output pair. Differential HCSL interface levels.
27	V_{DD}	Power	Power supply pin.
28	Q7	Output	Differential output pair. Differential HCSL interface levels.
29	nQ7	Output	Differential output pair. Differential HCSL interface levels.
30	V_{DD}	Power	Power supply pin.

Table 1. Pin Descriptions

Number	Name	Type	Description
31	Q8	Output	Differential output pair. Differential HCSL interface levels.
32	nQ8	Output	Differential output pair. Differential HCSL interface levels.
33	GND	Power	Power supply ground.
34	Q9	Output	Differential output pair. Differential HCSL interface levels.
35	nQ9	Output	Differential output pair. Differential HCSL interface levels.
36	V_{DD}	Power	Power supply pin.
37	GND	Power	Power supply ground.
38	CLK	Input	Non-inverting differential input.
39	nCLK	Input	Inverting differential clock input.
40	V_{DD}	Power	Power supply pin.
41	nc	unused	No connect.
42	Q10	Output	Differential output pair. Differential HCSL interface levels.
43	nQ10	Output	Differential output pair. Differential HCSL interface levels.
44	V_{DD}	Power	Power supply pin.
45	Q11	Output	Differential output pair. Differential HCSL interface levels.
46	nQ11	Output	Differential output pair. Differential HCSL interface levels.
47	nc	unused	No connect.
48	V_{DD}	Power	Power supply pin.

Output Driver Current

The 8V31012 outputs are HCSL differential current drive with the current being set with a resistor from I_{REF} to ground. For a *single load* and a 50Ω PC board trace, the drive current would typically be set with a R_{REF} of 950Ω which products an I_{REF} of 1.16mA. The I_{REF} is multiplied by a current mirror to an output drive of 12*1.16mA or 13.90mA. See Figure 1 for current mirror and output drive details.

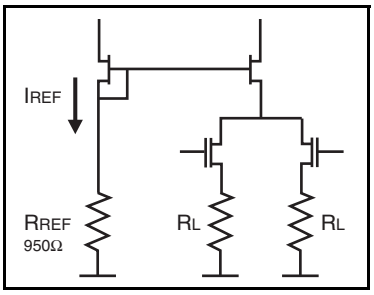


Figure 1. HCSL Current Mirror and Output Drive

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O	-0.5V to V_{DD} + 0.5V
Maximum Junction Temperature	125°C
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 2A. Power Supply DC Characteristics, V_{DD} = 3.3V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current	Output Unterminated			105	mA

Table 2B. Differential DC Characteristics, V_{DD} = 3.3V±5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK, nCLK	V_{DD} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	CLK, nCLK	V_{DD} = 3.465V, V_{IN} = 0V			5	µA
V_{PP}	Peak-to-Peak Voltage[1]			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage[1, 2]			GND + 0.5		V_{DD} – 0.85	V

NOTE 1. V_{IL} should not be less than -0.3V.

NOTE 2. Common mode input voltage is defined as V_{IH}.

AC Electrical Characteristics

Table 3. HCSL AC Characteristics, V_{DD} = 3.3V±5%, T_A = -40°C to 85°C[1, 2, 3]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
t_{PD}	Propagation Delay[4]	Measured on at V_{OX}		2.35	2.75	ns
*t*sk(o)	Output Skew[5, 6]	Measured on at V_{OX}		265	395	ps
*t*sk(pp)	Part-to-Part Skew[6, 7]			335		ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	CLK = 200MHz, Integration Range: 12kHz – 30MHz		0.15		ps
V_{MAX}	Absolute Max Output Voltage[8]	$f \leq$ 150MHz	500		850	mV
V_{MIN}	Absolute Min Output Voltage[8]	$f \leq$ 150MHz	-150		150	mV
V_{CROSS}	Absolute Crossing Voltage[9, 10, 11]		250		550	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all edges[9, 10, 12]				140	mV
	Rise/Fall Edge Rate[13, 14]		0.6		4.0	V/ns
	Rise/Fall Time Matching[15]				20	%
odc	Output Duty Cycle[16]		45		55	%

NOTE 1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 2. Current adjust set for V_{OH} = 0.7V. Measurements refer to PCIEX outputs only.

NOTE 3. Characterized using an R_{REF} value of 950Ω resistor.

NOTE 4. Measured from the differential input cross point to the differential output crossing point.

NOTE 5. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential output cross point.

NOTE 6. This parameter is defined in accordance with JEDEC Standard 65.

NOTE 7. Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross point.

NOTE 8. Measurement using R_{REF} = 950Ω, R_{LOAD} = 50Ω.

NOTE 9. Measurement taken from single-ended waveform.

NOTE 10. Measured at crossing point where the instantaneous voltage value of the rising edge of Qx equals the falling edge of nQx. See Parameter Measurement Information Section.

NOTE 11. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Parameter Measurement Information Section.

NOTE 12. Defined as the total variation of all crossing voltage of rising Qx and falling nQx. This is the maximum allowed variance in the V_{CROSS} for any particular system. See Parameter Measurement Information Section.

NOTE 13. Measurement taken from differential waveform.

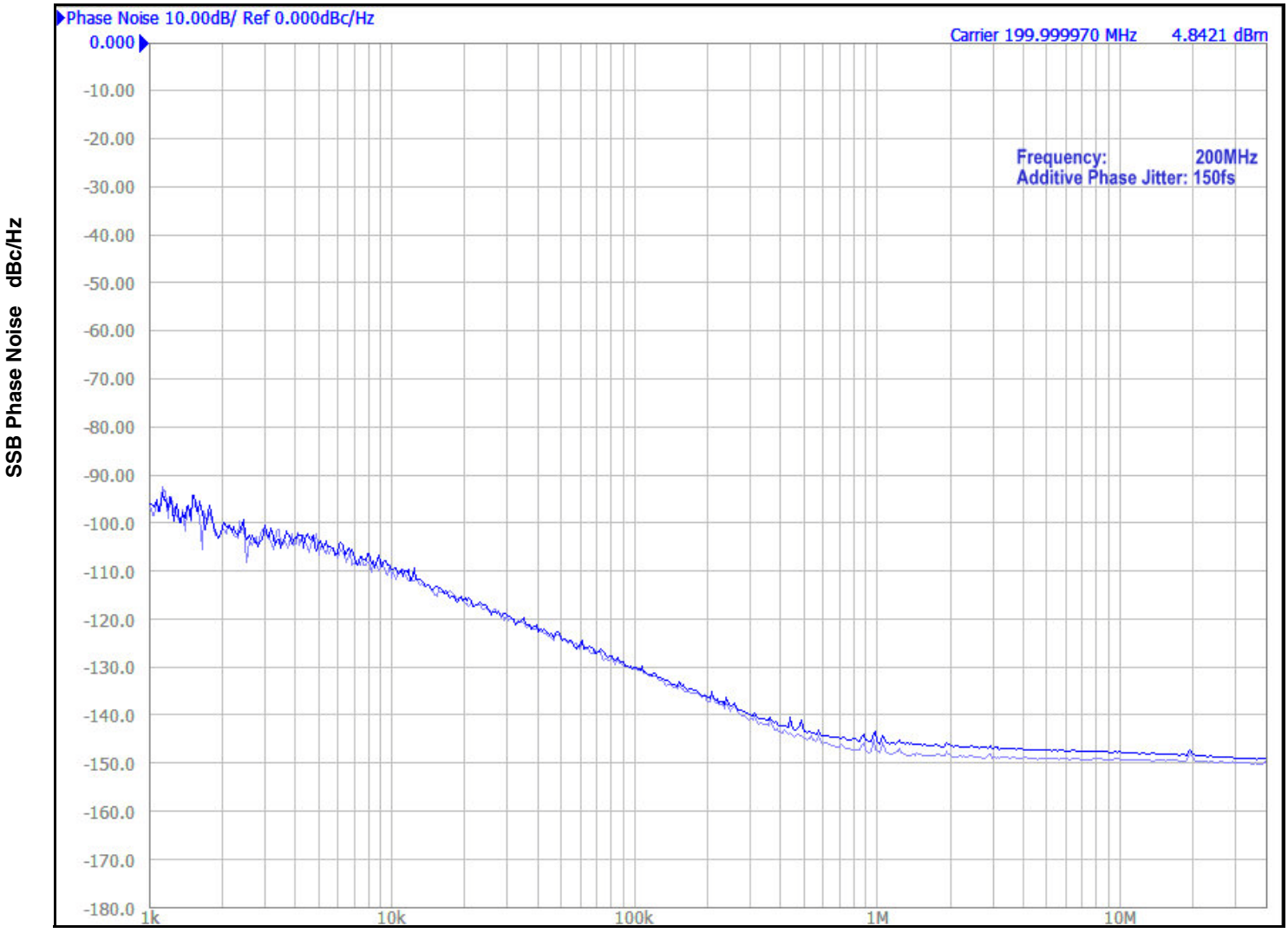
NOTE 14. Measurement from -150mV to +150mV on the differential waveform (derived from Qx minus nQx). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

NOTE 15. Matching applies to rising edge rate for Qx and falling edge rate for nQx. It is measured using a ±75mV window centered on the median cross point where Qx rising meets nQx falling.

NOTE 16. Assuming 50% input duty cycle. Data taken at $f \leq$ 200MHz, unless otherwise specified.

Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



As with most timing specifications, phase noise measurements have issues relating to the limitations of the measurement equipment. The noise floor of the equipment can be higher or lower than the noise floor of the device. Additive phase noise is dependent on both the noise floor of the input source and measurement equipment.

The additive phase jitter for this device was measured using a Stanford Research Systems CG635 input source and an Agilent E5052 phase noise analyzer.

Applications Information

Recommendations for Unused Output Pins

Outputs:

Differential Outputs

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 2 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock is driven from a single-ended 2.5V LVCMOS driver and the DC offset (or swing center) of this signal is 1.25V, the R1 and R2 values should be adjusted to set the V1 at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced while maintaining an edge rate faster than 1V/ns. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

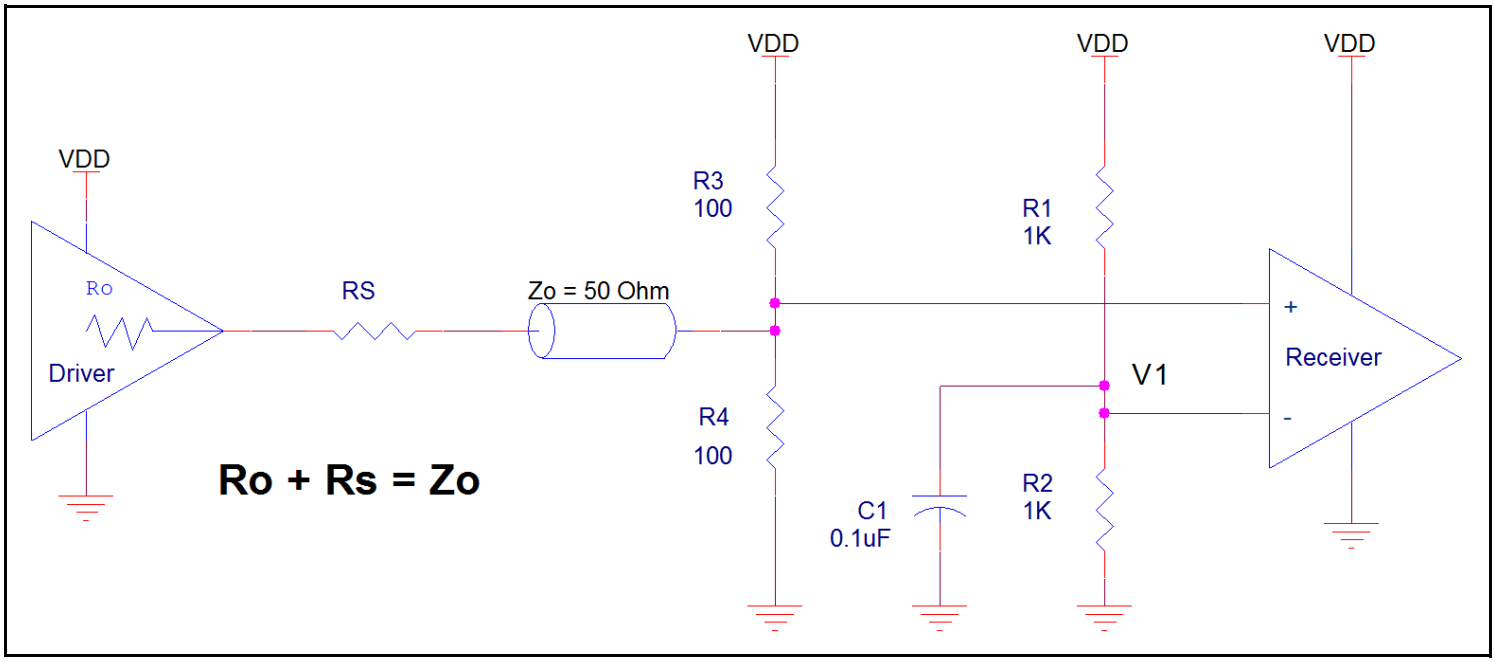


Figure 2. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Differential Clock Input Interface

The CLK/nCLK accepts HCSL, LVDS, LVPECL and LVHSTL and other differential signals. Both differential signals must meet the V_{PP} and V_{CMR} input requirements. *Figure 3A to* Figure 3E show interface examples for the CLK, nCLK input driven by the most common driver types. The input interfaces suggested here are examples only.

Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 3A*, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

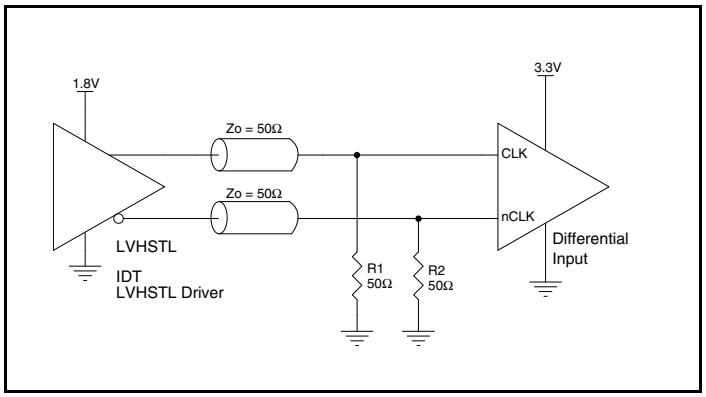


Figure 3A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

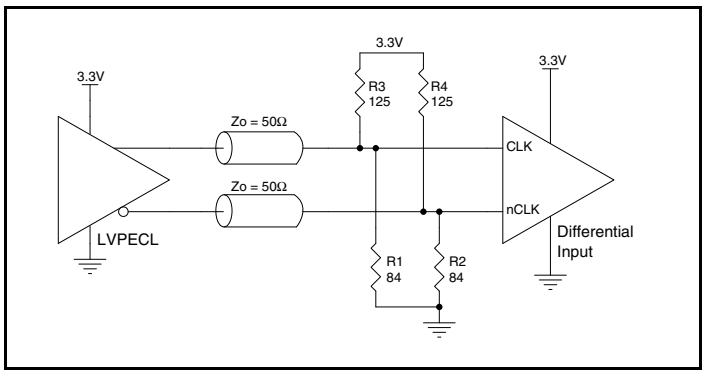


Figure 3B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

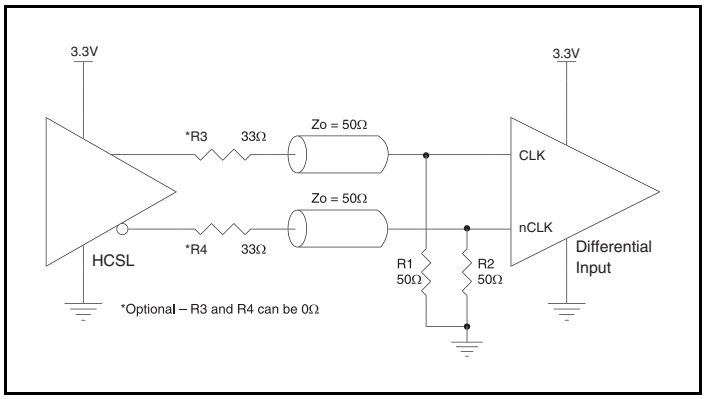


Figure 3C. CLK/nCLK Input Driven by a 3.3V HCSL Driver

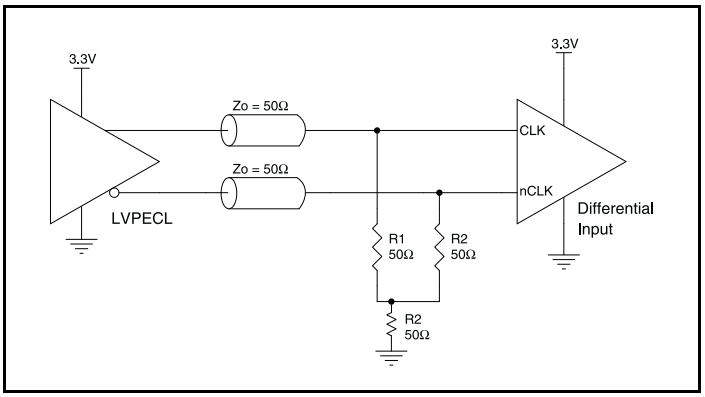


Figure 3D. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

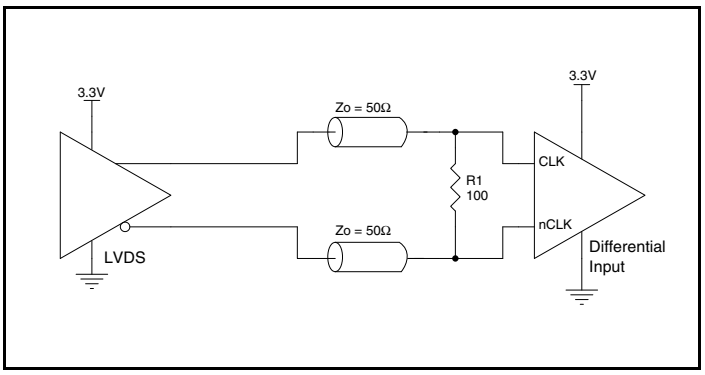


Figure 3E. CLK/nCLK Input Driven by a 3.3V LVDS Driver

Recommended Termination

Figure 4A is the recommended source termination for applications where the driver and receiver will be on a separate PCBs. This termination is the standard for PCI Express™and HCSL output types. All traces should be 50Ω impedance single-ended or 100Ω differential.

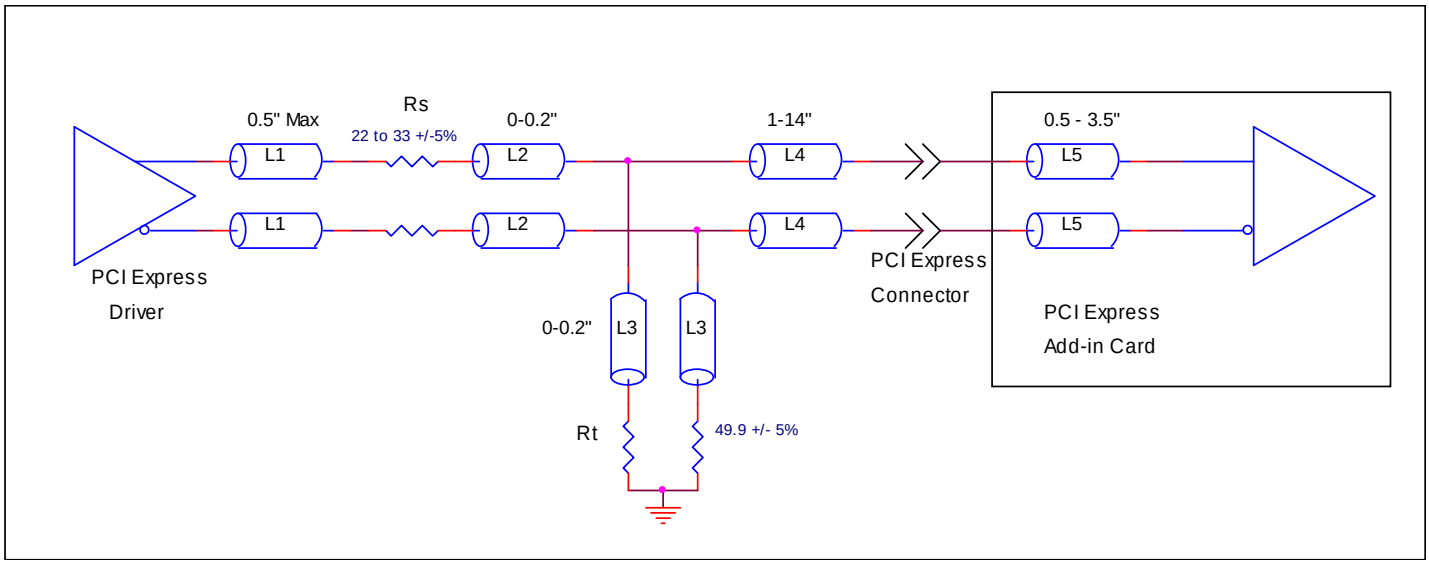


Figure 4A. Recommended Source Termination (where the driver and receiver will be on separate PCBs)

Figure 4B is the recommended termination for applications where a point-to-point connection can be used. A point-to-point connection contains both the driver and the receiver on the same PCB. With a matched termination at the receiver, transmission-line reflections will be minimized. In addition, a series resistor (Rs) at the driver offers flexibility and can help dampen unwanted reflections. The optional resistor can range from 0Ω to 33Ω. All traces should be 50Ω impedance single-ended or 100Ω differential.

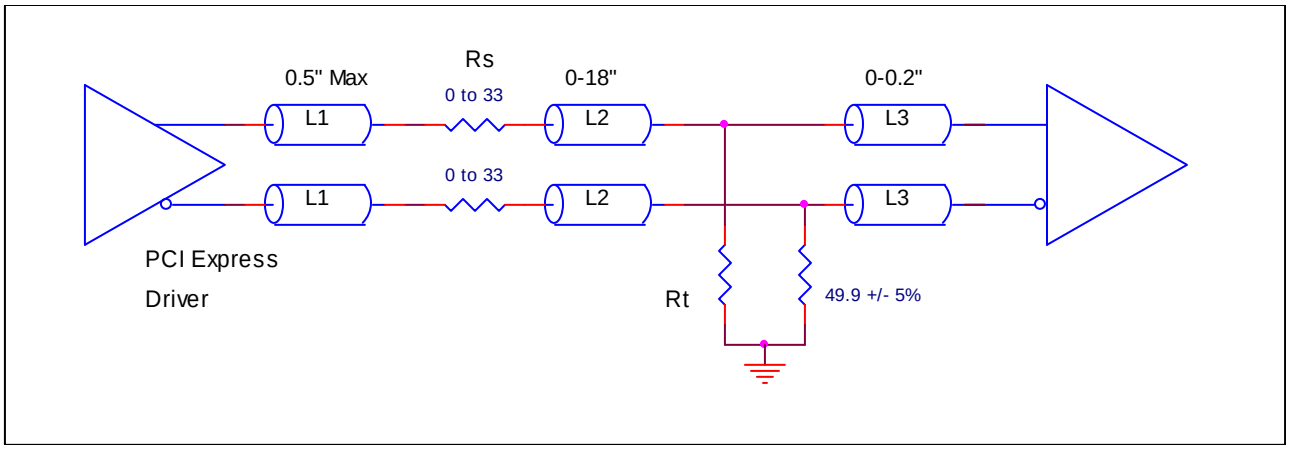


Figure 4B. Recommended Termination (where a point-to-point connection can be used)

EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 5*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

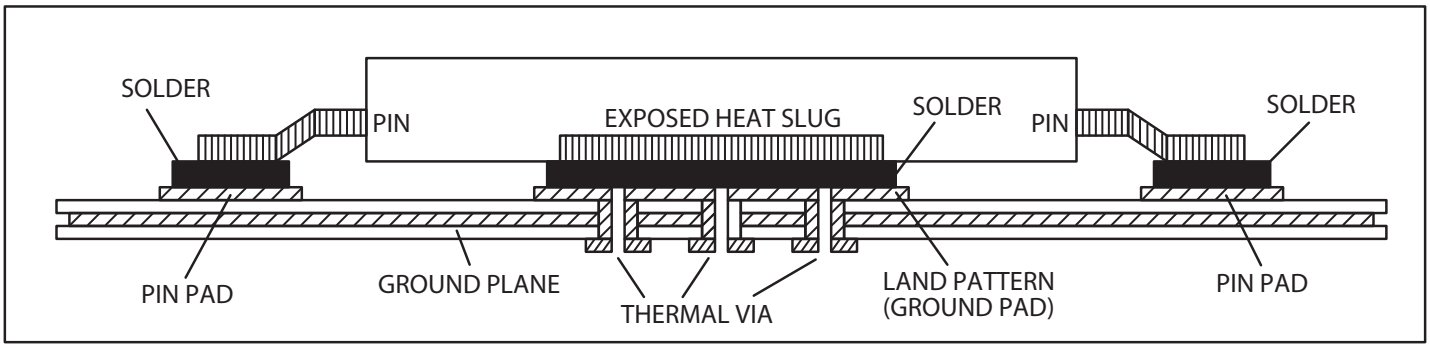


Figure 5. Assembly for Exposed Pad Thermal Release Path - Side View (drawing not to scale)

Power Considerations

This section provides information on power dissipation and junction temperature for the 8V31012.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8V31012 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

Power $(core)_{MAX} = V_{DD\_MAX} * (I_{DD\_MAX})$ = 3.465V *(105mA) = **363.825mW**

- Power $(outputs)_{MAX}$ = **44.5mW/Loaded Output pair**
  If all outputs are loaded, the total power is 12 * 44.5mW = **534mW**

Total Power$_{\_MAX}$ = (3.465V, with all outputs switching) = 363.825mW + 534mW = **897.825mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 29°C/W per Table 4 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.898W *29°C/W = 111°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 4. Thermal Resistance θ_{JA} for 48Lead VFQFN, E-Pad, Forced Convection

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	29.0°C/W	25.4°C/W	22.7°C/W

3. Calculations and Equations.

The purpose of this section is to calculate power dissipation on the IC per HCSL output pair.

HCSL output driver circuit and termination are shown in *Figure 6.*

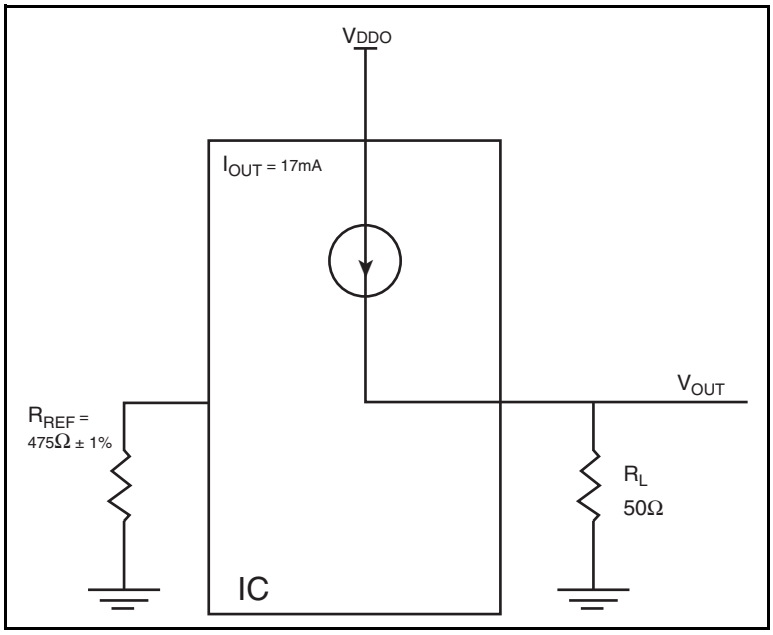


Figure 6. HCSL Driver Circuit and Termination

HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs when V_{DDO_MAX}.

Power = $(V_{DDO\_MAX} - V_{OUT}) * I_{OUT}$,
since $V_{OUT} - I_{OUT} * R_L$

$= (V_{DDO\_MAX} - I_{OUT} * R_L) * I_{OUT}$

$= (3.465V - 17mA * 50\Omega) * 17mA$

Total Power Dissipation per output pair = **44.5mW**

Reliability Information

Table 5. θ_{JA} vs. Air Flow Table for a 48 Lead VFQFN, E-Pad, Forced Convention

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	29.0°C/W	25.4°C/W	22.7°C/W

Transistor Count

The transistor count for 8V31012 is: 843

48-Lead VFQFN (NL) Package Outline and Package Dimensions

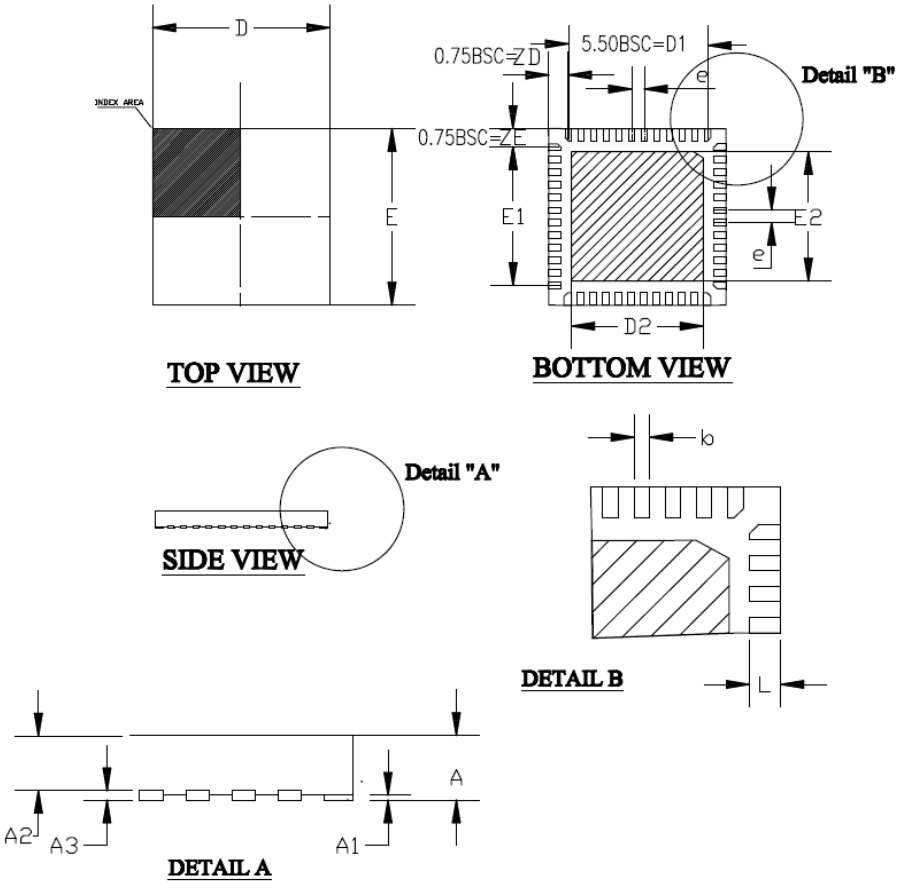


Table 6. Package Dimensions for 48-Lead Package[1]

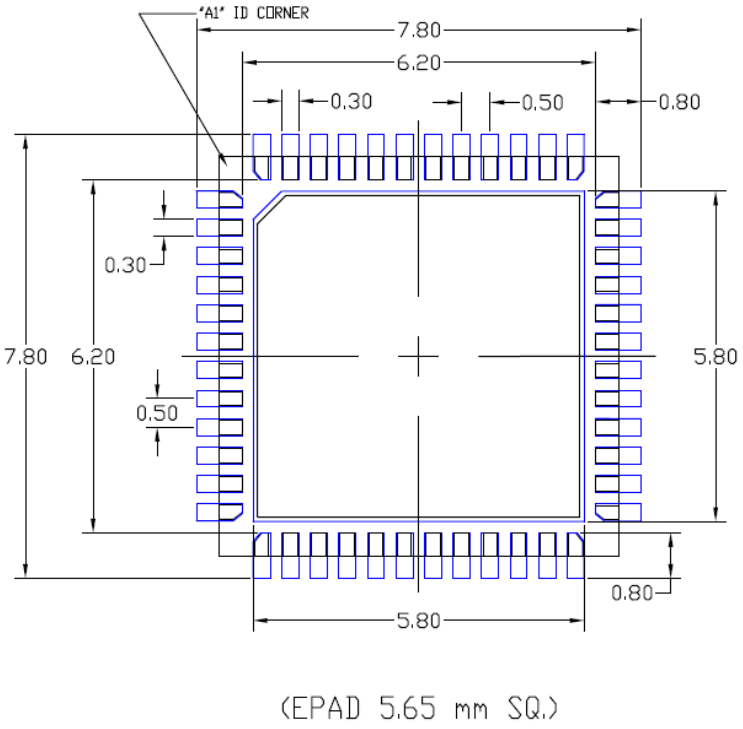
SYMBOL	DIMENSIONS		
	MIN	NOM	MAX
D		7.00 BSC	
E		7.00 BSC	
D2	5.50	5.65	5.80
E2	5.50	5.65	5.80
L	0.35	0.40	0.45
e		0.50 BSC	
N		48	
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.2 REF	
b	0.18	0.25	0.30

NOTE 1. The drawing and dimension data originates from IDT Package Outline Drawing PSC-4203, Rev 04.

All dimensions are in millimeters. All angles are in degrees.

Package Outline and Package Dimensions (Continued)

RECOMMENDED LAND PATTERN



NOTE:

THE RECOMMENDED LAND PATTERN ORIGINATES FROM IDT PACKAGE OUTLINE DRAWING PSC-4203, REV04.

1. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN BLACK.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Ordering Information

Table 7. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8V31012NLGI	IDT8V31012NLGI	48 Lead VFQFN, Lead-Free	Tray	-40°C to 85°C
8V31012NLGI8	IDT8V31012NLGI	48 Lead VFQFN, Lead-Free	Tape & Reel	-40°C to 85°C

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