

Recommended Application:

Serverworks HT2100-based systems using AMD K8 processors

Output Features:

- 7 - Pairs of AMD K8 clocks
- 6 - Pair of SRC/PCI Express* clock
- 3 - 14.318 MHz REF clocks
- 3 - 48MHz clocks
- 2 - PCI 33 MHz clocks
- 2 - 25MHz clocks

Features:

- Spread Spectrum for EMI reduction
- Outputs may be disabled via SMBus
- M/N programming via SMBus

Functionality

| Bit2 FS2 | Bit1 FS1 | Bit0 FS0 | CPU (MHz) |
|-------------|-------------|-------------|--------------|
| 0 | 0 | 0 | Hi-Z |
| 0 | 0 | 1 | X/4 |
| 0 | 1 | 0 | 180.00 |
| 0 | 1 | 1 | 220.00 |
| 1 | 0 | 0 | 100.00 |
| 1 | 0 | 1 | 133.33 |
| 1 | 1 | 0 | 166.67 |
| 1 | 1 | 1 | 200.00 |

Power Groups

| Pin Number | | Description |
|------------|------------|-----------------------|
| VDD | GND | |
| 8 | 12 | 48MHz Clocks |
| 64 | 61 | 25MHz Clocks |
| 15 | 18 | 33 MHz PCI Clocks |
| 21,24 | 22 | IREF, Analog Core |
| 31, 39 | 32 | SRC clocks |
| 55, 49, 41 | 54, 48, 40 | K8 CPU Clocks |
| 3 | 7 | REF Clocks, Xtal Osc. |

Pin Configuration:

| | | | |
|---------------|----|----|-----------|
| X1 | 1 | 64 | VDD25MHz |
| X2 | 2 | 63 | 25MHz_0 |
| VDDREF | 3 | 62 | 25MHz_1 |
| FS0/REF0 | 4 | 61 | GND25MHz |
| FS1/REF1 | 5 | 60 | SPREAD_EN |
| FS2/REF2 | 6 | 59 | CPUCLK8T6 |
| GNDREF | 7 | 58 | CPUCLK8C6 |
| VDD48 | 8 | 57 | CPUCLK8T5 |
| 48MHz_0 | 9 | 56 | CPUCLK8C5 |
| 48MHz_1 | 10 | 55 | VDDCPU |
| 48MHz_2 | 11 | 54 | GND |
| GND48 | 12 | 53 | CPUCLK8T4 |
| SCLK | 13 | 52 | CPUCLK8C4 |
| SDATA | 14 | 51 | CPUCLK8T3 |
| VDDPCI | 15 | 50 | CPUCLK8C3 |
| **FS3/PCICLK0 | 16 | 49 | VDDCPU |
| PCICLK1 | 17 | 48 | GND |
| GNDPCI | 18 | 47 | CPUCLK8T2 |
| PD# | 19 | 46 | CPUCLK8C2 |
| GND | 20 | 45 | CPUCLK8T1 |
| VDDA | 21 | 44 | CPUCLK8C1 |
| GND A | 22 | 43 | CPUCLK8T0 |
| IREF | 23 | 42 | CPUCLK8C0 |
| VDDA | 24 | 41 | VDDCPU |
| SRCCLKT0 | 25 | 40 | GND |
| SRCCLKC0 | 26 | 39 | VDDSRC |
| SRCCLKT1 | 27 | 38 | SRCCLKT5 |
| SRCCLKC1 | 28 | 37 | SRCCLKC5 |
| SRCCLKT2 | 29 | 36 | SRCCLKT4 |
| SRCCLKC2 | 30 | 35 | SRCCLKC4 |
| VDDSRC | 31 | 34 | SRCCLKT3 |
| GNDSRC | 32 | 33 | SRCCLKC3 |

932S805

64-TSSOP

* Internal Pull-Up Resistor

** Internal Pull-Down Resistor

Pin Description

| PIN # | PIN NAME | TYPE | DESCRIPTION |
|-------|---------------|------|---|
| 1 | X1 | IN | Crystal input, Nominally 14.318MHz. |
| 2 | X2 | OUT | Crystal output, Nominally 14.318MHz |
| 3 | VDDREF | PWR | Ref, XTAL power supply, nominal 3.3V |
| 4 | FS0/REF0 | I/O | Frequency select latch input pin / 14.318 MHz reference clock. |
| 5 | FS1/REF1 | I/O | Frequency select latch input pin / 14.318 MHz reference clock. |
| 6 | FS2/REF2 | I/O | Frequency select latch input pin / 14.318 MHz reference clock. |
| 7 | GNDREF | PWR | Ground pin for the REF outputs. |
| 8 | VDD48 | PWR | Power pin for the 48MHz output.3.3V |
| 9 | 48MHz_0 | OUT | 48MHz clock output. |
| 10 | 48MHz_1 | OUT | 48MHz clock output. |
| 11 | 48MHz_2 | OUT | 48MHz clock output. |
| 12 | GND48 | PWR | Ground pin for the 48MHz outputs |
| 13 | SCLK | IN | Clock pin of SMBus circuitry, 5V tolerant. |
| 14 | SDATA | I/O | Data pin for SMBus circuitry, 3.3V tolerant. |
| 15 | VDDPCI | PWR | Power supply for PCI clocks, nominal 3.3V |
| 16 | **FS3/PCICLK0 | I/O | Frequency select latch input pin / 3.3V PCI clock output. |
| 17 | PCICLK1 | OUT | PCI clock output. |
| 18 | GNDPCI | PWR | Ground pin for the PCI outputs |
| 19 | PD# | IN | Asynchronous active low input pin used to power down the device. The internal clocks are disabled and the VCO and the crystal are stopped. |
| 20 | GND | PWR | Ground pin. |
| 21 | VDDA | PWR | 3.3V power for the PLL core. |
| 22 | GNDA | PWR | Ground pin for the PLL core. |
| 23 | IREF | OUT | This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value. |
| 24 | VDDA | PWR | 3.3V power for the PLL core. |
| 25 | SRCCLKT0 | OUT | True clock of differential SRC clock pair. |
| 26 | SRCCLKC0 | OUT | Complement clock of differential SRC clock pair. |
| 27 | SRCCLKT1 | OUT | True clock of differential SRC clock pair. |
| 28 | SRCCLKC1 | OUT | Complement clock of differential push-pull SRC clock pair. |
| 29 | SRCCLKT2 | OUT | True clock of differential SRC clock pair. |
| 30 | SRCCLKC2 | OUT | Complement clock of differential SRC clock pair. |
| 31 | VDDSRC | PWR | Supply for SRC clocks, 3.3V nominal |
| 32 | GNDSRC | PWR | Ground pin for the SRC outputs |

Pin Description (continued)

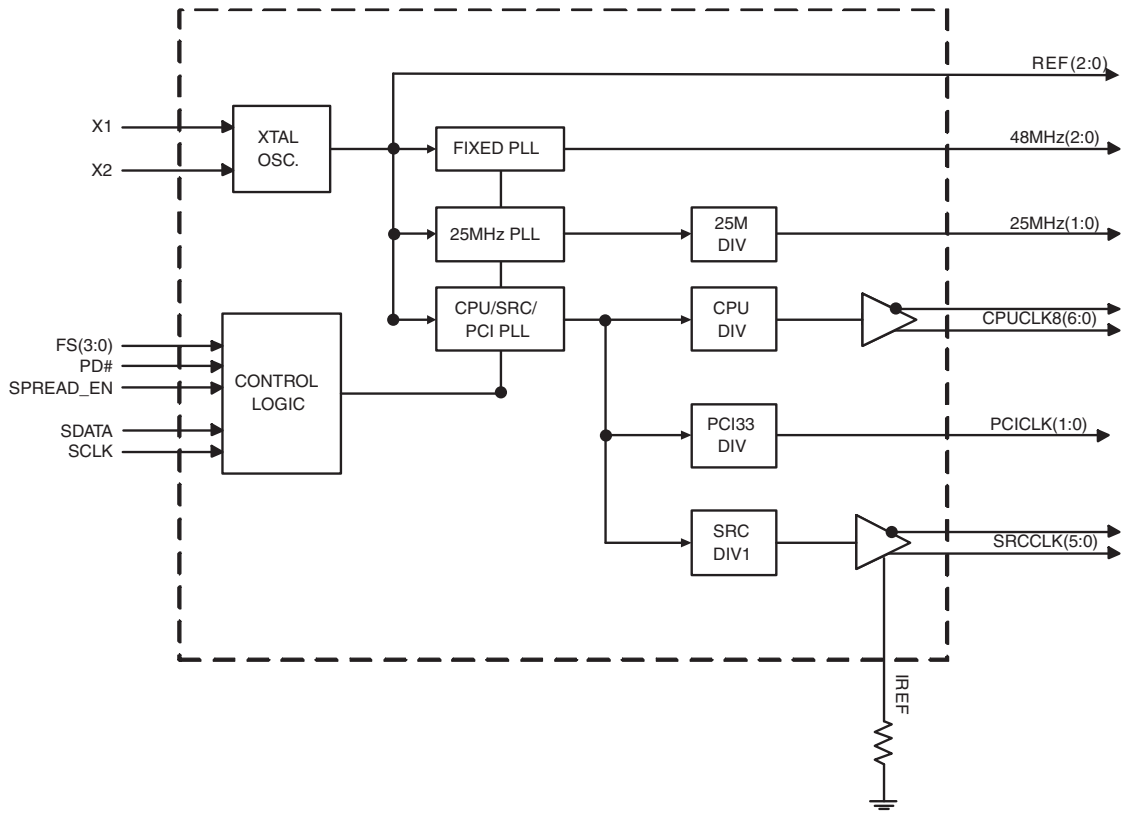
| PIN # | PIN NAME | TYPE | DESCRIPTION |
|-------|-----------|------|--|
| 33 | SRCCLKC3 | OUT | Complement clock of differential SRC clock pair. |
| 34 | SRCCLKT3 | OUT | True clock of differential SRC clock pair. |
| 35 | SRCCLKC4 | OUT | Complement clock of differential SRC clock pair. |
| 36 | SRCCLKT4 | OUT | True clock of differential SRC clock pair. |
| 37 | SRCCLKC5 | OUT | Complement clock of differential SRC clock pair. |
| 38 | SRCCLKT5 | OUT | True clock of differential SRC clock pair. |
| 39 | VDDSRC | PWR | Supply for SRC clocks, 3.3V nominal |
| 40 | GND | PWR | Ground pin. |
| 41 | VDDCPU | PWR | Supply for CPU clocks, 3.3V nominal |
| 42 | CPUCLK8C0 | OUT | Complementary clock of differential 0.8V push-pull K8 pair. |
| 43 | CPUCLK8T0 | OUT | True clock of differential 0.8V push-pull K8 pair. |
| 44 | CPUCLK8C1 | OUT | Complementary clock of differential 0.8V push-pull K8 pair. |
| 45 | CPUCLK8T1 | OUT | True clock of differential 0.8V push-pull K8 pair. |
| 46 | CPUCLK8C2 | OUT | Complementary clock of differential 0.8V push-pull K8 pair. |
| 47 | CPUCLK8T2 | OUT | True clock of differential 0.8V push-pull K8 pair. |
| 48 | GND | PWR | Ground pin. |
| 49 | VDDCPU | PWR | Supply for CPU clocks, 3.3V nominal |
| 50 | CPUCLK8C3 | OUT | Complementary clock of differential 0.8V push-pull K8 pair. |
| 51 | CPUCLK8T3 | OUT | True clock of differential 0.8V push-pull K8 pair. |
| 52 | CPUCLK8C4 | OUT | Complementary clock of differential 0.8V push-pull K8 pair. |
| 53 | CPUCLK8T4 | OUT | True clock of differential 0.8V push-pull K8 pair. |
| 54 | GND | PWR | Ground pin. |
| 55 | VDDCPU | PWR | Supply for CPU clocks, 3.3V nominal |
| 56 | CPUCLK8C5 | OUT | Complementary clock of differential 0.8V push-pull K8 pair. |
| 57 | CPUCLK8T5 | OUT | True clock of differential 0.8V push-pull K8 pair. |
| 58 | CPUCLK8C6 | OUT | Complementary clock of differential 0.8V push-pull K8 pair. |
| 59 | CPUCLK8T6 | OUT | True clock of differential 0.8V push-pull K8 pair. |
| 60 | SPREAD_EN | IN | Asynchronous, active high input to enable spread spectrum functionality. |
| 61 | GND25MHz | PWR | Ground pin for the 25MHz outputs |
| 62 | 25MHz_1 | OUT | 25MHz clock output, 3.3V |
| 63 | 25MHz_0 | OUT | 25MHz clock output, 3.3V |
| 64 | VDD25MHz | PWR | Power supply for 25MHz clocks, 3.3V nominal. |

General Description

The **ICS932S805** is a main clock synthesizer chip that, when paired with ICS9DB108, provides all clocks required by Serverworks HT2100-based servers.

An SMBus interface allows full control of the device.

Block Diagram



Single-ended Terminations

| Single-ended Output Strength | Number of Loads on Board | Series Resistor for Proper Termination | | |
|------------------------------|--------------------------|--|--------------|--------------|
| | | Zo = 50 ohms | Zo = 55 ohms | Zo = 60 ohms |
| 48MHz 1 Load | 1 | 15 | 24 | 30 |
| 48MHz 2 Load | 2 | 4.7 | 15 | 20 |
| 25MHz 1 Load | 1 | 15 | 24 | 30 |
| 25MHz 2 Load | 2 | 4.7 | 15 | 20 |
| PCI 1 Load | 1 | 15 | 24 | 30 |
| PCI 2 Load | 2 | 4.7 | 15 | 20 |
| REF 1 Load | 1 | 15 | 24 | 30 |
| REF 2 Load | 2 | 4.7 | 15 | 20 |

CPU Divider Ratios

| | | Divider (3:2) | | | | | | | |
|---------------|-----|---------------|-----|---------|-----|---------|-----|---------|-----|
| Divider (1:0) | Bit | 00 | | 01 | | 10 | | 11 | MSB |
| | 00 | 0000 | 4 | 0100 | 8 | 1000 | 16 | 1100 | 32 |
| | 01 | 0001 | 3 | 0101 | 6 | 1001 | 12 | 1101 | 24 |
| | 10 | 0010 | 5 | 0110 | 10 | 1010 | 20 | 1110 | 40 |
| | 11 | 0011 | 15 | 0111 | 30 | 1011 | 60 | 1111 | 120 |
| | LSB | Address | Div | Address | Div | Address | Div | Address | Div |

PCI Divider Ratios

| | | Divider (3:2) | | | | | | | |
|---------------|-----|---------------|-----|---------|-----|---------|-----|---------|-----|
| Divider (1:0) | Bit | 00 | | 01 | | 10 | | 11 | MSB |
| | 00 | 0000 | 4 | 0100 | 8 | 1000 | 16 | 1100 | 32 |
| | 01 | 0001 | 3 | 0101 | 6 | 1001 | 12 | 1101 | 24 |
| | 10 | 0010 | 5 | 0110 | 10 | 1010 | 20 | 1110 | 40 |
| | 11 | 0011 | 15 | 0111 | 30 | 1011 | 60 | 1111 | 120 |
| | LSB | Address | Div | Address | Div | Address | Div | Address | Div |

SRC Divider Ratios

| | | Divider (3:2) | | | | | | | |
|---------------|-----|---------------|-----|---------|-----|---------|-----|---------|-----|
| Divider (1:0) | Bit | 00 | | 01 | | 10 | | 11 | MSB |
| | 00 | 0000 | 2 | 0100 | 4 | 1000 | 8 | 1100 | 16 |
| | 01 | 0001 | 3 | 0101 | 6 | 1001 | 12 | 1101 | 24 |
| | 10 | 0010 | 5 | 0110 | 10 | 1010 | 20 | 1110 | 40 |
| | 11 | 0011 | 7 | 0111 | 14 | 1011 | 28 | 1111 | 56 |
| | LSB | Address | Div | Address | Div | Address | Div | Address | Div |

General SMBus serial interface information

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D2_{(h)}$
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) sends the data byte count = X
- ICS clock will **acknowledge**
- Controller (host) starts sending **Byte N through Byte N + X - 1**
- ICS clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address $D2_{(h)}$
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address $D3_{(h)}$
- ICS clock will **acknowledge**
- ICS clock will send the data byte count = X
- ICS clock sends **Byte N + X - 1**
- ICS clock sends **Byte 0 through byte X (if $X_{(n)}$ was written to byte 8).**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Write Operation | | | |
|-----------------------------|-----------|----------------------|-----|
| Controller (Host) | | ICS (Slave/Receiver) | |
| T | starT bit | | |
| Slave Address $D2_{(h)}$ | | | |
| WR | WRite | | |
| | | ACK | |
| Beginning Byte = N | | | |
| | | ACK | |
| Data Byte Count = X | | | |
| | | ACK | |
| Beginning Byte N | | X Byte | |
| | ◊ | | ACK |
| | ◊ | | ◊ |
| | ◊ | | ◊ |
| | ◊ | | ◊ |
| Byte N + X - 1 | | | |
| | | ACK | |
| P | stoP bit | | |

| Index Block Read Operation | | | |
|----------------------------|-----------------|----------------------|------------------|
| Controller (Host) | | ICS (Slave/Receiver) | |
| T | starT bit | | |
| Slave Address $D2_{(h)}$ | | | |
| WR | WRite | | |
| | | ACK | |
| Beginning Byte = N | | | |
| | | ACK | |
| RT | Repeat starT | | |
| Slave Address $D3_{(h)}$ | | | |
| RD | ReaD | | |
| | | ACK | |
| | | Data Byte Count = X | |
| ACK | | | |
| ACK | | X Byte | |
| | | | Beginning Byte N |
| ◊ | | | ◊ |
| ◊ | | | ◊ |
| ◊ | | | ◊ |
| | | Byte N + X - 1 | |
| N | Not acknowledge | | |
| P | stoP bit | | |

SMBus Table: Frequency Select and Spread Control Register

| Byte 0 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|--------|-------|------------------------|--|------|--------------------------------|----------|---------|
| Bit 7 | - | FS Source | Latched Input or SMBus Frequency Select | RW | Latched Inputs | SMBus | 0 |
| Bit 6 | - | Spread Spectrum Enable | Spread Enable for CPU, SRC and PCI Outputs. Setting SPREAD_EN pin to '1', forces Spread ON and overrides this bit. | RW | OFF | ON | 0 |
| Bit 5 | - | Reserved | Reserved | RW | Reserved | Reserved | 0 |
| Bit 4 | - | Reserved | Reserved | RW | Reserved | Reserved | 0 |
| Bit 3 | - | FS3 | Freq Select Bit 3 | RW | See CPU Frequency Select Table | | Latched |
| Bit 2 | - | FS2 | Freq Select Bit 2 | RW | | | Latched |
| Bit 1 | - | FS1 | Freq Select Bit 1 | RW | | | Latched |
| Bit 0 | - | FS0 | Freq Select Bit 0 | RW | | | Latched |

SMBus Table: Output Control Register

| Byte 1 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|--------|-------|---------|------------------|------|---------------|--------|-----|
| Bit 7 | 6 | REF2 | Output Enable | RW | Disable (Low) | Enable | 1 |
| Bit 6 | 5 | REF1 | Output Enable | RW | Disable (Low) | Enable | 1 |
| Bit 5 | 4 | REF0 | Output Enable | RW | Disable (Low) | Enable | 1 |
| Bit 4 | 17 | PCICLK1 | Output Enable | RW | Disable (Low) | Enable | 1 |
| Bit 3 | 16 | PCICLK0 | Output Enable | RW | Disable (Low) | Enable | 1 |
| Bit 2 | 11 | 48MHz_2 | Output Enable | RW | Disable (Low) | Enable | 1 |
| Bit 1 | 10 | 48MHz_1 | Output Enable | RW | Disable (Low) | Enable | 1 |
| Bit 0 | 9 | 48MHz_0 | Output Enable | RW | Disable (Low) | Enable | 1 |

SMBus Table: Output Control Register

| Byte 2 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|--------|-------|------------|--|------|----------|----------|-----|
| Bit 7 | - | Reserved | Reserved | RW | Reserved | Reserved | 0 |
| Bit 6 | 59/58 | CPUCLK8(6) | Output Enable When Disabled CPUCLKT = 0 CPUCLKC = 1 | RW | Disable | Enable | 1 |
| Bit 5 | 57/56 | CPUCLK8(5) | | RW | Disable | Enable | 1 |
| Bit 4 | 53/52 | CPUCLK8(4) | | RW | Disable | Enable | 1 |
| Bit 3 | 51/50 | CPUCLK8(3) | | RW | Disable | Enable | 1 |
| Bit 2 | 47/46 | CPUCLK8(2) | | RW | Disable | Enable | 1 |
| Bit 1 | 45/44 | CPUCLK8(1) | | RW | Disable | Enable | 1 |
| Bit 0 | 43/42 | CPUCLK8(0) | | RW | Disable | Enable | 1 |

SMBus Table: Output Control Register

| Byte 3 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|--------|----------|-----------|------------------------------|------|----------------|----------|-----|
| Bit 7 | SRC CLKs | SRCCLK PD | SRCCLK Power Down Drive Mode | RW | Driven | Hi-Z | 0 |
| Bit 6 | - | Reserved | Reserved | RW | Reserved | Reserved | 0 |
| Bit 5 | 38/37 | SRCCLK5 | Output Enable | RW | Disable (Hi-Z) | Enable | 1 |
| Bit 4 | 36/35 | SRCCLK4 | Output Enable | RW | Disable (Hi-Z) | Enable | 1 |
| Bit 3 | 34/33 | SRCCLK3 | Output Enable | RW | Disable (Hi-Z) | Enable | 1 |
| Bit 2 | 29/30 | SRCCLK2 | Output Enable | RW | Disable (Hi-Z) | Enable | 1 |
| Bit 1 | 27/28 | SRCCLK1 | Output Enable | RW | Disable (Hi-Z) | Enable | 1 |
| Bit 0 | 25/26 | SRCCLK0 | Output Enable | RW | Disable (Hi-Z) | Enable | 1 |

SMBus Table: Drive Strength Control Register

| Byte 4 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|--------|-------|---------|-----------------------|------|--------|---------|-----|
| Bit 7 | 6 | REF2 | Drive Strength Select | RW | 1 Load | 2 Loads | 1 |
| Bit 6 | 5 | REF1 | Drive Strength Select | RW | 1 Load | 2 Loads | 1 |
| Bit 5 | 4 | REF0 | Drive Strength Select | RW | 1 Load | 2 Loads | 1 |
| Bit 4 | 17 | PCICLK1 | Drive Strength Select | RW | 1 Load | 2 Loads | 1 |
| Bit 3 | 16 | PCICLK0 | Drive Strength Select | RW | 1 Load | 2 Loads | 1 |
| Bit 2 | 11 | 48MHz_2 | Drive Strength Select | RW | 1 Load | 2 Loads | 1 |
| Bit 1 | 10 | 48MHz_1 | Drive Strength Select | RW | 1 Load | 2 Loads | 1 |
| Bit 0 | 9 | 48MHz_0 | Drive Strength Select | RW | 1 Load | 2 Loads | 1 |

SMBus Table: SRC Frequency Select Register

| Byte 5 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|--------|-------|----------|-----------------------|------|---------------|----------|-----|
| Bit 7 | 62 | 25MHz_1 | Output Enable | RW | Disable (Low) | Enable | 1 |
| Bit 6 | 63 | 25MHz_0 | Output Enable | RW | Disable (Low) | Enable | 1 |
| Bit 5 | 62 | 25MHz_1 | Drive Strength Select | RW | 1 Load | 2 Loads | 1 |
| Bit 4 | 63 | 25MHz_0 | Drive Strength Select | RW | 1 Load | 2 Loads | 1 |
| Bit 3 | - | Reserved | Reserved | RW | Reserved | Reserved | 0 |
| Bit 2 | - | Reserved | Reserved | RW | Reserved | Reserved | 0 |
| Bit 1 | - | Reserved | Reserved | RW | Reserved | Reserved | 0 |
| Bit 0 | - | Reserved | Reserved | RW | Reserved | Reserved | 0 |

SMBus Table: Device ID Register

| Byte 6 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|--------|-------|---------|------------------|------|---|---|-----|
| Bit 7 | - | DevID 7 | Device ID MSB | R | - | - | 1 |
| Bit 6 | - | DevID 6 | Device ID 6 | R | - | - | 0 |
| Bit 5 | - | DevID 5 | Device ID 5 | R | - | - | 0 |
| Bit 4 | - | DevID 4 | Device ID4 | R | - | - | 0 |
| Bit 3 | - | DevID 3 | Device ID3 | R | - | - | 0 |
| Bit 2 | - | DevID 2 | Device ID2 | R | - | - | 1 |
| Bit 1 | - | DevID 1 | Device ID1 | R | - | - | 0 |
| Bit 0 | - | DevID 0 | Device ID LSB | R | - | - | 1 |

SMBus Table: Vendor ID Register

| Byte 7 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|--------|-------|------|---------------------------|------|---|---|-----|
| Bit 7 | - | RID3 | Revision ID | R | - | - | X |
| Bit 6 | - | RID2 | | R | - | - | X |
| Bit 5 | - | RID1 | | R | - | - | X |
| Bit 4 | - | RID0 | | R | - | - | X |
| Bit 3 | - | VID3 | VENDOR ID (0001 = ICS) | R | - | - | 0 |
| Bit 2 | - | VID2 | | R | - | - | 0 |
| Bit 1 | - | VID1 | | R | - | - | 0 |
| Bit 0 | - | VID0 | | R | - | - | 1 |

SMBus Table: Byte Count Register

| Byte 8 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|--------|-------|------|-------------------------------|------|--|---|-----|
| Bit 7 | - | BC7 | Byte Count Programming b(7:0) | RW | Writing to this register will configure how many bytes will be read back, default is 9 bytes. | | 0 |
| Bit 6 | - | BC6 | | RW | | | 0 |
| Bit 5 | - | BC5 | | RW | | | 0 |
| Bit 4 | - | BC4 | | RW | | | 0 |
| Bit 3 | - | BC3 | | RW | | | 1 |
| Bit 2 | - | BC2 | | RW | | | 0 |
| Bit 1 | - | BC1 | | RW | | | 0 |
| Bit 0 | - | BC0 | | RW | | | 1 |

SMBus Table: Reserved Register

| Byte 9 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|--------|-------|----------|------------------|------|----------|----------|-----|
| Bit 7 | - | Reserved | Reserved | RW | Reserved | Reserved | 0 |
| Bit 6 | - | Reserved | Reserved | RW | Reserved | Reserved | 0 |
| Bit 5 | - | Reserved | Reserved | RW | Reserved | Reserved | 0 |
| Bit 4 | - | Reserved | Reserved | RW | Reserved | Reserved | 0 |
| Bit 3 | - | Reserved | Reserved | RW | Reserved | Reserved | 0 |
| Bit 2 | - | Reserved | Reserved | RW | Reserved | Reserved | 0 |
| Bit 1 | - | Reserved | Reserved | RW | Reserved | Reserved | 0 |
| Bit 0 | - | Reserved | Reserved | RW | Reserved | Reserved | 0 |

SMBus Table: M/N Programming Enable

| Byte 10 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---------|-------|----------|--------------------------------|------|---------|--------|-----|
| Bit 7 | - | M/N_EN | CPU PLL M/N Programming Enable | RW | Disable | Enable | 0 |
| Bit 6 | - | Reserved | Reserved | RW | - | - | 0 |
| Bit 5 | - | Reserved | Reserved | RW | - | - | 0 |
| Bit 4 | - | Reserved | Reserved | RW | - | - | 0 |
| Bit 3 | - | Reserved | Reserved | RW | - | - | 0 |
| Bit 2 | - | Reserved | Reserved | RW | - | - | 0 |
| Bit 1 | - | Reserved | Reserved | RW | - | - | 0 |
| Bit 0 | - | Reserved | Reserved | RW | - | - | 0 |

Bytes 11:14 Are Reserved

SMBus Table: CPU/SRC Frequency Control Register

| Byte 15 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---------|-------|--------|---------------------------------|------|--|---|-----|
| Bit 7 | - | N Div8 | N Divider Prog bit 8 | RW | The decimal representation of M and N Divier in Byte 15 and 16 will configure the CPU VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2] | | X |
| Bit 6 | - | N Div9 | N Divider Prog bit 9 | RW | | | X |
| Bit 5 | - | M Div5 | M Divider Programming bit (5:0) | RW | | | X |
| Bit 4 | - | M Div4 | | RW | | | X |
| Bit 3 | - | M Div3 | | RW | | | X |
| Bit 2 | - | M Div2 | | RW | | | X |
| Bit 1 | - | M Div1 | | RW | | | X |
| Bit 0 | - | M Div0 | | RW | | | X |

SMBus Table: CPU/SRC Frequency Control Register

| Byte 16 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---------|-------|--------|---|------|--|---|-----|
| Bit 7 | - | N Div7 | N Divider Programming Byte12 bit(7:0) and Byte11 bit(7:6) | RW | The decimal representation of M and N Divier in Byte 15 and 16 will configure the CPU VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2] | | X |
| Bit 6 | - | N Div6 | | RW | | | X |
| Bit 5 | - | N Div5 | | RW | | | X |
| Bit 4 | - | N Div4 | | RW | | | X |
| Bit 3 | - | N Div3 | | RW | | | X |
| Bit 2 | - | N Div2 | | RW | | | X |
| Bit 1 | - | N Div1 | | RW | | | X |
| Bit 0 | - | N Div0 | | RW | | | X |

SMBus Table: CPU/SRC Spread Spectrum Control Register

| Byte 17 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---------|-------|------|--------------------------------------|------|---|---|-----|
| Bit 7 | - | SSP7 | Spread Spectrum Programming bit(7:0) | RW | These Spread Spectrum bits in Byte 17 and 18 will program the spread percentage of CPU and SRC outputs. | | X |
| Bit 6 | - | SSP6 | | RW | | | X |
| Bit 5 | - | SSP5 | | RW | | | X |
| Bit 4 | - | SSP4 | | RW | | | X |
| Bit 3 | - | SSP3 | | RW | | | X |
| Bit 2 | - | SSP2 | | RW | | | X |
| Bit 1 | - | SSP1 | | RW | | | X |
| Bit 0 | - | SSP0 | | RW | | | X |

SMBus Table: CPU/SRC Spread Spectrum Control Register

| Byte 18 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---------|-------|----------|--|------|---|---|-----|
| Bit 7 | - | Reserved | Reserved | R | - | - | 0 |
| Bit 6 | - | SSP14 | Spread Spectrum Programming bit(14:8) | RW | These Spread Spectrum bits in Byte 17 and 18 will program the spread percentage of CPU and SRC outputs. | | X |
| Bit 5 | - | SSP13 | | RW | | | X |
| Bit 4 | - | SSP12 | | RW | | | X |
| Bit 3 | - | SSP11 | | RW | | | X |
| Bit 2 | - | SSP10 | | RW | | | X |
| Bit 1 | - | SSP9 | | RW | | | X |
| Bit 0 | - | SSP8 | | RW | | | X |

SMBus Table: SRC Spread Spectrum Control Register

| Byte 18 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---------|-------|----------|------------------|------|---|---|-----|
| Bit 7 | - | Reserved | Reserved | R | - | - | 0 |
| Bit 6 | - | Reserved | Reserved | R | - | - | 0 |
| Bit 5 | - | Reserved | Reserved | R | - | - | 0 |
| Bit 4 | - | Reserved | Reserved | R | - | - | 0 |
| Bit 3 | - | Reserved | Reserved | R | - | - | 0 |
| Bit 2 | - | Reserved | Reserved | R | - | - | 0 |
| Bit 1 | - | Reserved | Reserved | R | - | - | 0 |
| Bit 0 | - | Reserved | Reserved | R | - | - | 0 |

SMBus Table: Programmable Output Divider Register

| Byte 19 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---------|-------|----------|------------------------------------|------|---------------------------------|---|-----|
| Bit 7 | - | CPUDiv3 | CPU Divider Ratio Programming Bits | RW | See CPU Divider Ratios Table | | X |
| Bit 6 | - | CPUDiv2 | | RW | | | X |
| Bit 5 | - | CPUDiv1 | | RW | | | X |
| Bit 4 | - | CPUDiv0 | | RW | | | X |
| Bit 3 | - | Reserved | Reserved | R | - | - | 0 |
| Bit 2 | - | Reserved | Reserved | R | - | - | 0 |
| Bit 1 | - | Reserved | Reserved | R | - | - | 0 |
| Bit 0 | - | Reserved | Reserved | R | - | - | 0 |

SMBus Table: Programmable Output Divider Register

| Byte 20 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---------|-------|-----------|---|------|---------------------------|---|-----|
| Bit 7 | - | 33MHzDiv3 | 33MHz Divider Ratio Programming Bits | RW | 33MHz Divider Ratio Table | | X |
| Bit 6 | - | 33MHzDiv2 | | RW | | | X |
| Bit 5 | - | 33MHzDiv1 | | RW | | | X |
| Bit 4 | - | 33MHzDiv0 | | RW | | | X |
| Bit 3 | - | SRC_Div3 | SRC_ Divider Ratio Programming Bits | RW | SRC Divider Ratio Table | | X |
| Bit 2 | - | SRC_Div2 | | RW | | | X |
| Bit 1 | - | SRC_Div1 | | RW | | | X |
| Bit 0 | - | SRC_Div0 | | RW | | | X |

SMBusTable: Reserved Regsiter

Byte 21 is reserved do not write this register!

Absolute Maximum Ratings

| Symbol | Parameter | Min | Max | Units |
|----------|---------------------------------------|-----------|------------|-------|
| VDD_A | 3.3V Core Supply Voltage | - | VDD + 0.5V | V |
| VDD_In | 3.3V Logic Input Supply Voltage | GND - 0.5 | VDD + 0.5V | V |
| Ts | Storage Temperature | -65 | 150 | °C |
| Tambient | Ambient Operating Temp | 0 | 70 | °C |
| Tc | Case Temperature | - | 115 | °C |
| ESD prot | Input ESD protection human body model | 2000 | - | V |

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5%

| PARAMETER | SYMBOL | Conditions | MIN | TYP | MAX | UNITS | NOTES |
|--|----------------------|---|-----------------------|--------|-----------------------|-------|-------|
| Input High Voltage | V _{IH} | 3.3 V +/-5% | 2 | | V _{DD} + 0.3 | V | 1 |
| Input Low Voltage | V _{IL} | 3.3 V +/-5% | V _{SS} - 0.3 | | 0.8 | V | 1 |
| Input High Current | I _{IH} | V _{IN} = V _{DD} | -5 | | 5 | uA | 1 |
| Input Low Current | I _{IL1} | V _{IN} = 0 V; Inputs with no pull-up resistors | -5 | | | uA | 1 |
| | I _{IL2} | V _{IN} = 0 V; Inputs with pull-up resistors | -200 | | | uA | 1 |
| Operating Supply Current | I _{DD3.3OP} | Full Active, C _L = Full load; | | 258 | 350 | mA | |
| Operating Current | I _{DD3.3OP} | all outputs driven | | | tbd | mA | |
| Powerdown Current | I _{DD3.3PD} | all diff pairs driven | | | tbd | mA | |
| | | all differential pairs tri-stated | | | tbd | mA | |
| Input Frequency ³ | F _i | V _{DD} = 3.3 V | | 14.318 | | MHz | 3 |
| Pin Inductance ¹ | L _{pin} | | | | 7 | nH | 1 |
| Input Capacitance ¹ | C _{IN} | Logic Inputs | | | 5 | pF | 1 |
| | C _{OUT} | Output pin capacitance | | | 6 | pF | 1 |
| | C _{INX} | X1 & X2 pins | | | 5 | pF | 1 |
| Clk Stabilization ^{1,2} | T _{STAB} | From V _{DD} Power-Up or de-assertion of PD# to 1st clock | | | 3 | ms | 1,2 |
| Modulation Frequency | | Triangular Modulation | 30 | | 33 | kHz | 1 |
| SMBus Voltage | V _{DD} | | 2.7 | | 5.5 | V | 1 |
| Low-level Output Voltage | V _{OL} | @ I _{PULLUP} | | | 0.4 | V | 1 |
| Current sinking at V _{OL} = 0.4 | I _{PULLUP} | | 4 | | | mA | 1 |
| SCLK/SDATA Clock/Data Rise Time ³ | T _{RI2C} | (Max V _{IL} - 0.15) to (Min V _{IH} + 0.15) | | | 1000 | ns | 1 |
| SCLK/SDATA Clock/Data Fall Time ³ | T _{FI2C} | (Min V _{IH} + 0.15) to (Max V _{IL} - 0.15) | | | 300 | ns | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

²See timing diagrams for timing requirements.

³Input frequency should be measured at the REFOUT pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.

Electrical Characteristics - K8 Push Pull Differential Pair

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{ V} \pm 5\%$; $C_L = \text{AMD64 Processor Test Load}$

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------------------|-----------------------|--|-------|------|------|----------|-------|
| Rising Edge Rate | $\delta V/\delta t$ | Measured at the AMD64 processor's test load. 0 V +/- 400 mV (differential measurement) | 2 | | 10 | V/ns | 1 |
| Falling Edge Rate | $\delta V/\delta t$ | | 2 | | 10 | V/ns | 1 |
| Differential Voltage | V_{DIFF} | Measured at the AMD64 processor's test load. (single-ended measurement) | 0.4 | 1.25 | 2.3 | V | 1 |
| Change in V_{DIFF_DC} Magnitude | ΔV_{DIFF} | | -150 | | 150 | mV | 1 |
| Common Mode Voltage | V_{CM} | | 1.05 | 1.25 | 1.45 | V | 1 |
| Change in Common Mode Voltage | ΔV_{CM} | | -200 | | 200 | mV | 1 |
| Jitter, Cycle to cycle | $t_{j\text{cyc-cyc}}$ | Measurement from differential waveform. Maximum difference of cycle time between 2 adjacent cycles. | 0 | 100 | 200 | ps | 1 |
| Jitter, Accumulated | t_{ja} | Measured using the JIT2 software package with a Tek 7404 scope. TIE (Time Interval Error) measurement technique: Sample resolution = 50 ps, Sample Duration = 10 μs | -1000 | | 1000 | | 1,2,3 |
| Duty Cycle | d_{13} | Measurement from differential waveform | 45 | | 53 | % | 1 |
| Output Impedance | R_{ON} | Average value during switching transition. Used for determining series termination value. | 15 | 35 | 55 | Ω | 1 |
| Group Skew | $t_{src-skew}$ | Measurement from differential waveform | | | 250 | ps | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

²All accumulated jitter specifications are guaranteed assuming that REF is at 14.31818MHz

³Spread Spectrum is off

Electrical Characteristics - SRC 0.7V Current Mode Differential Pair

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{ V} \pm 5\%$; $C_L = 2\text{pF}$, $R_S = 33.2\Omega$, $R_P = 49.9\Omega$, $I_{REF} = 475\Omega$

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---------------------------------|-----------------------|--|---------|---------|---------|----------|-------|
| Current Source Output Impedance | Zo | $V_O = V_x$ | 3000 | | | Ω | 1 |
| Voltage High | VHigh | Statistical measurement on single ended signal using oscilloscope math function. | 660 | | 850 | mV | 1,3 |
| Voltage Low | VLow | | -150 | | 150 | | |
| Max Voltage | Vovs | Measurement on single ended signal using absolute value. | | | 1150 | mV | 1 |
| Min Voltage | Vuds | | -300 | | | | 1 |
| Crossing Voltage (abs) | Vcross(abs) | | 250 | 350 | 550 | mV | 1 |
| Crossing Voltage (var) | d-Vcross | Variation of crossing over all edges | | 12 | 140 | mV | 1 |
| Long Accuracy | ppm | see Tperiod min-max values | -300 | | 300 | ppm | 1,2 |
| Average period | Tperiod | 75.00 MHz nominal | 8.5684 | 8.5714 | 8.5744 | ns | 2 |
| | | 75.00 MHz spread | 8.5684 | | 8.6244 | ns | 2 |
| | | 100.00 MHz nominal | 9.9970 | 10.0000 | 10.0030 | ns | 2 |
| | | 100.00 MHz spread | 9.9970 | | 10.0530 | ns | 2 |
| | | 116.67 MHz nominal | 13.3303 | 13.3333 | 13.3363 | ns | 2 |
| | | 116.67 MHz spread | 13.3303 | | 13.3863 | ns | 2 |
| | | 133.33 MHz nominal | 7.4972 | 7.5002 | 7.5032 | ns | 2 |
| Absolute min period | Tabsm | @ 100.00MHz nominal/spread | 9.8720 | | | ns | 1,2 |
| Rise Time | t _r | $V_{OL} = 0.175\text{V}$, $V_{OH} = 0.525\text{V}$ | 175 | | 700 | ps | 1 |
| Fall Time | t _f | $V_{OH} = 0.525\text{V}$, $V_{OL} = 0.175\text{V}$ | 175 | | 700 | ps | 1 |
| Rise Time Variation | d-t _r | | | 30 | 125 | ps | 1 |
| Fall Time Variation | d-t _f | | | 30 | 125 | ps | 1 |
| Duty Cycle | d ₁₃ | Measurement from differential waveform | 45 | | 55 | % | 1 |
| Group Skew | t _{src-skew} | Measurement from differential waveform | | | 250 | ps | |
| Jitter, Cycle to cycle | t _{jcc-cyc} | Measurement from differential waveform | | | 125 | ps | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

²All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF is at 14.31818MHz

³ $I_{REF} = V_{DD}/(3xR_R)$. For $R_R = 475\Omega$ (1%), $I_{REF} = 2.32\text{mA}$. $I_{OH} = 6 \times I_{REF}$ and $V_{OH} = 0.7\text{V}$ @ $Z_O = 50\Omega$.

Electrical Characteristics - 33 MHz PCICLK, 25MHz Outputs

$T_A = 0 - 70^\circ\text{C}$; $V_{DD}=3.3\text{V} \pm 5\%$; $C_L = 5 \text{ pF}$ (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | Notes |
|------------------------|-----------------------|--|---------|-----|---------|-------|-------|
| PCI Long Accuracy | ppm | see Tperiod min-max values | -300 | | 300 | ppm | 1,2 |
| PCI Clock period | T_{period} | 33.33MHz output nominal | 29.9910 | | 30.0090 | ns | 2 |
| | | 33.33MHz output spread | 29.9910 | | 30.1598 | ns | 2 |
| 25MHz Long Accuracy | ppm | see Tperiod min-max values | -100 | | 100 | ns | 2 |
| 25MHz Clock period | T_{period} | 25MHz output nominal | 0.0000 | | 0.0000 | ns | 2 |
| Output High Voltage | V_{OH} | $I_{\text{OH}} = -1 \text{ mA}$ | 2.4 | | | V | 1 |
| Output Low Voltage | V_{OL} | $I_{\text{OL}} = 1 \text{ mA}$ | | | 0.55 | V | 1 |
| Output High Current | I_{OH} | $V_{\text{OH}} @ \text{MIN} = 1.0 \text{ V}$ | -33 | | | mA | 1 |
| | | $V_{\text{OH}} @ \text{MAX} = 3.135 \text{ V}$ | | | -33 | mA | 1 |
| Output Low Current | I_{OL} | $V_{\text{OL}} @ \text{MIN} = 1.95 \text{ V}$ | 30 | | | mA | 1 |
| | | $V_{\text{OL}} @ \text{MAX} = 0.4 \text{ V}$ | | | 38 | mA | 1 |
| Edge Rate | $\delta V/\delta t$ | Rising edge rate | 1 | | 4 | V/ns | 1 |
| Edge Rate | $\delta V/\delta t$ | Falling edge rate | 1 | | 4 | V/ns | 1 |
| Duty Cycle | d_{t1} | $V_T = 1.5 \text{ V}$ | 45 | | 55 | % | 1 |
| PCI Skew | t_{sk1} | $V_T = 1.5 \text{ V}$ | | | 250 | ps | 1 |
| 25MHz Skew | t_{sk1} | $V_T = 1.5 \text{ V}$ | | | 250 | ps | 1 |
| Jitter, Cycle to cycle | $t_{\text{jycy-cyc}}$ | $V_T = 1.5 \text{ V}$ | | | 250 | ps | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

²All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF is at 14.31818MHz

Electrical Characteristics - 48MHz

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3 \text{ V} \pm 5\%$; $C_L = 5 \text{ pF}$ (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | Notes |
|------------------------|-----------------------|--|---------|-----|---------|-------|-------|
| Long Accuracy | ppm | see Tperiod min-max values | -100 | | 100 | ppm | 1,2 |
| Clock period | T_{period} | 48.00MHz output nominal | 20.8257 | | 20.8340 | ns | 2 |
| Output High Voltage | V_{OH} | $I_{\text{OH}} = -1 \text{ mA}$ | 2.4 | | | V | 1 |
| Output Low Voltage | V_{OL} | $I_{\text{OL}} = 1 \text{ mA}$ | | | 0.55 | V | 1 |
| Output High Current | I_{OH} | $V_{\text{OH}} @ \text{MIN} = 1.0 \text{ V}$ | -33 | | | mA | 1 |
| | | $V_{\text{OH}} @ \text{MAX} = 3.135 \text{ V}$ | | | -33 | mA | 1 |
| Output Low Current | I_{OL} | $V_{\text{OL}} @ \text{MIN} = 1.95 \text{ V}$ | 30 | | | mA | 1 |
| | | $V_{\text{OL}} @ \text{MAX} = 0.4 \text{ V}$ | | | 38 | mA | 1 |
| Edge Rate | $\delta V/\delta t$ | Rising edge rate | 1 | | 2 | V/ns | 1 |
| Edge Rate | $\delta V/\delta t$ | Falling edge rate | 1 | | 2 | V/ns | 1 |
| Duty Cycle | d_{t1} | $V_T = 1.5 \text{ V}$ | 45 | | 55 | % | 1 |
| Group Skew | t_{sk1} | $V_T = 1.5 \text{ V}$ | | | 250 | ps | 1 |
| Jitter, Cycle to cycle | $t_{\text{jycy-cyc}}$ | $V_T = 1.5 \text{ V}$ | | | 150 | ps | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

²All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF is at 14.31818MHz

Electrical Characteristics - REF-14.318MHz

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{ V} \pm 5\%$; $C_L = 5\text{ pF}$ (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | Notes |
|------------------------|-----------------------|--|---------|-----|---------|-------|-------|
| Long Accuracy | ppm | see Tperiod min-max values | -300 | | 300 | ppm | 1 |
| Clock period | T_{period} | 14.318MHz output nominal | 69.8270 | | 69.8550 | ns | 2 |
| Output High Voltage | V_{OH} | $I_{OH} = -1\text{ mA}$ | 2.4 | | | V | 1 |
| Output Low Voltage | V_{OL} | $I_{OL} = 1\text{ mA}$ | | | 0.4 | V | 1 |
| Output High Current | I_{OH} | $V_{OH} @\text{MIN} = 1.0\text{ V}$, $I_{OH} @\text{MAX} = 3.135\text{ V}$ | -29 | | -23 | mA | 1 |
| Output Low Current | I_{OL} | $V_{OL} @\text{MIN} = 1.95\text{ V}$, $I_{OL} @\text{MAX} = 0.4\text{ V}$ | 29 | | 27 | mA | 1 |
| Edge Rate | $\delta V/\delta t$ | Rising edge rate | 1 | | 2 | V/ns | 1 |
| Edge Rate | $\delta V/\delta t$ | Falling edge rate | 1 | | 2 | V/ns | 1 |
| Skew | t_{sk1} | $V_T = 1.5\text{ V}$ | | | 500 | ps | 1 |
| Duty Cycle | d_{t1} | $V_T = 1.5\text{ V}$ | 45 | | 55 | % | 1 |
| Jitter, Cycle to cycle | $t_{j\text{cyc-cyc}}$ | $V_T = 1.5\text{ V}$ | | | 1000 | ps | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

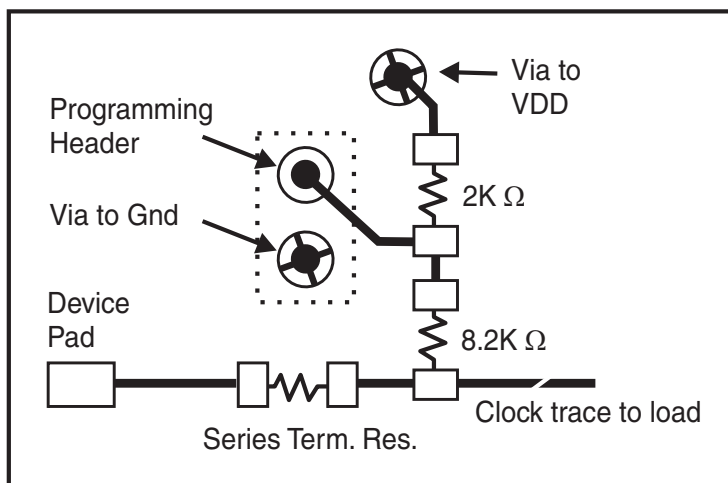
²All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF is at 14.31818MHz

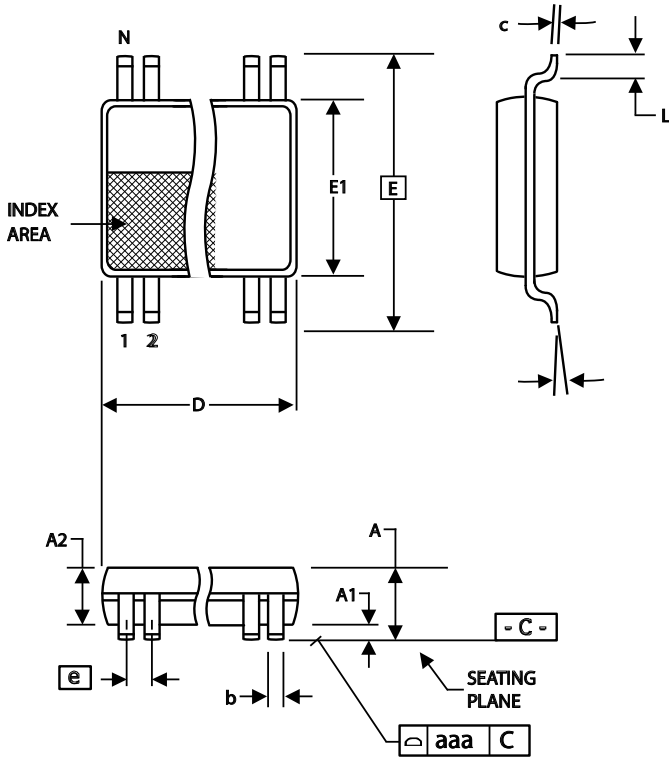
Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the **ICS932S805** serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.





6.10 mm. Body, 0.50 mm. Pitch TSSOP
(240 mil) (20 mil)

| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|----------|-------------------------------------|------|--------------------------------|------|
| | MIN | MAX | MIN | MAX |
| A | -- | 1.20 | -- | .047 |
| A1 | 0.05 | 0.15 | .002 | .006 |
| A2 | 0.80 | 1.05 | .032 | .041 |
| b | 0.17 | 0.27 | .007 | .011 |
| c | 0.09 | 0.20 | .0035 | .008 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 8.10 BASIC | | 0.319 BASIC | |
| E1 | 6.00 | 6.20 | .236 | .244 |
| e | 0.50 BASIC | | 0.020 BASIC | |
| L | 0.45 | 0.75 | .018 | .030 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| α | 0° | 8° | 0° | 8° |
| aaa | -- | 0.10 | -- | .004 |

VARIATIONS

| N | D mm. | | D (inch) | |
|----|-------|-------|----------|------|
| | MIN | MAX | MIN | MAX |
| 64 | 16.90 | 17.10 | .665 | .673 |

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

Ordering Information

| Part/Order Number | Shipping Packaging | Package | Temperature |
|-------------------|--------------------|--------------|-------------|
| 932S805CGLF | Tubes | 64-pin TSSOP | 0 to 70° C |
| 932S805CGLFT | Tape and Reel | 64-pin TSSOP | 0 to 70° C |

“LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

“C” is the device revision designator (will not correlate with the datasheet revision)

Revision History

| Rev. | Issue Date | Description | Page # |
|------|------------|--|----------|
| A | 2/21/2008 | 1. Corrected Byte0 bits 7:6. They are no longer reserved. 2. Corrected SMBUS CPU PLL programming registers (Moved from Bytes 11:14 to Bytes 15:18) | 8, 11,12 |
| B | 2/21/2008 | Updated maximum value for 48MHz Jitter, cycle to cycle | 15 |
| C | 2/23/2009 | Updated Functionality table. | 1 |
| D | 5/4/2010 | Added Tcase spec. | 12 |

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