

General Description

The 932SQL456 is a low power version of the CK420BQ synthesizer for Intel-based server platforms. It has 85 ohm Low-Power (LP) HCSL outputs that save 48 resistors and reduce power consumption by 50% compared to the standard CK420BQ. The 932SQL456 is driven with a 25MHz crystal for maximum performance. It generates CPU outputs of 100MHz. This device meets Separate- Reference-no-Spread (SRnS) PCIe requirements making it ideal for use in systems that need to communicate “outside the box”.

Recommended Application

Low-Power CK420BQ for SRnS PCIe Applications

Key Specifications

- CPU, SRC, NS_SRC and NS_SAS cycle-cycle jitter <50ps
- Output to output skew <50ps
- Phase jitter: PCIe Gen2 SRnS <2.2ps rms
- Phase jitter: PCIe Gen3 SRnS <0.7ps rms
- Phase jitter: QPI <0.3ps rms
- Phase jitter: NS-SAS <1.3ps rms using long period phase jitter method

Pin Configurations

| | | | |
|----------------------|----|----|--------------|
| SMBCLK | 1 | 64 | SMBDAT |
| GND14 | 2 | 63 | VDDCPU |
| AVDD14 | 3 | 62 | CPU3_Z85T |
| VDD14 | 4 | 61 | CPU3_Z85C |
| vREF14_2x/TEST_SELLY | 5 | 60 | CPU2_Z85T |
| GND14 | 6 | 59 | CPU2_Z85C |
| GNDXTAL | 7 | 58 | GNDCPU |
| X1_25 | 8 | 57 | VDDCPU |
| X2_25 | 9 | 56 | CPU1_Z85T |
| VDDXTAL | 10 | 55 | CPU1_Z85C |
| GNDPCI | 11 | 54 | CPU0_Z85T |
| VDDPCI | 12 | 53 | CPU0_Z85C |
| PCI4_2x | 13 | 52 | GNDNS |
| PCI3_2x | 14 | 51 | AVDD_NS_SAS |
| PCI2_2x | 15 | 50 | NS_SAS1_Z85T |
| PCI1_2x | 16 | 49 | NS_SAS1_Z85C |
| PCI0_2x | 17 | 48 | NS_SAS0_Z85T |
| GNDPCI | 18 | 47 | NS_SAS0_Z85C |
| VDDPCI | 19 | 46 | GNDNS |
| VDD48 | 20 | 45 | VDDNS |
| 48M_2x | 21 | 44 | NS_SRC1_Z85T |
| GND48 | 22 | 43 | NS_SRC1_Z85C |
| GND96 | 23 | 42 | NS_SRC0_Z85T |
| DOT96_Z85T | 24 | 41 | NS_SRC0_Z85C |
| DOT96_Z85C | 25 | 40 | NC |
| AVDD96 | 26 | 39 | GNDSRC |
| TEST_MODE | 27 | 38 | AVDD_SRC |
| CKPWRGD#/PD | 28 | 37 | VDDSRC |
| VDDSRC | 29 | 36 | SRC2_Z85T |
| SRC0_Z85T | 30 | 35 | SRC2_Z85C |
| SRC0_Z85C | 31 | 34 | SRC1_Z85T |
| GNDSRC | 32 | 33 | SRC1_Z85C |

64-TSSOP

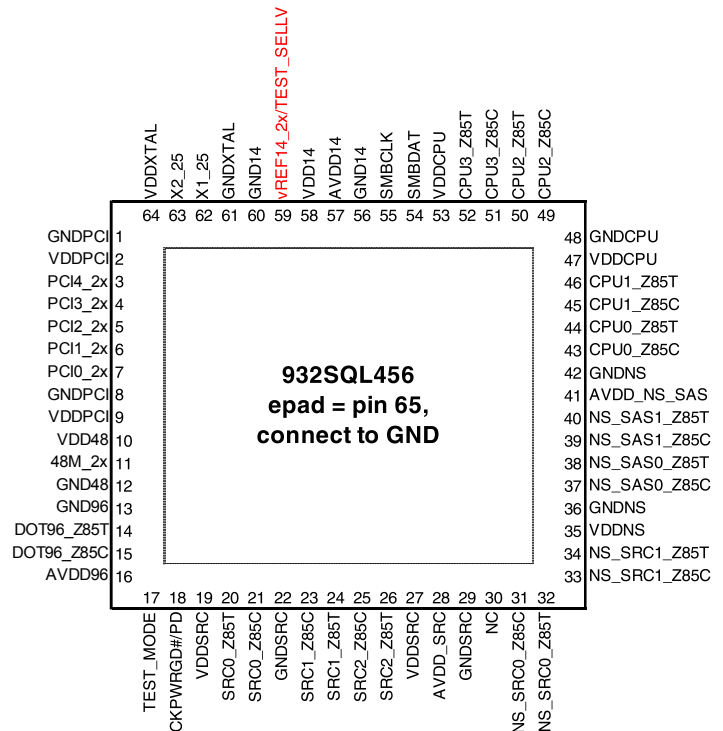
Note: Pins with ^ prefix have internal 120K pullup
Pins with v prefix have internal 120K pulldown

Features/Benefits

- Integrated 85-ohm differential terminations; saves 48 resistors compared to CK420BQ
- LP-HCSL outputs; up to 50% power savings compared to standard CK420BQ
- 64-pin TSSOP and VFQFPN packages; smallest board footprint
- Available in -40° to +85°C industrial temperature range version; supports demanding operating environments

Output Features

- Differential outputs are LP-HCSL with integrated 85Ω terminations
- 11 – *non-spreading* interchangeable 100MHz differential outputs
 - 4 – “CPU” outputs
 - 2 – “NS_SAS” outputs
 - 2 – “NS_SRC” outputs
 - 3 – “SRC” outputs
- 1 – DOT96 96MHz output
- 1 – 3.3V 48M output
- 5 – 3.3V PCI outputs
- 1 – 3.3V 14.318M output



64-Pin VFQFPN

Note: Pins with ^ prefix have internal 120K pullup
Pins with v prefix have internal 120K pulldown

64TSSOP Pin Descriptions

| PIN # | PIN NAME | TYPE | DESCRIPTION |
|-------|----------------------|------|--|
| 1 | SMBCLK | IN | Clock pin of SMBUS circuitry, 5V tolerant |
| 2 | GND14 | PWR | Ground pin for 14MHz output and logic. |
| 3 | AVDD14 | PWR | Analog power pin for 14MHz PLL |
| 4 | VDD14 | PWR | Power pin for 14MHz output and logic |
| 5 | vREF14_2x/TEST_SELLV | I/O | 14.318 MHz reference clock capable of driving 2 loads/ TEST_SEL latched input to enable test mode. The TEST_SEL input is a low threshold input. See the Electrical Tables and the Test Clarification Table. This pin has a weak (~120Kohm) internal pull down. |
| 6 | GND14 | PWR | Ground pin for 14MHz output and logic. |
| 7 | GNDXTAL | PWR | Ground pin for Crystal Oscillator. |
| 8 | X1_25 | IN | Crystal input, Nominally 25.00MHz. |
| 9 | X2_25 | OUT | Crystal output, Nominally 25.00MHz. |
| 10 | VDDXTAL | PWR | 3.3V power for the crystal oscillator. |
| 11 | GNDPCI | PWR | Ground pin for PCI outputs and logic. |
| 12 | VDDPCI | PWR | 3.3V power for the PCI outputs and logic |
| 13 | PCI4_2x | OUT | 3.3V PCI clock output |
| 14 | PCI3_2x | OUT | 3.3V PCI clock output |
| 15 | PCI2_2x | OUT | 3.3V PCI clock output |
| 16 | PCI1_2x | OUT | 3.3V PCI clock output |
| 17 | PCI0_2x | OUT | 3.3V PCI clock output |
| 18 | GNDPCI | PWR | Ground pin for PCI outputs and logic. |
| 19 | VDDPCI | PWR | 3.3V power for the PCI outputs and logic |
| 20 | VDD48 | PWR | 3.3V power for the 48MHz output and logic |
| 21 | 48M_2x | OUT | 3.3V 48MHz output |
| 22 | GND48 | PWR | Ground pin for 48MHz output and logic. |
| 23 | GND96 | PWR | Ground pin for DOT96 output and logic. |
| 24 | DOT96_Z85T | OUT | True clock of low-power push-pull differential 96MHz output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 25 | DOT96_Z85C | OUT | Complementary clock of low-power push-pull differential 96MHz output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 26 | AVDD96 | PWR | 3.3V power for the 48/96MHz PLL and the 96MHz output and logic |
| 27 | TEST_MODE | IN | TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table. |
| 28 | CKPWRGD#/PD | IN | CKPWRGD# is an active low input used to sample latched inputs and allow the device to Power Up. PD is an asynchronous active high input pin used to put the device into a low power state. The internal clocks and PLLs are stopped. |
| 29 | VDDSRC | PWR | 3.3V power for the SRC outputs and logic |
| 30 | SRC0_Z85T | OUT | True clock of low-power push-pull differential SRC output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 31 | SRC0_Z85C | OUT | Complementary clock of low-power push-pull differential SRC output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 32 | GNDSRC | PWR | Ground pin for SRC outputs and logic. |
| 33 | SRC1_Z85C | OUT | Complementary clock of low-power push-pull differential SRC output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 34 | SRC1_Z85T | OUT | True clock of low-power push-pull differential SRC output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 35 | SRC2_Z85C | OUT | Complementary clock of low-power push-pull differential SRC output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 36 | SRC2_Z85T | OUT | True clock of low-power push-pull differential SRC output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 37 | VDDSRC | PWR | 3.3V power for the SRC outputs and logic |
| 38 | AVDD_SRC | PWR | 3.3V power for the SRC PLL analog circuits |
| 39 | GNDSRC | PWR | Ground pin for SRC outputs and logic. |
| 40 | NC | N/A | No Connection. |

64TSSOP Pin Descriptions (cont.)

| PIN # | PIN NAME | TYPE | DESCRIPTION |
|-------|--------------|------|--|
| 41 | NS_SRC0_Z85C | OUT | Complementary clock of low-power push-pull differential non-spreading SRC output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 42 | NS_SRC0_Z85T | OUT | True clock of low-power push-pull differential non-spreading SRC output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 43 | NS_SRC1_Z85C | OUT | Complementary clock of low-power push-pull differential non-spreading SRC output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 44 | NS_SRC1_Z85T | OUT | True clock of low-power push-pull differential non-spreading SRC output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 45 | VDDNS | PWR | 3.3V power for the Non-Spreading differential outputs outputs and logic |
| 46 | GNDNS | PWR | Ground pin for non-spreading differential outputs and logic. |
| 47 | NS_SAS0_Z85C | OUT | Complementary clock of low-power push-pull differential non-spreading SAS output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 48 | NS_SAS0_Z85T | OUT | True clock of low-power push-pull differential non-spreading SAS output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 49 | NS_SAS1_Z85C | OUT | Complementary clock of low-power push-pull differential non-spreading SAS output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 50 | NS_SAS1_Z85T | OUT | True clock of low-power push-pull differential non-spreading SAS output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 51 | AVDD_NS_SAS | PWR | 3.3V power for the non-spreading SAS/SRC PLL analog circuits. |
| 52 | GNDNS | PWR | Ground pin for non-spreading differential outputs and logic. |
| 53 | CPU0_Z85C | OUT | Complementary clock of low-power push-pull differential CPU output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 54 | CPU0_Z85T | OUT | True clock of low-power push-pull differential CPU output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 55 | CPU1_Z85C | OUT | Complementary clock of low-power push-pull differential CPU output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 56 | CPU1_Z85T | OUT | True clock of low-power push-pull differential CPU output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 57 | VDDCPU | PWR | 3.3V power for the CPU outputs and logic |
| 58 | GNDCPU | PWR | Ground pin for CPU outputs and logic. |
| 59 | CPU2_Z85C | OUT | Complementary clock of low-power push-pull differential CPU output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 60 | CPU2_Z85T | OUT | True clock of low-power push-pull differential CPU output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 61 | CPU3_Z85C | OUT | Complementary clock of low-power push-pull differential CPU output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 62 | CPU3_Z85T | OUT | True clock of low-power push-pull differential CPU output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 63 | VDDCPU | PWR | 3.3V power for the CPU outputs and logic |
| 64 | SMBDAT | I/O | Data pin of SMBUS circuitry, 5V tolerant |

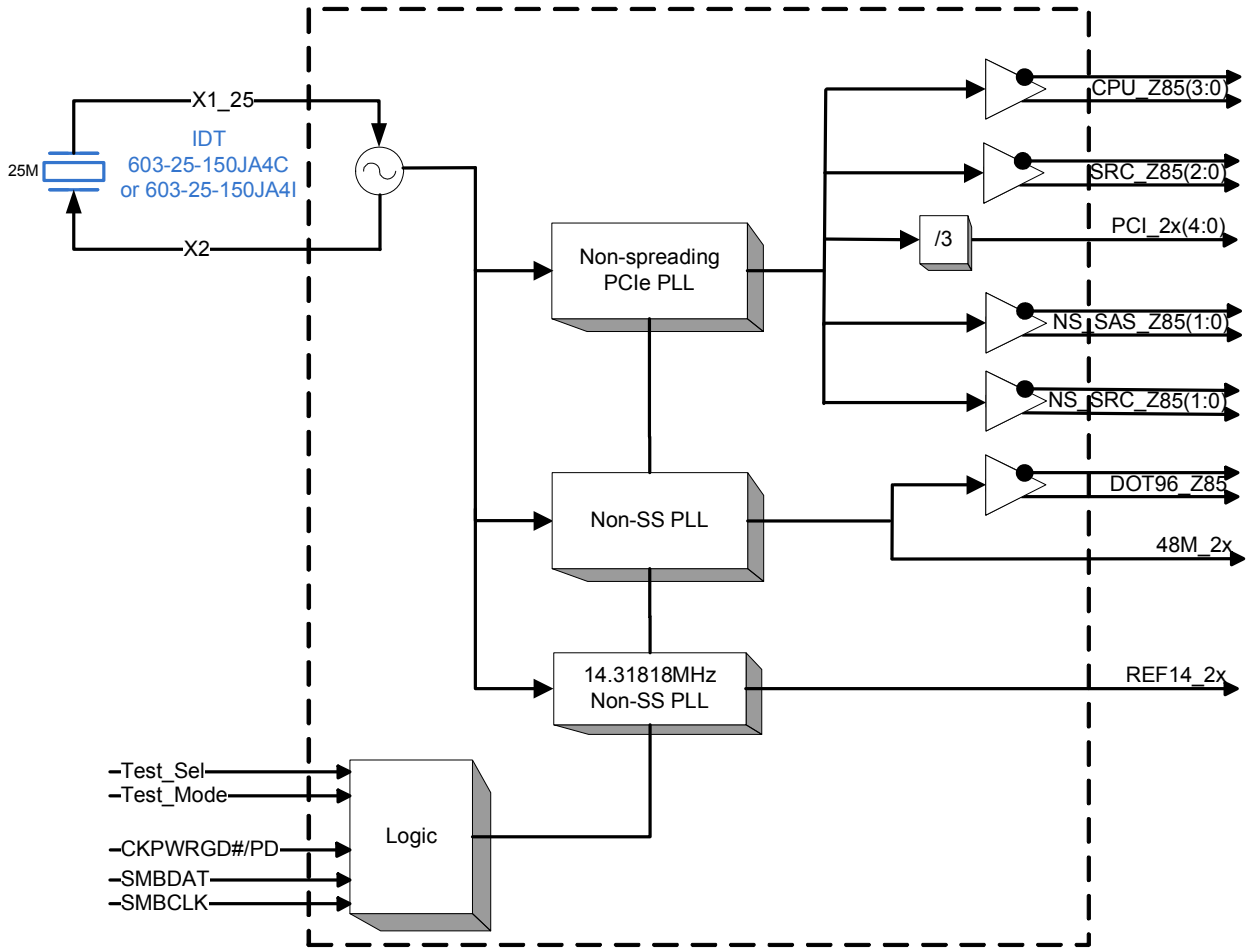
64VFQFPN Pin Descriptions

| PIN # | PIN NAME | TYPE | DESCRIPTION |
|-------|--------------|------|--|
| 1 | GNDPCI | PWR | Ground pin for PCI outputs and logic. |
| 2 | VDDPCI | PWR | 3.3V power for the PCI outputs and logic |
| 3 | PCI4_2x | OUT | 3.3V PCI clock output |
| 4 | PCI3_2x | OUT | 3.3V PCI clock output |
| 5 | PCI2_2x | OUT | 3.3V PCI clock output |
| 6 | PCI1_2x | OUT | 3.3V PCI clock output |
| 7 | PCI0_2x | OUT | 3.3V PCI clock output |
| 8 | GNDPCI | PWR | Ground pin for PCI outputs and logic. |
| 9 | VDDPCI | PWR | 3.3V power for the PCI outputs and logic |
| 10 | VDD48 | PWR | 3.3V power for the 48MHz output and logic |
| 11 | 48M_2x | OUT | 3.3V 48MHz output |
| 12 | GND48 | PWR | Ground pin for 48MHz output and logic. |
| 13 | GND96 | PWR | Ground pin for DOT96 output and logic. |
| 14 | DOT96_Z85T | OUT | True clock of low-power push-pull differential 96MHz output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 15 | DOT96_Z85C | OUT | Complementary clock of low-power push-pull differential 96MHz output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 16 | AVDD96 | PWR | 3.3V power for the 48/96MHz PLL and the 96MHz output and logic |
| 17 | TEST_MODE | IN | TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table. |
| 18 | CKPWRGD#/PD | IN | CKPWRGD# is an active low input used to sample latched inputs and allow the device to Power Up. PD is an asynchronous active high input pin used to put the device into a low power state. The internal clocks and PLLs are stopped. |
| 19 | VDDSRC | PWR | 3.3V power for the SRC outputs and logic |
| 20 | SRC0_Z85T | OUT | True clock of low-power push-pull differential SRC output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 21 | SRC0_Z85C | OUT | Complementary clock of low-power push-pull differential SRC output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 22 | GNDSRC | PWR | Ground pin for SRC outputs and logic. |
| 23 | SRC1_Z85C | OUT | Complementary clock of low-power push-pull differential SRC output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 24 | SRC1_Z85T | OUT | True clock of low-power push-pull differential SRC output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 25 | SRC2_Z85C | OUT | Complementary clock of low-power push-pull differential SRC output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 26 | SRC2_Z85T | OUT | True clock of low-power push-pull differential SRC output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 27 | VDDSRC | PWR | 3.3V power for the SRC outputs and logic |
| 28 | AVDD_SRC | PWR | 3.3V power for the SRC PLL analog circuits |
| 29 | GNDSRC | PWR | Ground pin for SRC outputs and logic. |
| 30 | NC | N/A | No Connection. |
| 31 | NS_SRC0_Z85C | OUT | Complementary clock of low-power push-pull differential non-spreading SRC output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 32 | NS_SRC0_Z85T | OUT | True clock of low-power push-pull differential non-spreading SRC output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 33 | NS_SRC1_Z85C | OUT | Complementary clock of low-power push-pull differential non-spreading SRC output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 34 | NS_SRC1_Z85T | OUT | True clock of low-power push-pull differential non-spreading SRC output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 35 | VDDNS | PWR | 3.3V power for the Non-Spreading differential outputs and logic |
| 36 | GNDNS | PWR | Ground pin for non-spreading differential outputs and logic. |
| 37 | NS_SAS0_Z85C | OUT | Complementary clock of low-power push-pull differential non-spreading SAS output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 38 | NS_SAS0_Z85T | OUT | True clock of low-power push-pull differential non-spreading SAS output. Internally terminated to drive 85ohm transmission lines with no external components. |

64VFQFPN Pin Descriptions (cont.)

| PIN # | PIN NAME | TYPE | DESCRIPTION |
|-------|----------------------|------|--|
| 39 | NS_SAS1_Z85C | OUT | Complementary clock of low-power push-pull differential non-spreading SAS output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 40 | NS_SAS1_Z85T | OUT | True clock of low-power push-pull differential non-spreading SAS output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 41 | AVDD_NS_SAS | PWR | 3.3V power for the non-spreading SAS/SRC PLL analog circuits. |
| 42 | GNDNS | PWR | Ground pin for non-spreading differential outputs and logic. |
| 43 | CPU0_Z85C | OUT | Complementary clock of low-power push-pull differential CPU output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 44 | CPU0_Z85T | OUT | True clock of low-power push-pull differential CPU output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 45 | CPU1_Z85C | OUT | Complementary clock of low-power push-pull differential CPU output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 46 | CPU1_Z85T | OUT | True clock of low-power push-pull differential CPU output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 47 | VDDCPU | PWR | 3.3V power for the CPU outputs and logic |
| 48 | GNDCPU | PWR | Ground pin for CPU outputs and logic. |
| 49 | CPU2_Z85C | OUT | Complementary clock of low-power push-pull differential CPU output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 50 | CPU2_Z85T | OUT | True clock of low-power push-pull differential CPU output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 51 | CPU3_Z85C | OUT | Complementary clock of low-power push-pull differential CPU output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 52 | CPU3_Z85T | OUT | True clock of low-power push-pull differential CPU output. Internally terminated to drive 85ohm transmission lines with no external components. |
| 53 | VDDCPU | PWR | 3.3V power for the CPU outputs and logic |
| 54 | SMBDAT | I/O | Data pin of SMBUS circuitry, 5V tolerant |
| 55 | SMBCLK | IN | Clock pin of SMBUS circuitry, 5V tolerant |
| 56 | GND14 | PWR | Ground pin for 14MHz output and logic. |
| 57 | AVDD14 | PWR | Analog power pin for 14MHz PLL |
| 58 | VDD14 | PWR | Power pin for 14MHz output and logic |
| 59 | vREF14_2x/TEST_SELLV | I/O | 14.318 MHz reference clock capable of driving 2 loads/ TEST_SEL latched input to enable test mode. The TEST_SEL input is a low threshold input. See the Electrical Tables and the Test Clarification Table. This pin has a weak (~120Kohm) internal pull down. |
| 60 | GND14 | PWR | Ground pin for 14MHz output and logic. |
| 61 | GNDXTAL | PWR | Ground pin for Crystal Oscillator. |
| 62 | X1_25 | IN | Crystal input, Nominally 25.00MHz. |
| 63 | X2_25 | OUT | Crystal output, Nominally 25.00MHz. |
| 64 | VDDXTAL | PWR | 3.3V power for the crystal oscillator. |
| 65 | EPAD | GND | Epad should be connected to ground. |

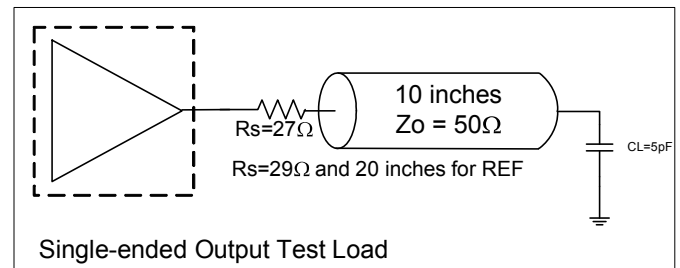
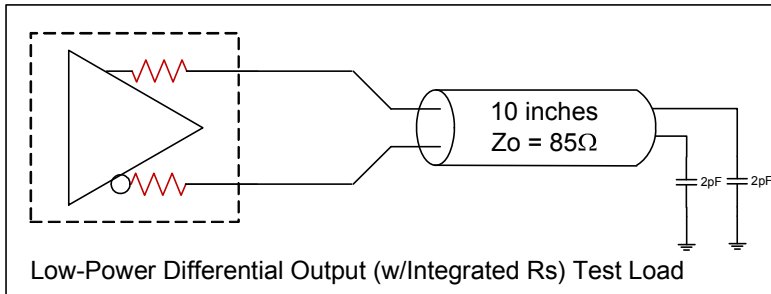
Block Diagram



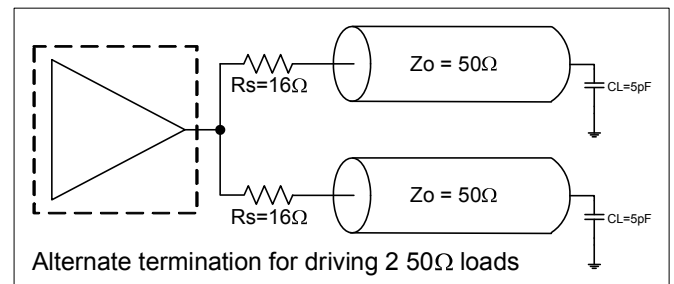
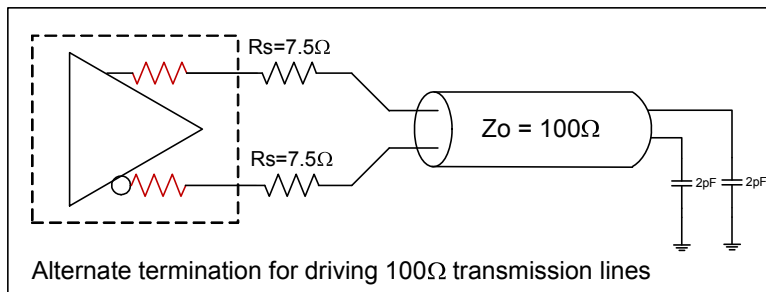
Power Supply and Test Loads

Power Group Pin Numbers

| VFQFPN | | TSSOP | | Description |
|--------|------|--------|--------|--|
| VDD | GND | VDD | GND | |
| 57 | 56 | 3 | 2 | 14MHz PLL Analog |
| 58 | 60 | 4 | 6 | REF14M Output and Logic |
| 64 | 61 | 10 | 7 | 25MHz XTAL |
| 2, 9 | 1, 8 | 12, 19 | 11, 18 | PCI Outputs and Logic |
| 10 | 12 | 20 | 22 | 48MHz Output and Logic |
| 16 | 13 | 26 | 23 | 96MHz PLL Analog, Output and Logic |
| 19, 27 | 22 | 29, 37 | 32 | SRC Outputs and Logic |
| 28 | 29 | 38 | 39 | SRC PLL Analog |
| 35 | 36 | 45 | 46 | Non-Spreading Differential Outputs & Logic |
| 41 | 42 | 51 | 52 | NS-SAS/SRC PLL Analog |
| 47, 53 | 48 | 57,63 | 58 | CPU Outputs and Logic |



Alternate Terminations



The 932SQL456 can also drive other logic levels such as LVPECL, LVDS, and CML. See [“AN-891 Driving LVPECL, LVDS, and CML Logic with IDT’s “Universal” Low-Power HCSL Outputs”](#) for details.

Functionality Tables

932SQL456 Functionality

| | | | | | | | |
|-----|-----|-------|--------|------------------|-------|-------|-----|
| CPU | SRC | PCI | REF | NS_SAS NS_SRC | DOT96 | USB | |
| 100 | 100 | 33.33 | 14.318 | 100.00 | 96.00 | 48.00 | MHz |

932SQL456 Power Down Functionality

| CKPWRGD#/PD | Differential Outputs | Single-ended Outputs | Single-ended Outputs w/Latch |
|-------------|----------------------|----------------------|------------------------------|
| 1 | Low/Low | Low | Low ¹ |
| 0 | Running | | |

1. Single-ended outputs with a Latch will be Hi-Z until the first application of CKPWRGD#.

Clock AC Tolerances

| | CPU, SRC | NS_SAS, NS_SRC | PCI | DOT96 | 48MHz | REF | |
|------------------------------|----------|-------------------|-------|-------|-------|-------|------------|
| PPM tolerance | 100 | 100 | 100 | 100 | 100 | 100 | ppm |
| Cycle to Cycle Jitter | 50 | 50 | 250 | 50 | 250 | 250 | ps |
| Spread | 0.00% | 0.00% | 0.00% | 0 | 0.00% | 0.00% | % |

Clock Periods–Outputs

| SSC OFF | Center Freq. MHz | Measurement Window | | | | | | | Units | Notes |
|---------------------------|------------------|------------------------------|--------------------------------------|--------------------------------------|----------------------------|--------------------------------------|--------------------------------------|------------------------------|-------|-------|
| | | 1 Clock | 1us | 0.1s | 0.1s | 0.1s | 1us | 1 Clock | | |
| | | -c2c jitter AbsPer Min | -SSC Short-Term Average Min | - ppm Long-Term Average Min | 0 ppm Period Nominal | + ppm Long-Term Average Max | +SSC Short-Term Average Max | +c2c jitter AbsPer Max | | |
| SRC, NS_SAS, NS_SRC | 100.000 | 9.94900 | | 9.99900 | 10.00000 | 10.00100 | | 10.05100 | ns | 1,2 |
| PCI | 33.333 | 29.74700 | | 29.99700 | 30.00000 | 30.00300 | | 30.25300 | ns | 1,2 |
| DOT96 | 96.000 | 10.36563 | | 10.41563 | 10.41667 | 10.41771 | | 10.46771 | ns | 1,2 |
| 48MHz | 48.000 | 20.58125 | | 20.83125 | 20.83333 | 20.83542 | | 21.08542 | ns | 1,2 |
| REF | 14.318 | 69.78429 | | 69.83429 | 69.84128 | 69.84826 | | 69.89826 | ns | 1,2 |

¹Guaranteed by design and characterization, not 100% tested in production.

²All Long Term Accuracy specifications are guaranteed with the assumption that the REF output is tuned to exactly 14.31818MHz.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 932SQL456. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---------------------------|--------------------|----------------------------|---------|-----|-----------------------|-------|-------|
| 3.3V Core Supply Voltage | VDDA | | | | 4.6 | V | 1,2 |
| 3.3V Logic Supply Voltage | VDD | | | | 4.6 | V | 1,2 |
| Input Low Voltage | V _{IL} | | GND-0.5 | | | V | 1 |
| Input High Voltage | V _{IH} | Except for SMBus interface | | | V _{DD} +0.5V | V | 1 |
| Input High Voltage | V _{IHSMB} | SMBus clock and data pins | | | 5.5V | V | 1 |
| Storage Temperature | T _s | | -65 | | 150 | °C | 1 |
| Junction Temperature | T _j | | | | 125 | °C | 1 |
| Case Temperature | T _c | | | | 110 | °C | 1 |
| Input ESD protection | ESD prot | Human Body Model | 2000 | | | V | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Operation under these conditions is neither implied nor guaranteed.

Electrical Characteristics—Current Consumption

T_A = T_{AMB}; Supply Voltage VDDx = 3.3 V +/-5%

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|--------------------------|-----------------------|--|-----|-----|-----|-------|-------|
| Operating Supply Current | I _{DD3.3OP} | All outputs active @100MHz, C _L = Full load; | | 217 | 250 | mA | 1 |
| Powerdown Current | I _{DD3.3PDZ} | | | 4.3 | 8 | mA | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

AC Electrical Characteristics—CPU, SRC, NS_SAS, NS_SRC, DOT96 LP-HCSL Outputs

T_A = T_{AMB}; Supply Voltage VDDx = 3.3 V +/-5%

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|-----------------------|---|-----|-------|-----|-------|-------|
| Duty Cycle | t _{DC} | Measured differentially, PLL Mode | 45 | 49.6% | 55 | % | |
| Skew, Output to Output | t _{sk3SRC} | Across all SRC outputs, V _T = 50% | | 23 | 50 | ps | 1 |
| Skew, Output to Output | t _{sk3CPU} | Across all CPU outputs, V _T = 50% | | 24 | 50 | ps | 1 |
| Jitter, Cycle to cycle | t _{jcyc-cyc} | CPU, SRC, NS_SAS outputs | | 6 | 50 | ps | 1,3 |
| | | DOT96 output | | 5 | 50 | ps | 1,3 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Z_o=85Ω (differential impedance).

³Measured from differential waveform

Electrical Characteristics–Input/Supply/Common Parameters

TA = T_{AMB}; Supply Voltage VDDx = 3.3 V +/-5%

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|----------------------------------|---------------------|---|-----------------------|-------|-----------------------|-------|-------|
| Operating Voltage | V | | 3.135 | 3.3 | 3.465 | V | |
| Ambient Operating Temperature | T _{AMB} | Commercial range | 0 | | 70 | °C | |
| | | Industrial range | -40 | | 85 | °C | |
| Input High Voltage | V _{IH} | Single-ended inputs, except SMBus, low threshold and tri-level inputs | 2 | | V _{DD} + 0.3 | V | |
| Input Low Voltage | V _{IL} | Single-ended inputs, except SMBus, low threshold and tri-level inputs | GND - 0.3 | | 0.8 | V | |
| Input Current | I _{IN} | Single-ended inputs, V _{IN} = GND, V _{IN} = VDD | -5 | | 5 | uA | |
| | I _{INP} | Single-ended inputs. V _{IN} = 0 V; Inputs with internal pull-up resistors V _{IN} = VDD; Inputs with internal pull-down resistors | -200 | | 200 | uA | |
| Low Threshold Input-High Voltage | V _{IH_FS} | 3.3 V +/-5% | 0.7 | | V _{DD} + 0.3 | V | |
| Low Threshold Input-Low Voltage | V _{IL_FS} | 3.3 V +/-5% | V _{SS} - 0.3 | | 0.35 | V | |
| Input Frequency | F _i | | | 25.00 | | MHz | 2 |
| Pin Inductance | L _{pin} | | | | 7 | nH | 1 |
| Capacitance | C _{IN} | Logic Inputs | | | 5 | pF | 1 |
| | C _{OUT} | Output pin capacitance | | | 5 | pF | 1 |
| | C _{INX} | X1 & X2 pins | | | 5 | pF | 1 |
| Clk Stabilization | T _{STAB} | From V _{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock | | | 1.8 | ms | 2 |
| Tdrive_PD# | t _{DRVPD} | Differential output enable after PD# de-assertion | | | 300 | us | 1,3 |
| Tfall | t _F | Fall time of control inputs | | | 5 | ns | 1,2 |
| Trise | t _R | Rise time of control inputs | | | 5 | ns | 1,2 |
| SMBus Input Low Voltage | V _{ILSMB} | | | | 0.8 | V | |
| SMBus Input High Voltage | V _{IHSMB} | | 2.1 | | V _{DD} SMB | V | |
| SMBus Output Low Voltage | V _{OL} SMB | @ I _{PULLUP} | | | 0.4 | V | |
| SMBus Sink Current | I _{PULLUP} | @ V _{OL} | 4 | | | mA | |
| Nominal Bus Voltage | V _{DD} SMB | 3V to 5V +/- 10% | 2.7 | | 5.5 | V | 1 |
| SCLK/SDATA Rise Time | t _{RSMB} | (Max V _{IL} - 0.15) to (Min V _{IH} + 0.15) | | | 1000 | ns | 1 |
| SCLK/SDATA Fall Time | t _{FSMB} | (Min V _{IH} + 0.15) to (Max V _{IL} - 0.15) | | | 300 | ns | 1 |
| SMBus Operating Frequency | f _{SMB} | SMBus operating frequency | 400 | | | kHz | |

¹Guaranteed by design and characterization, not 100% tested in production.

²Control input must be monotonic from 20% to 80% of input swing.

³Time from deassertion until outputs are >200 mV

DC Electrical Characteristics—CPU, SRC, NS_SAS, NS_SRC, DOT96 LP-HCSL Outputs

TA = T_{AMB}; Supply Voltage VDDx = 3.3 V +/-5%

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|-------------------------|------------------|---|------|------|------|-------|---------|
| Slew rate | dV/dt | Scope averaging on | 2 | 3.3 | 4.5 | V/ns | 1, 2, 3 |
| Slew rate matching | Δ dV/dt | Slew rate matching, Scope averaging on | | 11.1 | 20 | % | 1, 2, 4 |
| Rise/Fall Time Matching | Δ Trf | Rise/fall matching, Scope averaging off | | 9.0 | 125 | ps | 1, 8, 9 |
| Voltage High | VHigh | Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on) | 660 | 845 | 850 | mV | |
| Voltage Low | VLow | | -150 | 122 | 150 | | |
| Max Voltage | Vmax | Measurement on single ended signal using absolute value. | | 1026 | 1150 | mV | 1, 7 |
| Min Voltage | Vmin | | -300 | -22 | | | 1, 7 |
| Crossing Voltage (abs) | Vcross_abs | Scope averaging off | 250 | 482 | 550 | mV | 1, 5 |
| Crossing Voltage (var) | Δ -Vcross | Scope averaging off | | 22 | 140 | mV | 1, 6 |

¹Guaranteed by design and characterization, not 100% tested in production. Z_O=85 Ω (differential impedance).

² Measured from differential waveform

³ Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

⁴ Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

⁵ Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

⁶ The total variation of all Vcross measurements in any particular system. Note that this is a subset of V_cross_min/max (V_cross absolute) allowed. The intent is to limit Vcross induced modulation by setting V_cross_delta to be smaller than

⁷ Includes overshoot and undershoot.

⁸ Measured from single-ended waveform

⁹ Measured with scope averaging off, using statistics function. Variation is difference between min and max.

Electrical Characteristics—48MHz

TA = T_{AMB}; Supply Voltage VDDx = 3.3 V +/-5%

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|--------------------------|--------------------------|-------|------|--------|-------|-------|
| Output High Voltage | V _{OH} | I _{OH} = -1 mA | 2.4 | | | V | |
| Output Low Voltage | V _{OL} | I _{OL} = 1 mA | | | 0.55 | V | |
| Clock High Time | T _{HIGH} | 1.5V | 8.094 | | 10.036 | ns | 1 |
| Clock Low Time | T _{LOW} | 1.5V | 7.694 | | 9.836 | ns | 1 |
| Edge Rate | t _{slewr/f USB} | Rising/Falling edge rate | 1 | 1.7 | 2 | V/ns | 1,2 |
| Duty Cycle | d _{t1} | V _T = 1.5 V | 45 | 50.4 | 55 | % | 1 |
| Jitter, Cycle to cycle | t _{jycyc-cyc} | V _T = 1.5 V | | 29 | 250 | ps | 1 |

See "Power Supply and Test Loads" page for termination circuits

¹Guaranteed by design and characterization, not 100% tested in production.

² Measured between 0.8V and 2.0V

Electrical Characteristics–PCI

TA = T_{AMB}; Supply Voltage VDDx = 3.3 V +/-5%

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|----------------------|--------------------------|-----|------|------|-------|-------|
| Output High Voltage | V _{OH} | I _{OH} = -1 mA | 2.4 | | | V | |
| Output Low Voltage | V _{OL} | I _{OL} = 1 mA | | | 0.55 | V | |
| Clock High Time | T _{HIGH} | 1.5V | 12 | | | ns | 1 |
| Clock Low Time | T _{LOW} | 1.5V | 12 | | | ns | 1 |
| Edge Rate | t _{slwrf} | Rising/Falling edge rate | 1 | 1.7 | 4 | V/ns | 1,2 |
| Duty Cycle | d _{t1} | V _T = 1.5 V | 45 | 50.6 | 55 | % | 1 |
| Group Skew | t _{skew} | V _T = 1.5 V | | 496 | 550 | ps | 1 |
| Jitter, Cycle to cycle | t _{jcc-cyc} | V _T = 1.5 V | | 23 | 250 | ps | 1 |

See "Power Supply and Test Loads" page for termination circuits

¹Guaranteed by design and characterization, not 100% tested in production.

² Measured between 0.8V and 2.0V

Electrical Characteristics–Phase Jitter Parameters

TA = T_{AMB}; Supply Voltage VDDx = 3.3 V +/-5%

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | IND. LIMIT | UNITS | Notes |
|------------------------|----------------------------|---|------|---------|-------|------------|----------|---------|
| Phase Jitter | t _{jphPCIeG1} | PCIe Gen 1 | | 24.8 | 30 | 86 | ps (p-p) | 1,2,3,6 |
| | t _{jphPCIeG2} | PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz | | 0.54 | 0.7 | 3 | ps (rms) | 1,2,6 |
| | | PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) | | 2.2 | 2.6/3 | 3.1 | ps (rms) | 1,2,6 |
| | t _{jphPCIeG3Com} | PCIe Gen 3 Common Clock (PLL BW of 2-4MHz. CDR = 10MHz) | | 0.46 | 0.6 | 1 | ps (rms) | 1,2,4,6 |
| | t _{jphPCIeG3SRns} | PCIe Gen 3 Separate Reference no Spread (SRnS) (PLL BW of 2-4MHz. CDR = 10MHz) | | 0.46 | 0.6 | 0.7 | ps (rms) | 1,2,4,6 |
| | t _{jphQPI_SMI} | QPI & SMI (100MHz, 4.8Gb/s, 6.4Gb/s 12UI) | | 0.24 | 0.4 | 0.5 | ps (rms) | 1,5,6 |
| | | QPI & SMI (100MHz, 8.0Gb/s, 12UI) | | 0.13 | 0.15 | 0.3 | ps (rms) | 1,5,6 |
| | | QPI & SMI (100MHz, 9.6Gb/s, 12UI) | | 0.11 | 0.13 | 0.2 | ps (rms) | 1,5,6 |
| t _{jphSAS12G} | SAS 12G | | 0.84 | 1.1/1.2 | 1.3 | ps (rms) | 1,5,6 | |

¹ Guaranteed by design and characterization, not 100% tested in production.

² See <http://www.pcisig.com> for complete specs

³ Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

⁴ Subject to final radification by PCI SIG.

⁵ Calculated from Intel-supplied Clock Jitter Tool v 1.6.6

⁶ Applied to SRC, CPU and NS_SRC, NS_SAS outputs, second figure if present applies to -40C.

Electrical Characteristics–REF14M

TA = T_{AMB}; Supply Voltage VDDx = 3.3 V +/-5%

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | Notes |
|------------------------|----------------------|--------------------------|------|------|------|-------|-------|
| Output High Voltage | V _{OH} | I _{OH} = -1 mA | 2.4 | | | V | |
| Output Low Voltage | V _{OL} | I _{OL} = 1 mA | | | 0.55 | V | |
| Clock High Time | T _{HIGH} | 1.5V | 27.5 | | | ns | 1 |
| Clock Low Time | T _{LOW} | 1.5V | 27.5 | | | ns | 1 |
| Edge Rate | t _{slewr/f} | Rising/Falling edge rate | 1 | 1.9 | 4 | V/ns | 1,2 |
| Duty Cycle | d _{t1} | V _T = 1.5 V | 45 | 50.2 | 55 | % | 1 |
| Jitter, Cycle to cycle | t _{jyc-cyc} | V _T = 1.5 V | | 19 | 250 | ps | 1 |

See "Power Supply and Test Loads" page for termination circuits

¹Guaranteed by design and characterization, not 100% tested in production.

² Measured between 0.8V and 2.0V

Test Clarification Table

| Comments | HW | | SW | | OUTPUT |
|---|--------------------|-------------------------|---------------------------|--------------------------|--------|
| | TEST_SEL HW PIN | TEST_MOD E HW PIN | TEST ENTRY BIT B6b6 | REF/N or HI-Z B6b7 | |
| | 0 | X | 0 | X | NORMAL |
| Power-up w/ TEST_SEL = 1 (>0.7V) to enter test mode. TEST_SEL is low threshold input . Cycle power to disable test mode. | 1 | 0 | X | 0 | HI-Z |
| | 1 | 0 | X | 1 | REF/N |
| | 1 | 1 | X | 0 | REF/N |
| | 1 | 1 | X | 1 | REF/N |
| If TEST_SEL HW pin is 0 during power-up, test mode can be selected through B6b6. If test mode is selected by B6b6, then B6b7 is used to select HI-Z or REF/N. FS_B/TEST_Mode pin is not used. Cycle power to disable test mode. | 0 | X | 1 | 0 | HI-Z |
| | 0 | X | 1 | 1 | REF/N |

B6b6: 1= ENTER TEST MODE, Default = 0 (NORMAL OPERATION)

B6b7: 1= REF/N, Default = 0 (HI-Z)

General SMBus Serial Interface Information for 932SQL456

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte N through Byte N+X-1
- IDT clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

| Index Block Write Operation | | | |
|---------------------------------|-----------|----------------------|-----|
| Controller (Host) | | IDT (Slave/Receiver) | |
| T | starT bit | | |
| Slave Address D2 _(H) | | | |
| WR | WRite | | |
| | | ACK | |
| Beginning Byte = N | | | |
| | | ACK | |
| Data Byte Count = X | | | |
| | | ACK | |
| Beginning Byte N | | X Byte | |
| | | | ACK |
| O | | | O |
| O | | | O |
| O | | O | |
| Byte N + X - 1 | | | |
| | | ACK | |
| P | stoP bit | | |

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte N+X-1
- IDT clock sends **Byte 0 through Byte X (if X_(H) was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation | | |
|---------------------------------|-----------------|----------------------|
| Controller (Host) | | IDT (Slave/Receiver) |
| T | starT bit | |
| Slave Address D2 _(H) | | |
| WR | WRite | |
| | | ACK |
| Beginning Byte = N | | |
| | | ACK |
| RT | Repeat starT | |
| Slave Address D3 _(H) | | |
| RD | ReaD | |
| | | ACK |
| | | Data Byte Count=X |
| ACK | | |
| | | Beginning Byte N |
| ACK | | |
| O | | O |
| O | | O |
| O | | O |
| | | Byte N + X - 1 |
| N | Not acknowledge | |
| P | stoP bit | |

| Read Address | Write Address |
|-------------------|-------------------|
| D3 _(H) | D2 _(H) |

NOTE: Pin numbers refer to TSSOP

SMBus Table: Output Enable Register

| Byte 0 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|----------------|------------------|------|-----------------|--------|---------|
| Bit 7 | 24/25 | DOT96 Enable | Output Enable | RW | Disable-Low/Low | Enable | 1 |
| Bit 6 | 50/49 | NS_SAS1 Enable | Output Enable | RW | Disable-Low/Low | Enable | 1 |
| Bit 5 | 48/47 | NS_SAS0 Enable | Output Enable | RW | Disable-Low/Low | Enable | 1 |
| Bit 4 | 44/43 | NS_SRC1 Enable | Output Enable | RW | Disable-Low/Low | Enable | 1 |
| Bit 3 | 42/41 | NS_SRC0 Enable | Output Enable | RW | Disable-Low/Low | Enable | 1 |
| Bit 2 | 36/35 | SRC2 Enable | Output Enable | RW | Disable-Low/Low | Enable | 1 |
| Bit 1 | 34/33 | SRC1 Enable | Output Enable | RW | Disable-Low/Low | Enable | 1 |
| Bit 0 | 30/31 | SRC0 Enable | Output Enable | RW | Disable-Low/Low | Enable | 1 |

SMBus Table: Output Enable Register

| Byte 1 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|-----------------|------------------|------|-----------------|--------|---------|
| Bit 7 | 5 | REF14_2x Enable | Output Enable | RW | Disable-Low | Enable | 1 |
| Bit 6 | | RESERVED | | | | | 0 |
| Bit 5 | | RESERVED | | | | | 0 |
| Bit 4 | 62/61 | CPU3 | Output Enable | RW | Disable-Low/Low | Enable | 1 |
| Bit 3 | 60/59 | CPU2 | Output Enable | RW | Disable-Low/Low | Enable | 1 |
| Bit 2 | 56/55 | CPU1 | Output Enable | RW | Disable-Low/Low | Enable | 1 |
| Bit 1 | 54/53 | CPU0 | Output Enable | RW | Disable-Low/Low | Enable | 1 |
| Bit 0 | | RESERVED | | | | | 0 |

SMBus Table: Output Enable Register

| Byte 2 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|--------------|------------------|------|-------------|--------|---------|
| Bit 7 | | RESERVED | | | | | 0 |
| Bit 6 | | RESERVED | | | | | 0 |
| Bit 5 | 13 | PCI4 Enable | Output Enable | RW | Disable-Low | Enable | 1 |
| Bit 4 | 14 | PCI3 Enable | Output Enable | RW | Disable-Low | Enable | 1 |
| Bit 3 | 15 | PCI2 Enable | Output Enable | RW | Disable-Low | Enable | 1 |
| Bit 2 | 16 | PCI1 Enable | Output Enable | RW | Disable-Low | Enable | 1 |
| Bit 1 | 17 | PCI0 Enable | Output Enable | RW | Disable-Low | Enable | 1 |
| Bit 0 | 21 | 48MHz Enable | Output Enable | RW | Disable-Low | Enable | 1 |

SMBus Table: Differential Amplitude Control

| Byte 3 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------------------------|------------------|------|------------|-------------|---------|
| Bit 7 | | CPU AMPLITUDE 1 | CPU Vhigh | RW | 00 = 700mV | 01 = 800mV | 0 |
| Bit 6 | | CPU AMPLITUDE 0 | | RW | 10 = 900mV | 11 = 1000mV | 1 |
| Bit 5 | | SRC AMPLITUDE 1 | SRC Vhigh | RW | 00 = 700mV | 01 = 800mV | 0 |
| Bit 4 | | SRC AMPLITUDE 0 | | RW | 10 = 900mV | 11 = 1000mV | 1 |
| Bit 3 | | DOT96 AMPLITUDE 1 | DOT96 Vhigh | RW | 00 = 700mV | 01 = 800mV | 0 |
| Bit 2 | | DOT96 AMPLITUDE 0 | | RW | 10 = 900mV | 11 = 1000mV | 1 |
| Bit 1 | | NS-SAS/SRC AMPLITUDE 1 | NS-SAS/SRC Vhigh | RW | 00 = 700mV | 01 = 800mV | 0 |
| Bit 0 | | NS-SAS/SRC AMPLITUDE 0 | | RW | 10 = 900mV | 11 = 1000mV | 1 |

SMBus Table: Reserved

| Byte 4 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|----------|------------------|------|---|---|---------|
| Bit 7 | | RESERVED | | | | | 0 |
| Bit 6 | | RESERVED | | | | | 0 |
| Bit 5 | | RESERVED | | | | | 0 |
| Bit 4 | | RESERVED | | | | | 0 |
| Bit 3 | | RESERVED | | | | | 0 |
| Bit 2 | | RESERVED | | | | | 0 |
| Bit 1 | | RESERVED | | | | | 1 |
| Bit 0 | | RESERVED | | | | | 1 |

SMBus Table: Reserved

| Byte 5 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7 | | | RESERVED | | | | 0 |
| Bit 6 | | | RESERVED | | | | 0 |
| Bit 5 | | | RESERVED | | | | 0 |
| Bit 4 | | | RESERVED | | | | 0 |
| Bit 3 | | | RESERVED | | | | 0 |
| Bit 2 | | | RESERVED | | | | 1 |
| Bit 1 | | | RESERVED | | | | 1 |
| Bit 0 | | | RESERVED | | | | 1 |

SMBus Table: Test Mode and CPU/SRC/PCI Frequency Select Register

| Byte 6 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|-------------|------------------|------|---------|--------|---------|
| Bit 7 | - | Test Mode | Test Mode Type | RW | Hi-Z | REF/N | 0 |
| Bit 6 | - | Test Select | Select Test Mode | RW | Disable | Enable | 0 |
| Bit 5 | - | | RESERVED | | | | 0 |
| Bit 4 | - | | RESERVED | | | | 1 |
| Bit 3 | - | | RESERVED | | | | 0 |
| Bit 2 | - | | RESERVED | | | | 0 |
| Bit 1 | - | | RESERVED | | | | 1 |
| Bit 0 | - | | RESERVED | | | | 1 |

SMBus Table: Vendor & Revision ID Register

| Byte 7 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|--------------------------------|------|------------------|---|---------|
| Bit 7 | - | RID3 | REVISION ID (10h for A rev) | R | 0 for A rev | | 0 |
| Bit 6 | - | RID2 | | R | | | 0 |
| Bit 5 | - | RID1 | | R | | | 0 |
| Bit 4 | - | RID0 | | R | | | 0 |
| Bit 3 | - | VID3 | VENDOR ID | R | 0001 for ICS/IDT | | 0 |
| Bit 2 | - | VID2 | | R | | | 0 |
| Bit 1 | - | VID1 | | R | | | 0 |
| Bit 0 | - | VID0 | | R | | | 1 |

SMBus Table: Byte Count Register

| Byte 8 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|----------------------------------|------|---|---|---------|
| Bit 7 | - | BC7 | Byte Count Programming b(7:0) | RW | Writing to this register will configure how many bytes will be read back, default is A bytes. (0 to 9) | | 0 |
| Bit 6 | - | BC6 | | RW | | | 0 |
| Bit 5 | - | BC5 | | RW | | | 0 |
| Bit 4 | - | BC4 | | RW | | | 0 |
| Bit 3 | - | BC3 | | RW | | | 0 |
| Bit 2 | - | BC2 | | RW | | | 0 |
| Bit 1 | - | BC1 | | RW | | | 0 |
| Bit 0 | - | BC0 | | RW | | | 1 |

SMBus Table: Device ID Register

| Byte 9 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|-----------------------|------|---|---|---------|
| Bit 7 | | DID7 | Device ID (46 hex) | R | - | - | 0 |
| Bit 6 | | DID6 | | R | - | - | 1 |
| Bit 5 | | DID5 | | R | - | - | 0 |
| Bit 4 | | DID4 | | R | - | - | 0 |
| Bit 3 | | DID3 | | R | - | - | 0 |
| Bit 2 | | DID2 | | R | - | - | 1 |
| Bit 1 | | DID1 | | R | - | - | 1 |
| Bit 0 | | DID0 | | R | - | - | 0 |

Recommended Crystal Characteristics (3225 package)

| PARAMETER | VALUE | UNITS | NOTES |
|--|-------------|---------|-------|
| Frequency | 25 | MHz | 1 |
| Resonance Mode | Fundamental | - | 1 |
| Frequency Tolerance @ 25°C | ±20 | PPM Max | 1 |
| Frequency Stability, ref @ 25°C Over Operating Temperature Range | ±20 | PPM Max | 1 |
| Temperature Range (commercial) | 0~70 | °C | 1 |
| Temperature Range (industrial) | -40~85 | °C | 2 |
| Equivalent Series Resistance (ESR) | 50 | Ω Max | 1 |
| Shunt Capacitance (C ₀) | 7 | pF Max | 1 |
| Load Capacitance (C _L) | 8 | pF Max | 1 |
| Drive Level | 0.3 | mW Max | 1 |
| Aging per year | ±5 | PPM Max | 1 |

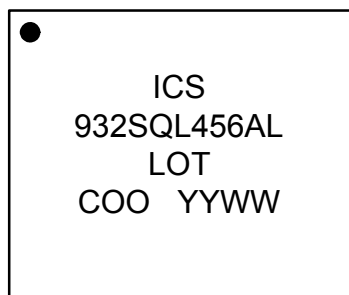
Notes:

1. IDT 603-25-150JA4C or 603-25-150JA4I

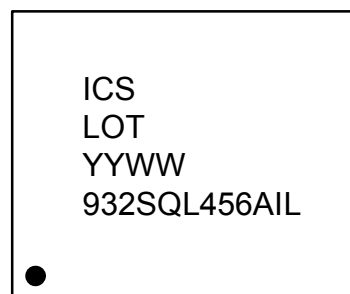
Marking Diagrams



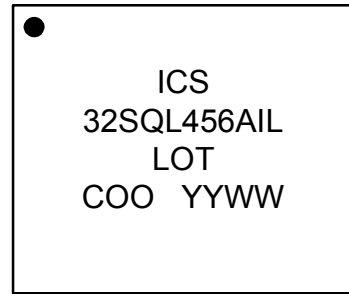
64TSSOP



64VFQFPN



64TSSOP

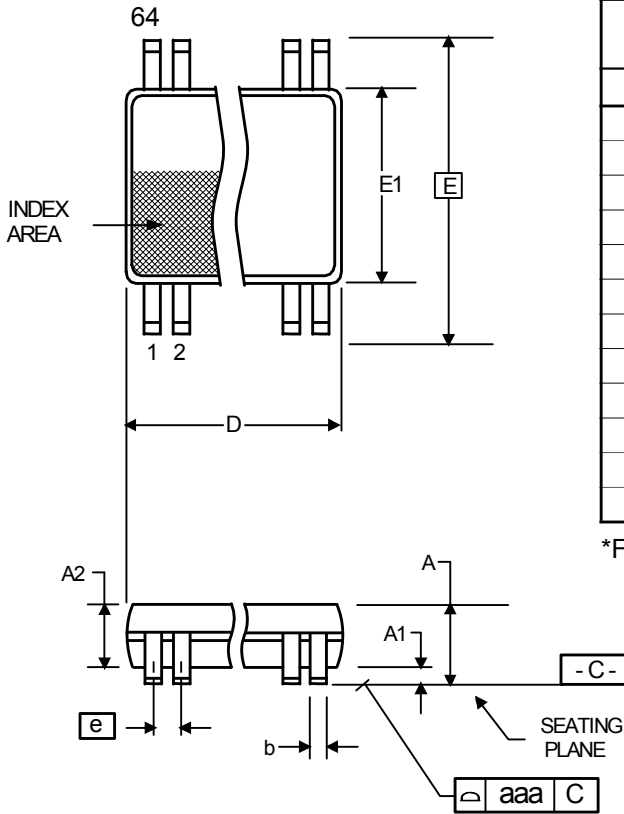


64VFQFPN

Notes:

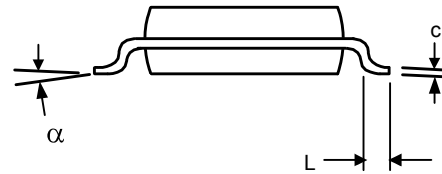
1. "L" denotes Pb-free, RoHS compliant.
2. "LOT" denotes the lot number.
3. "YYWW" denotes the last two digits and week the part was assembled.
4. "COO" denotes the country of origin.
5. "A" denotes the device revision designator.
6. Bottom marking (TSSOP only): country of origin.

Package Outline and Package Dimensions (64-pin TSSOP)

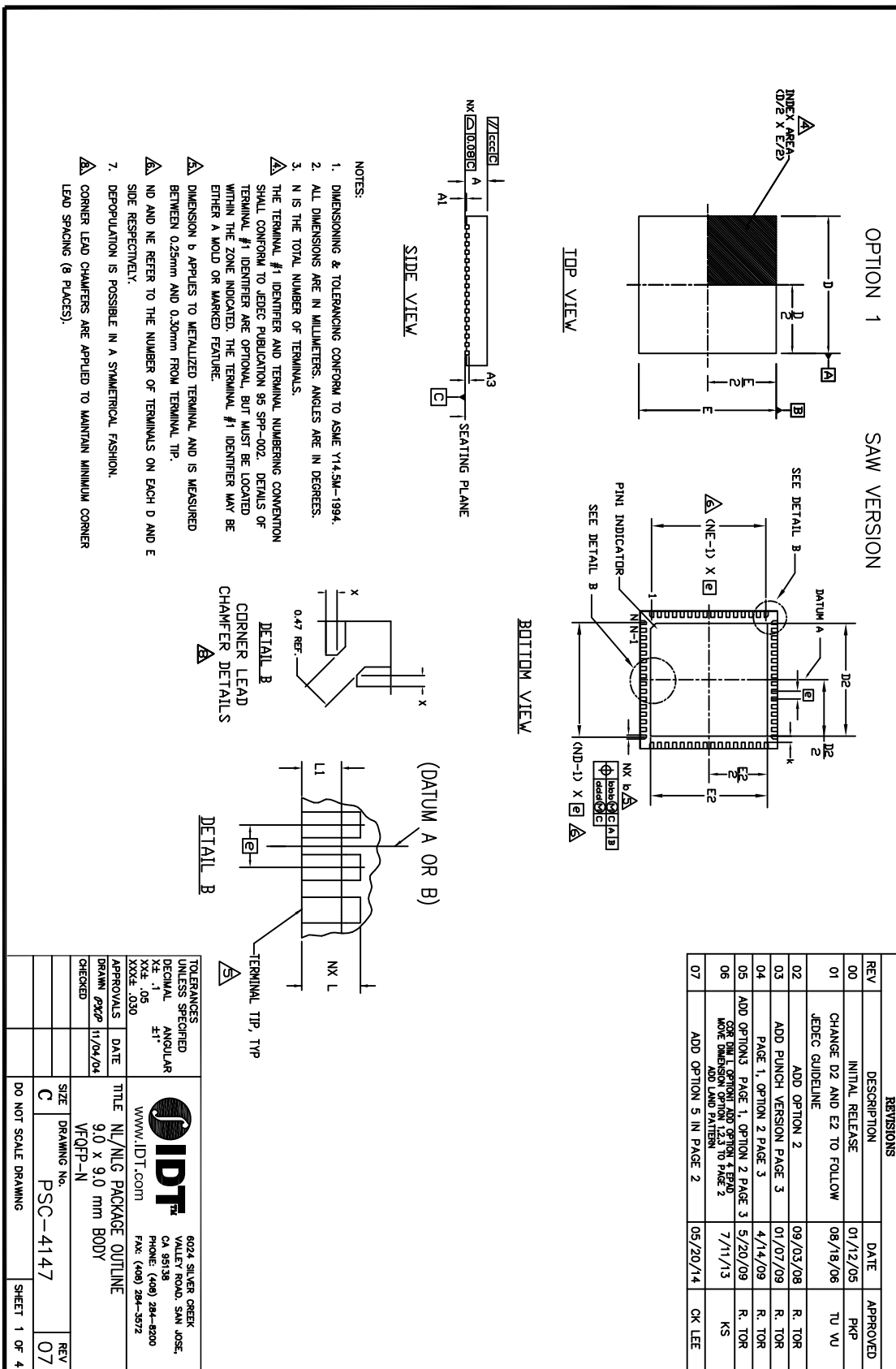


| Symbol | Millimeters | | Inches* | |
|--------|-------------|-------|-------------|------|
| | Min | Max | Min | Max |
| A | – | 1.20 | – | .047 |
| A1 | 0.05 | 0.15 | .002 | .006 |
| A2 | 0.80 | 1.05 | 0.32 | 0.41 |
| b | 0.17 | 0.27 | .007 | .011 |
| c | 0.09 | 0.20 | .0035 | .008 |
| D | 16.90 | 17.10 | .665 | .673 |
| E | 8.10 BASIC | | 0.319 BASIC | |
| E1 | 6.00 | 6.20 | .236 | .244 |
| e | 0.50 BASIC | | 0.020 BASIC | |
| aaa | – | 0.10 | – | .004 |
| L | 0.45 | 0.75 | .018 | .030 |
| a | 0° | 8° | 0° | 8° |

*For reference only. Controlling dimensions in mm.



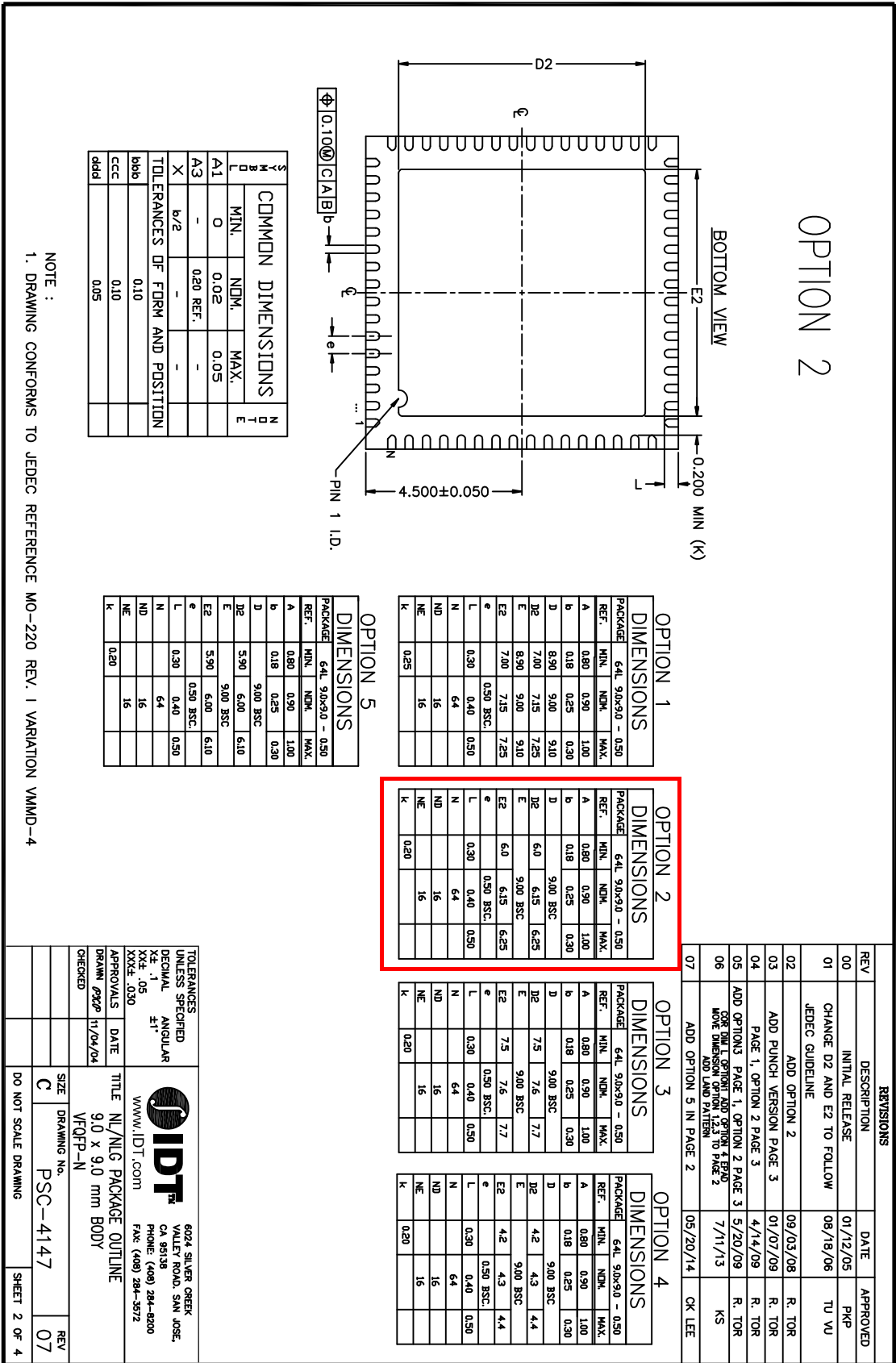
NLG64 Package Outline and Package Dimensions



| | |
|-----------------------------|----------|
| TOLERANCES UNLESS SPECIFIED | |
| DECIMAL | ANGULAR |
| XX.X | ±1° |
| XX.XX | ±0.5° |
| XXXX | ±0.50 |
| APPROVALS | |
| DRAWN | DATE |
| VFQFP-N | 11/04/04 |
| CHECKED | |
| | |
| SIZE | |
| C | |
| DO NOT SCALE DRAWING | |

| | | |
|--|---|--------|
| | 8004 SILVER CREEK VALLEY ROAD, SAN JOSE, CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-5372 | |
| | WWW.IDT.COM | |
| TITLE | | |
| NL/NLG PACKAGE OUTLINE 9.0 x 9.0 mm BODY VFQFP-N | | |
| DRAWING No. PSC-4147 | | |
| REV | SHEET | 1 OF 4 |
| 07 | | |

NLG64 Package Outline and Package Dimensions, cont. Use Option 2 dimensions table.



NOTE :
1. DRAWING CONFORMS TO JEDEC REFERENCE MO-220 REV. 1 VARIATION VMMD-4

| | |
|---|--|
| <p>TOLERANCES UNLESS SPECIFIED</p> <p>DECIMAL ANGULAR</p> <p>XX.X .05 ±1°</p> <p>XX.X .050 ±1°</p> <p>APPROVALS</p> <p>DRAWN <i>g2g</i> 11/04/04</p> <p>CHECKED</p> | <p>6024 SILVER CREEK VALLEY ROAD, SAN JOSE, CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-5572</p> <p>SIDT www.idt.com</p> <p>TITLE NL/NLG PACKAGE OUTLINE 9.0 x 9.0 mm BODY VF0FP-N</p> <p>SIZE C DRAWING No. PSC-4147</p> <p>DO NOT SCALE DRAWING</p> |
|---|--|

NLG64 Package Outline and Package Dimensions, cont. Use EPAD 6.15 option

NOTES:

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW, AS VIEWED ON PCB.
3. LAND PATTERN IN BLUE, NSMD PATTERN ASSUMED.
4. LAND PATTERN RECOMMENDATION PER IPC-7351B LP CALCULATOR.

| REVISIONS | | | |
|-----------|---|----------|----------|
| REV | DESCRIPTION | DATE | APPROVED |
| 00 | INITIAL RELEASE | 01/12/05 | PKP |
| 01 | CHANGE D2 AND E2 TO FOLLOW JEDEC GUIDELINE | 08/18/06 | TU VU |
| 02 | ADD OPTION 2 | 09/03/08 | R. TOR |
| 03 | ADD PUNCH VERSION PAGE 3 | 01/07/09 | R. TOR |
| 04 | PAGE 1, OPTION 2 PAGE 3 | 4/14/09 | R. TOR |
| 05 | ADD OPTION 3 PAGE 1, OPTION 2 PAGE 3 | 5/20/09 | R. TOR |
| 06 | CORR DIM L OPTION 4 EPAD MOVE DIMENSION OPTION 1,2,3 TO PAGE 2 ADD LAND PATTERN | 7/11/13 | KS |
| 07 | ADD OPTION 5 IN PAGE 2 | 05/20/14 | OK LEE |

TOLERANCES UNLESS SPECIFIED

| | |
|---------|---------|
| DECIMAL | ANGULAR |
| XX.X | 1° |
| XXXX.X | 0.50 |

APPROVALS

| | |
|---------|----------|
| DRAWN | DATE |
| PKP | 11/04/04 |
| CHECKED | |
| | |

IDT

6024 SILVER CREEK
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PHONE: (408) 284-8200
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WWW.IDT.COM

TITLE NLG64 PACKAGE OUTLINE
9.0 x 9.0 mm BODY
VFQFP-N

SIZE DRAWING No. PSC-4147
DO NOT SCALE DRAWING

Ordering Information

| Part / Order Number | Shipping Packaging | Package | Temperature |
|---------------------|--------------------|---------------|---------------|
| 932SQL456AGLF | Tubes | 64-pin TSSOP | 0 to +70° C |
| 932SQL456AGLFT | Tape and Reel | 64-pin TSSOP | 0 to +70° C |
| 932SQL456AKLF | Tray | 64-pin VFQFPN | 0 to +70° C |
| 932SQL456AKLFT | Tape and Reel | 64-pin VFQFPN | 0 to +70° C |
| 932SQL456AGILF | Tubes | 64-pin TSSOP | -40 to +85° C |
| 932SQL456AGILFT | Tape and Reel | 64-pin TSSOP | -40 to +85° C |
| 932SQL456AKILF | Tray | 64-pin VFQFPN | -40 to +85° C |
| 932SQL456AKILFT | Tape and Reel | 64-pin VFQFPN | -40 to +85° C |

"LF" suffix to the part number denotes Pb-Free configuration, RoHS6.6 compliant.

"A" is the device revision designator (will not correlate with the datasheet revision).

Revision History

| Rev. | Issue Date | Who | Description | Page # |
|------|------------|-----|---|-------------------------|
| A | 8/5/2015 | RDW | <ol style="list-style-type: none"> Updated front page text and data sheet title. Updated REF14 pin name to reflect 2x drive. Update pin description for REF14 pin. Moved block diagram to page 1 and pinouts to page 2. Updated block diagram to incorporate crystal recommendations. Updated Clock AC tolerance to reflected tightened c2c jitter specs on single ended outputs. Updated Clock periods table accordingly. Updated AC/DC Electrical tables with char data. Updated package drawing to latest format for NLG64. Move to final and release. | 1-14,20 |
| B | 9/29/2015 | RDW | <ol style="list-style-type: none"> Added I-temp device to data sheet Changed max power down current from 6mA to 8mA Slight updates to PCIe Gen2 Hi-band and SAS12G for -40C Corrected typo in bit name of Byte 1, bit 7. Updated marking diagrams to include I-temp devices Updated ordering information to include I-temp devices. | 1,9,12, 15,17, 22 |



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(Disclaimer Rev.1.01 Jan 2024)

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