

Description

DDR & SDRAM fanout buffer, for VIA Pro 266, KT266 and P4X266 DDR chipsets

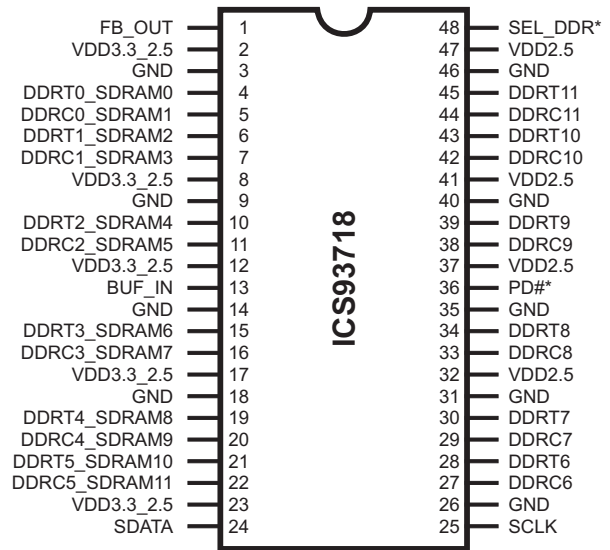
Output Features

- Low skew, fanout buffer
- 1 to 12 differential clock distribution
- I²C for functional and output control
- Feedback pin for input to output synchronization
- Supports up to 4 DDR DIMMs or 3 SDRAM DIMMs + 2 DDR DIMMs
- Frequency supports up to 200MHz (DDR400)
- Supports Power Down Mode for power management
- CMOS level control signal input

Key Specifications

- OUTPUT - OUTPUT skew: <100ps
- Output Rise and Fall Time for DDR outputs: 500ps - 700ps
- DUTY CYCLE: 47% - 53%
- 48-pin SSOP package
- Available in RoHS compliant packaging

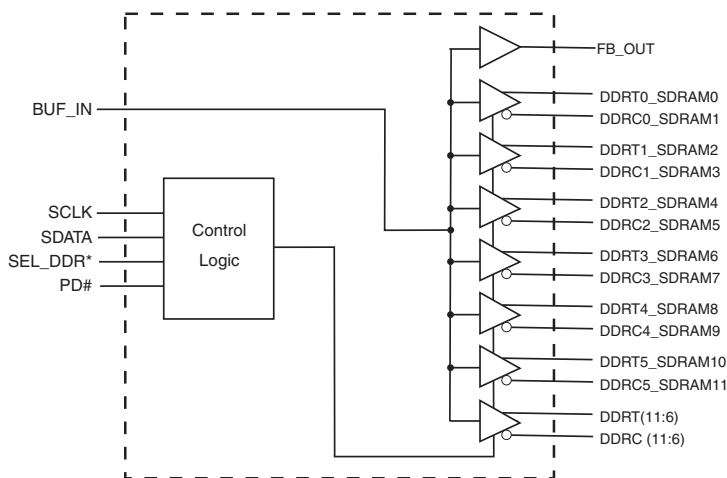
Pin Configuration



48-Pin SSOP

*Internal Pull-up Resistor of 120K to VDD

Functional Block Diagram



Functionality Table

| MODE | PIN 48 | VDD 3.3_2.5 | PIN 4, 5, 6, 7, 10, 11, 15, 16, 19, 20, 21, 22 |
|----------------|-----------|----------------|--|
| DDR Mode | SEL_DDR=1 | 2.5V | These outputs will be DDR outputs |
| DDR/SD Mode | SEL_DDR=0 | 3.3V | These outputs will be standard SDRAM outputs |

Pin Description

| PIN NUMBER | PIN NAME | TYPE | DESCRIPTION |
|-------------------------------------|---|------|--|
| 1 | FB_OUT | OUT | Feedback output, dedicated for external feedback |
| 2, 8, 12, 17, 23, | VDD3.3_2.5 | PWR | 2.5V or 3.3V voltage supply to pins 4, 5, 6, 7, 10, 11, 15, 16, 19, 20, 21, 22 |
| 3, 9, 14, 18, 26, 31, 35, 40, 46 | GND | PWR | Ground |
| 45, 43, 39, 34, 30, 28, | DDRT (11:6) | OUT | "True" Clock of differential pair outputs. |
| 44, 42, 38, 33, 29, 27, | DDRC (11:6) | OUT | "Complementary" clocks of differential pair outputs. |
| 21, 19, 15, 10, 6, 4 | DDRT (5:0) SDRAM (10, 8, 6, 4, 2, 0) | OUT | "True" Clock of differential pair outputs, or 3.3V SDRAM clock outputs depending on SEL_DDR input |
| 22, 20, 16, 11, 7, 5 | DDRC (5:0) SDRAM (11, 9, 7, 5, 3, 1,) | OUT | "Complementary" clocks of differential pair outputs, or 3.3V SDRAM clock outputs depending on SEL_DDR input |
| 13 | BUF_IN | IN | Single ended buffer input |
| 24 | SDATA | I/O | Data pin for I ² C circuitry 5V tolerant |
| 25 | SCLK | IN | Clock input of I ² C input, 5V tolerant input |
| 32, 37, 41, 47 | VDD2.5 | PWR | 2.5V voltage supply |
| 36 | PD# | IN | Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled. The latency of the power down will not be greater than 3ms. |
| 48 | SEL_DDR | IN | Select input for DDR mode or DDR/SD mode 0=DDR/SD mode 1=DDR mode |

General I²C serial interface information

The information in this section assumes familiarity with I²C programming.
For more information, contact ICS for an I²C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D4_(H)
- ICS clock will **acknowledge**
- Controller (host) sends a dummy command code
- ICS clock will **acknowledge**
- Controller (host) sends a dummy byte count
- ICS clock will **acknowledge**
- Controller (host) starts sending first byte (Byte 0) through byte 6
- ICS clock will **acknowledge** each byte **one at a time**.
- Controller (host) sends a Stop bit

| How to Write: | |
|------------------------------|----------------------|
| Controller (Host) | ICS (Slave/Receiver) |
| Start Bit | |
| Address D4 _(H) | |
| | ACK |
| Dummy Command Code | |
| | ACK |
| Dummy Byte Count | |
| | ACK |
| Byte 0 | |
| | ACK |
| Byte 1 | |
| | ACK |
| Byte 2 | |
| | ACK |
| Byte 3 | |
| | ACK |
| Byte 4 | |
| | ACK |
| Byte 5 | |
| | ACK |
| Byte 6 | |
| | ACK |
| Byte 7 | |
| | ACK |
| Stop Bit | |

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D5_(H)
- ICS clock will **acknowledge**
- ICS clock will send the **byte count**
- Controller (host) acknowledges
- ICS clock sends first byte (**Byte 0**) through **byte 7**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

| How to Read: | |
|------------------------------|----------------------|
| Controller (Host) | ICS (Slave/Receiver) |
| Start Bit | |
| Address D5 _(H) | |
| | ACK |
| | Byte Count |
| ACK | |
| | Byte 0 |
| ACK | |
| | Byte 1 |
| ACK | |
| | Byte 2 |
| ACK | |
| | Byte 3 |
| ACK | |
| | Byte 4 |
| ACK | |
| | Byte 5 |
| ACK | |
| | Byte 6 |
| ACK | |
| | Byte 7 |
| Stop Bit | |

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol.**
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

Byte 6: Output Control
(1= enable, 0 = disable)

| BIT | PIN# | PWD | DESCRIPTION |
|-------|--------|-----|--------------------------|
| Bit 7 | 48 | 1 | SEL_DDR (Read back only) |
| Bit 6 | - | 1 | (Reserved) |
| Bit 5 | - | 1 | (Reserved) |
| Bit 4 | - | 1 | (Reserved) |
| Bit 3 | 45, 44 | 1 | DDRT11, DDRC11 |
| Bit 2 | 43, 42 | 1 | DDRT10, DDRC10 |
| Bit 1 | 39, 38 | 1 | DDRT9, DDRC9 |
| Bit 0 | 34, 33 | 1 | DDRT8, DDRC8 |

Byte 7: Output Control
(1= enable, 0 = disable)

| BIT | PIN# | PWD | DESCRIPTION |
|-------|--------|-----|---------------------------------|
| Bit 7 | 30, 29 | 1 | DDRT7, DDRC7 |
| Bit 6 | 28, 27 | 1 | DDRT6, DDRC6 |
| Bit 5 | 21, 22 | 1 | DDRT5, SDRAM10 DDRC5_SDRAM11 |
| Bit 4 | 19, 20 | 1 | DDRT4_SDRAM8 DDRC4_SDRAM9 |
| Bit 3 | 15, 16 | 1 | DDRT3_SDRAM6 DDRC3_SDRAM7 |
| Bit 2 | 10, 11 | 1 | DDRT2_SDRAM4 DDRC2_SDRAM5 |
| Bit 1 | 6, 7 | 1 | DDRT1_SDRAM2 DDRC1_SDRAM3 |
| Bit 0 | 4, 5 | 1 | DDRT0_SDRAM1 DDRC0_SDRAM0 |

Absolute Max

| | |
|-------------------------------|--------------------------------------|
| Supply Voltage (VDD & VDD2.5) | -0.5V to 3.6V |
| Logic Inputs | GND -0.5 V to V _{DD} +0.5 V |
| Ambient Operating Temperature | 0°C to +85°C |
| Case Temperature | 115°C |
| Storage Temperature | -65°C to +150°C |

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

SEL_DDR = 0 SDRAM Outputs V_{DD} = 3.3V, T_A = 0 - 85°C; (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------|------------------------|---|------|------|-----|-------|
| Input High Current | I _{IH} | V _I = V _{DD} or GND | | 1 | 10 | μA |
| Input Low Current | I _{IL} | V _I = V _{DD} or GND | -100 | -20 | | μA |
| Operating Supply Current | I _{DD3.3 2.5} | C _L = 0pf, 133MHz | | 200 | 250 | mA |
| | I _{DD2.5} | C _L = 0pf, 133MHz | | 100 | 200 | mA |
| | I _{DDPD} | C _L = 0pf, all frequencies | | 3 | 10 | mA |
| Output High Current | I _{OH} | V _{DD} = 3.3V, V _{OUT} = 1V | | -74 | -18 | mA |
| Output Low Current | I _{OL} | V _{DD} = 3.3V, V _{OUT} = 1.2V | 26 | 42 | | mA |
| High-level output voltage | V _{OH} | V _{DD} = 3.3V, | 2 | 2.95 | | V |
| | | V _{OH} = -12mA | | | | |
| Low-level output voltage | V _{OL} | V _{DD} = 3.3V | | 0.35 | 0.4 | |
| | | I _{OH} = 12mA | | | | |
| Input Capacitance ¹ | C _{IN} | V _I = GND or V _{DD} | | 2 | | pF |

¹Guaranteed by design, not 100% tested in production.

Recommended Operating Condition

SEL_DDR=0 SDRAM Outputs V_{DD}=3.3V, T_A = 0 - 85°C; (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|----------------------|------------------------|--------------------|-----|-----------------|-----|-------|
| Power Supply Voltage | V _{DD3.3 2.5} | | 3.0 | 3.3 | 3.6 | V |
| | V _{DD2.5} | | 2.3 | 2.5 | 2.7 | |
| Input High Voltage | V _{IH} | SEL_DDR, PD# input | 2.0 | | | V |
| Input Low Voltage | V _{IL} | SEL_DDR, PD# input | | | 0.8 | V |
| Input voltage level | V _{IN} | | | V _{DD} | | V |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

SEL_DDR = 1 DDR/DDR_SDRAM Outputs $V_{DD}=2.5$, $T_A = 0 - 85^\circ\text{C}$; (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|-------------|--|--------------------|-------|--------------------|---------------|
| Input High Current | I_{IH} | $V_I = V_{DD}$ or GND | | 1 | 10 | μA |
| Input Low Current | I_{IL} | $V_I = V_{DD}$ or GND | -100 | -25 | | μA |
| Operating Supply Current | $I_{DD2.5}$ | $C_L = 0\text{pf}$, 133MHz | | 76 | 200 | mA |
| | I_{DDPD} | $C_L = 0\text{pf}$, all | | 3 | 10 | mA |
| Output High Current | I_{OH} | $V_{DD} = 2.5\text{V}$, $V_{OUT} = 1\text{V}$ | | -74.5 | -18 | mA |
| Output Low Current | I_{OL} | $V_{DD} = 2.5\text{V}$, $V_{OUT} =$ | 26 | 42.5 | | mA |
| High-level output voltage | V_{OH} | $V_{DD} = 2.5\text{V}$, | 1.7 | 2.3 | | V |
| | | $V_{OH} = -12\text{mA}$ | | | | |
| Low-level output voltage | V_{OL} | $V_{DD} = 2.5\text{V}$ | | 0.35 | 0.46 | |
| | | $I_{OH} = 12\text{mA}$ | | | | |
| Output differential-pair crossing voltage | V_{OC} | | $(V_{DD}/2) - 0.1$ | 1.25 | $(V_{DD}/2) + 0.1$ | V |
| Input Capacitance ¹ | C_{IN} | $V_I = \text{GND}$ or V_{DD} | | 2 | | pF |

¹Guaranteed by design, not 100% tested in production.

Recommended Operating Condition

SEL_DDR=1 DDR/DDR_SDRAM Outputs = 2.5V, $T_A = 0 - 85^\circ\text{C}$ (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|----------------------|------------------|--------------------|-----|----------|-----|-------|
| Power Supply Voltage | $V_{DD3.3\ 2.5}$ | | 2.3 | 2.5 | 2.7 | V |
| | $V_{DD2.5}$ | | 2.3 | 2.5 | 2.7 | |
| Input High Voltage | V_{IH} | SEL_DDR, PD# input | 2.0 | | | V |
| Input Low Voltage | V_{IL} | SEL_DDR, PD# input | | | 0.8 | V |
| Input voltage level | V_{IN} | | | V_{DD} | | V |

¹Guaranteed by design, not 100% tested in production.

Switching Characteristics

DDR_Mode (SEL_DDR = 1), VDD = 2.5±5%

| PARAMETER | SYMBOL | CONDITION | MIN | TYP | MAX | UNITS |
|------------------------------------|------------|--|-----|-----|-----|-------|
| Operating Frequency | | | 66 | 133 | 200 | MHz |
| Input clock duty cycle | d_{tin} | | 40 | 50 | 60 | % |
| Output to Output Skew | T_{skew} | Output crossover skew DDR[0:11] | | 80 | 100 | ps |
| Duty cycle | D_C^2 | 66MHz to 100MHz, w/loads | 48 | 49 | 52 | % |
| | | 101MHz to 167MHz, w/loads | 47 | 50 | 53 | % |
| Rise Time, Fall Time (DDR Outputs) | trd, tfd | Measured between 20% and 80% output, w/loads | 500 | 600 | 700 | ps |

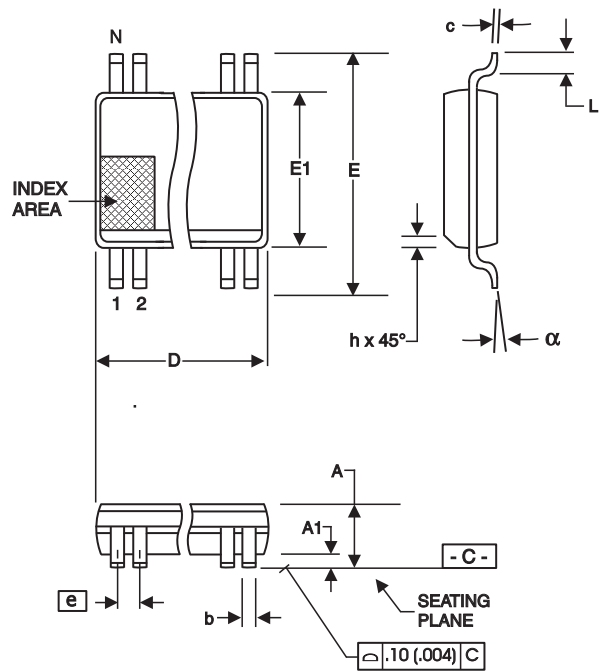
Switching Characteristics

SD_Mode (SEL_DDR = 0), VDD = 3.3±5%

| PARAMETER | SYMBOL | CONDITION | MIN | TYP | MAX | UNITS |
|--|------------|---|-----|-----|-----|-------|
| Operating Frequency | | | 66 | 133 | 200 | MHz |
| Input clock duty cycle | d_{tin} | | 40 | 50 | 60 | % |
| Output to Output Skew | T_{skew} | $V_T = 1.50V$ | | 150 | | ps |
| Duty cycle | D_C^2 | 66MHz to 200MHz | | 54 | | % |
| Rise Time, Fall Time (SDRAM Outputs) | trs, tfs | $V_{OL} = 0.4V, V_{OH} = 2.4V, w/loads$ | 0.5 | 1.5 | 1.7 | ns |
| SDRAM Buffer LH Prop. Delay ¹ | t^{PLH} | Input edge greater than 1V/ns | | 2 | 2.5 | ns |
| SDRAM Bufer HL Prop. Delay ¹ | t^{PHL} | Input edge greater than 1V/ns | | 1.9 | 2.5 | ns |

Notes:

1. Refers to transition on non-inverting output.
2. While the pulse skew is almost constant over frequency, the duty cycle error increases at higher frequencies. This is due to the formula: duty cycle= t_2/t_1 , were the cycle (t_1) decreases as the frequency goes up.



300 mil SSOP

300 mil SSOP

| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|--------|-------------------------------------|-------|--------------------------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 2.41 | 2.80 | .095 | .110 |
| A1 | 0.20 | 0.40 | .008 | .016 |
| b | 0.20 | 0.34 | .008 | .0135 |
| c | 0.13 | 0.25 | .005 | .010 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 10.03 | 10.68 | .395 | .420 |
| E1 | 7.40 | 7.60 | .291 | .299 |
| e | 0.635 BASIC | | 0.025 BASIC | |
| h | 0.38 | 0.64 | .015 | .025 |
| L | 0.50 | 1.02 | .020 | .040 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| alpha | 0° | | 8° | |

VARIATIONS

| N | D mm. | | D (inch) | |
|----|-------|-------|----------|------|
| | MIN | MAX | MIN | MAX |
| 48 | 15.75 | 16.00 | .620 | .630 |

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

ICS93718yFLFT

Example:

ICS XXXX y F LF - T

Designation for tape and reel packaging

Lead Free (optional)

Package Type
F = SSOP

Revision Designator (will not correlate with datasheet revision)

Device Type (consists of 3 or 4 digit numbers)

Prefix

ICS, AV = Standard Device

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