Low Cost DDR Phase Lock Loop Zero Delay Buffer

93722

Description

DDR Zero Delay Clock Buffer

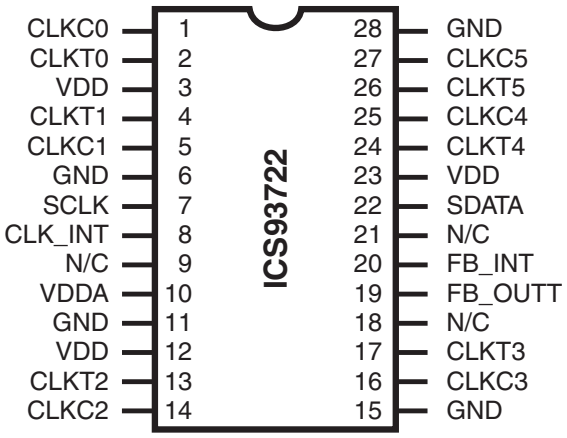
Output Features

- Low skew, low jitter PLL clock driver
- I^2C for functional and output control
- Feedback pins for input to output synchronization
- Spread Spectrum tolerant inputs
- 3.3V tolerant CLK_INT input

Key Specifications

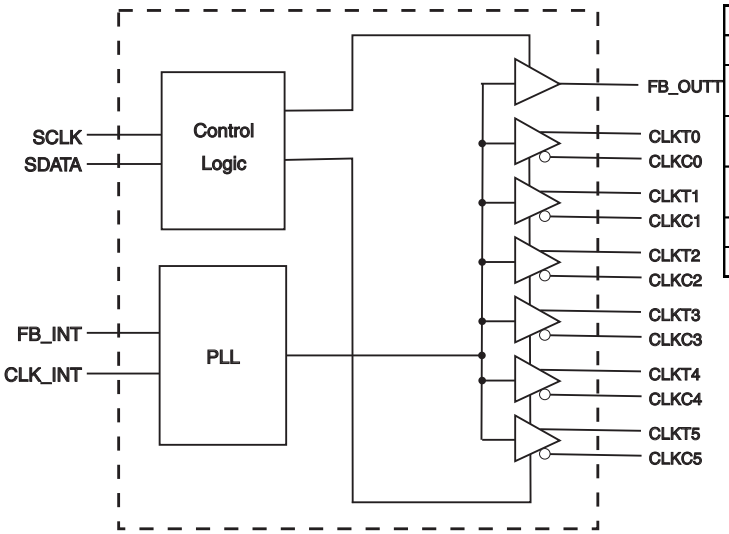
- PEAK - PEAK jitter (66MHz): <120ps
- PEAK - PEAK jitter (>100MHz): <75ps
- CYCLE - CYCLE jitter (66MHz):<110ps
- CYCLE - CYCLE jitter (>100MHz):<65ps
- OUTPUT - OUTPUT skew: <100ps
- Output Rise and Fall Time: 650ps - 950ps
- DUTY CYCLE: 49.5% - 50.5%

Pin Configuration



28-Pin SSOP

Functional Block Diagram



Functionality Table

INPUTS		OUTPUTS			PLL State
AVDD	CLK_INT	CLKT	CLKC	FB_OUT	
2.5V (nom)	L	L	H	L	on
2.5V (nom)	H	H	L	H	on
2.5V (nom)	<20MHz	Z	Z	Z	off
GND	L	L	H	L	Bypassed/off
GND	H	H	L	H	Bypassed/off

Pin Description

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
6, 11, 15, 28	GND	PWR	Ground
27, 25, 16, 14, 5, 1	CLKC(5:0)	OUT	"Complementary" clocks of differential pair outputs.
26, 24, 17, 13, 4, 2	CLKT(5:0)	OUT	"True" Clock of differential pair outputs.
3, 12, 23	VDD	PWR	Power supply 2.5V
7	SCLK	IN	Clock input of I^2C input, 5V tolerant input
8	CLK_INT	IN	"True" reference clock input
9, 18, 21	N/C	-	Not connected
10	VDDA	PWR	Analog power supply, 2.5V
19	FB_OUTT	OUT	"True" Feedback output, dedicated for external feedback. It switches at the same frequency as the CLK. This output must be wired to FB_INT.
20	FB_INT	IN	"True" Feedback input, provides feedback signal to the internal PLL for synchronization with CLK_INT to eliminate phase error.
22	SDATA	IN	Data input for I^2C serial input, 5V tolerant input

Bytes 0 to 4 are reserved power up default = 1.

Byte 5: Output Control
(1= enable, 0 = disable)

Bit	PIN#	PWD	DESCRIPTION
Bit7	2, 1	1	CLK0 (T&C)
Bit6	4, 5	1	CLK1 (T&C)
Bit5		1	Reserved
Bit4		1	Reserved
Bit3	13, 14	1	CLK2 (T&C)
Bit2	17, 16	1	CLK3 (T&C)
Bit1		1	Reserved
Bit0		1	Reserved

Note: PWD = Power Up Default

Byte 6: Output Control
(1= enable, 0 = disable)

Bit	PIN#	PWD	DESCRIPTION
Bit7		1	Reserved
Bit6		1	Reserved
Bit5		1	Reserved
Bit4		1	Reserved
Bit3	24, 25	1	CLK4 (T&C)
Bit2		1	Reserved
Bit1	26, 27	1	CLK5 (T&C)
Bit0		1	Reserved

Absolute Max

Supply Voltage (VDD & AVDD)	-0.5V to 3.6V
Logic Inputs	GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature	0°C to +85°C
Case Temperature	115°C
Storage Temperature	–65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input / Supply / Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 2.5 V +/-0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Current	I_{IH}	$V_{IN} = V_{DD}$ or GND		1	10	µA
Input Low Current	I_{IL}	$V_{IN} = V_{DD}$ or GND	-100	-20		µA
Operating Supply Current	$I_{DD2.5}$	C_L = 0 pF at 133 MHz		275	325	mA
	I_{DDPD}	C_L = 0 pF			100	µA
Output High Current	I_{OH}	V_{DD} = 2.3V, V_{OUT} = 1V		-43	-18	mA
Output High Current	I_{OL}	V_{DD} = 2.3V, V_{OUT} = 1.2V	26	43		mA
High Impedance Output Current	I_{OZ}	V_{DD} = 2.7V, $V_{OUT} = V_{DD}$ or GND			10	µA
Input Clamp Voltage	V_{IK}	I_{IN} = -18 mA;				V
High-level Output Voltage	V_{OH}	V_{DD} = min to max, I_{OH} = -1mA	2.1	2.42		V
		V_{DD} = 2.3V, I_{OH} = -12mA		1.87		V
Low-level Output Voltage	V_{OL}	V_{DD} = min to max, I_{OH} = 1mA		0.04	0.1	V
		V_{DD} = 2.3V, I_{OH} = 12mA		0.35	0.6	V
Input Capacitance[1]	C_{IN}	$V_{IN} = V_{DD}$ or GND		2		pF
Output Capacitance[1]	C_{OUT}	$V_{OUT} = V_{DD}$ or GND		3		pF

1. Guaranteed by design, not 100% tested in production.

Recommended Operating Condition (see note 1)

T_A = 0 - 70°C; Supply Voltage AV_{DD}, V_{DD} = 2.5 V +/-0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog / Core Supply Voltage	V_{DD}, AV_{DD}		2.3	2.5	2.7	V
Input Voltage Level	V_{IL}				V_{DD}/2 - 0.5V	V
	V_{IH}		V_{DD}/2 + 0.5V			V
Inpu Duty Cycle	I_{DC}		40		60	
Input max jitter	I_{TCYC}				500	ps

Timing Requirements

T_A = 0 - 70°C; Supply Voltage AV_{DD}, V_{DD} = 2.5 V +/-0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Clock Frequency[1]	$freq_{op}$		66		200	MHz
Input Clock Duty Cycle[1]	d_{tin}		40		60	%
Clock Stabilization[1]	t_{STAB}	from V_{DD} = 2.5V to 1% target frequency			100	s

1. Guaranteed by design, not 100% tested in production.

Switching Characteristics

T_A = 0 - 70°C; Supply Voltage V_{DD} = 2.5 V +/-0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Absolute Jitter[1]	T_{jabs}	66 MHz			120	ps
		100 - 200 MHz			75	
Cycle to cycle Jitter[1,2]	$T_{cyc-cyc}$	66 MHz		50	110	ps
		100 - 200 MHz		25	65	
Phase Error[1]	$t_{(phase\ error)}$	CLK_INT to FB_INT	-150	50	150	ps
Output to output Skew[1]	T_{skew}	V_T = 50%		70	100	ps
Pulse Skew[1]	T_{skewp}				100	ps
Duty Cycle (differential)[1,3]	D_C	V_T = 50%, 66 MHz to 100 MHz	49.5	50	50.5	%
		V_T = 50%, 101 MHz to 167 MHz	49	50	51	
Rise Time, Fall Time[1]	t_R, t_F	Single-ended 20 - 80 % Load = 120 / 12 pF	450	550	950	ps

1. Guaranteed by design, not 100% tested in production.
2. Refers to transistion on non-inverting output.
3. While the pulse skew is almost constant over frequency, the duty cycle error increases at higher frequencies. This is due to the formula: duty cycle = t_{wH} / t_C, where the cycle time (t_C) decreases as the frequency increases.

General I²C serial interface information

The information in this section assumes familiarity with I²C programming.
For more information, contact IDT for an I²C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D4_{(H)}$
- IDT clock will ***acknowledge***
- Controller (host) sends a dummy command code
- IDT clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- IDT clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 6
- IDT clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address $D5_{(H)}$
- IDT clock will ***acknowledge***
- IDT clock will send the ***byte count***
- Controller (host) acknowledges
- IDT clock sends first byte ***(Byte 0) through byte 7***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Write:

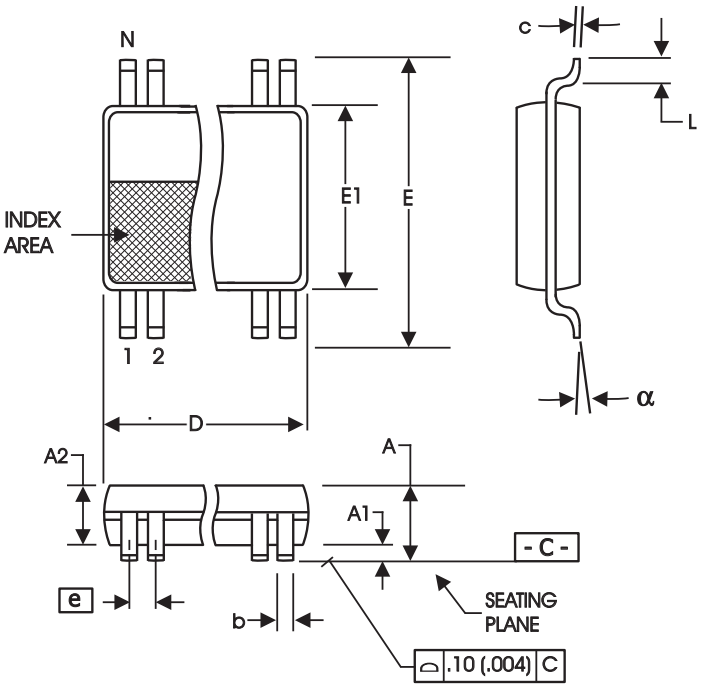
Controller (Host)	IDT (Slave/Receiver)
Start Bit	
Address $D4_{(H)}$	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Byte 6	
	ACK
Byte 7	
	ACK
Stop Bit	

How to Read:

Controller (Host)	IDT (Slave/Receiver)
Start Bit	
Address $D5_{(H)}$	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
	Byte 6
ACK	
	Byte 7
Stop Bit	

Notes:

1. The IDT clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.



209 mil SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	-	2.00	-	.079
A1	0.05	-	.002	-
A2	1.65	1.85	.065	.073
b	0.22	0.38	.009	.015
c	0.09	0.25	.0035	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	7.40	8.20	.291	.323
E1	5.00	5.60	.197	.220
e	0.65 BASIC		0.0256 BASIC	
L	0.55	0.95	.022	.037
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
28	9.90	10.50	.390	.413

MO-150 JEDEC
Doc.# 10-0033
6/1/00 Rev B

Ordering Information

93722yFLFT

Example:

XXXX y F LF T

- **Designation for tape and reel packaging**
- **Annealed Lead Free (optional)**
- **Package Type**
  F = SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 or 4 digit numbers)**

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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