

Description

The 9FGU0241 is a member of IDT's 1.5V Ultra-Low-Power PCIe clock family with integrated output terminations providing $Z_o=100\Omega$. The device has 2 output enables for clock management, 2 different spread spectrum levels in addition to spread off and 2 selectable SMBus addresses.

Recommended Application

1.5V PCIe Gen1-2-3 clock generator

Output Features

- 2 - 100MHz Low-Power (LP) HCSL DIF pairs w/ $Z_o=100\Omega$
- 1 - 1.5V LVCMOS REF output w/Wake-On-LAN (WOL) support

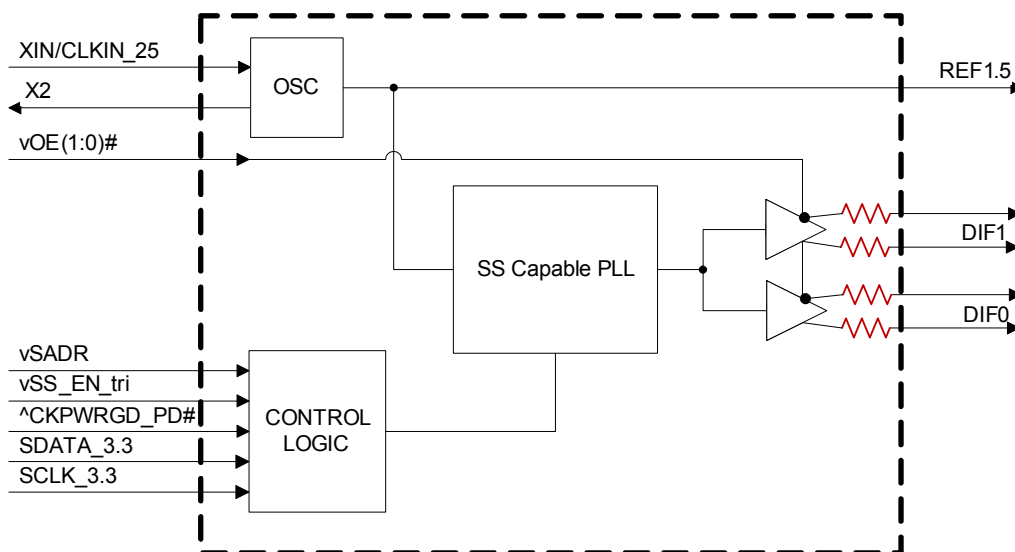
Key Specifications

- DIF cycle-to-cycle jitter <50ps
- DIF output-to-output skew <50ps
- DIF phase jitter is PCIe Gen1-2-3 compliant
- REF phase jitter is < 3.0ps RMS

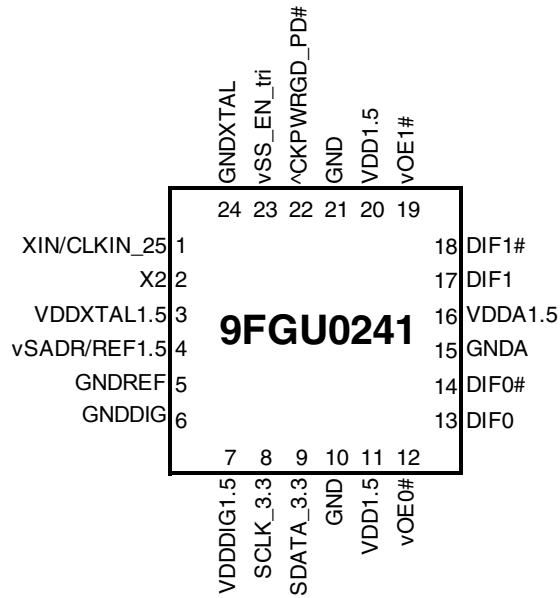
Features/Benefits

- Direct connection to 100ohm transmission lines; saves 16 resistors compared to standard PCIe devices
- 23mW typical power consumption; reduced thermal concerns
- OE# pins; support DIF power management
- Programmable Slew rate for each output; allows tuning for various line lengths
- Programmable output amplitude; allows tuning for various application environments
- DIF outputs blocked until PLL is locked; clean system start-up
- Selectable 0%, -0.25% or -0.5% spread on DIF outputs; reduces EMI
- External 25MHz crystal; supports tight ppm with 0 ppm synthesis error
- Configuration can be accomplished with strapping pins; SMBus interface not required for device control
- Selectable SMBus addresses; multiple devices can easily share an SMBus segment
- 3.3V tolerant SMBus interface works with legacy controllers
- Space saving 24-pin 4x4 mm VFQFPN; minimal board space

Block Diagram



Pin Configuration



24-pin VQFPN, 4x4 mm, 0.5mm pitch

^ prefix indicates internal 120KOhm pull up resistor
v prefix indicates internal 120KOhm pull down resistor

SMBus Address Selection Table

| | SADR | Address | + Read/Write Bit |
|---|------|---------|------------------|
| State of SADR on first application of CKPWRGD_PD# | 0 | 1101000 | x |
| | 1 | 1101010 | x |

Power Management Table

| CKPWRGD_PD# | SMBus OE bit | DIFx | | REF |
|-------------|--------------|----------|-----------|-------------------|
| | | True O/P | Comp. O/P | |
| 0 | X | Low | Low | Hi-Z ¹ |
| 1 | 1 | Running | Running | Running |
| 1 | 0 | Low | Low | Low |

1. REF is Hi-Z until the 1st assertion of CKPWRGD_PD# high. After this, when CKPWRGD_PD# is low, REF is Low.

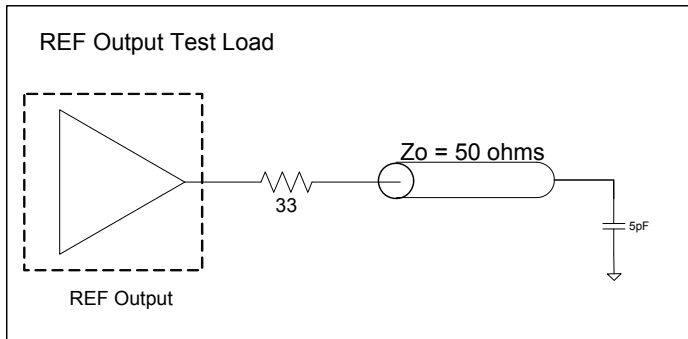
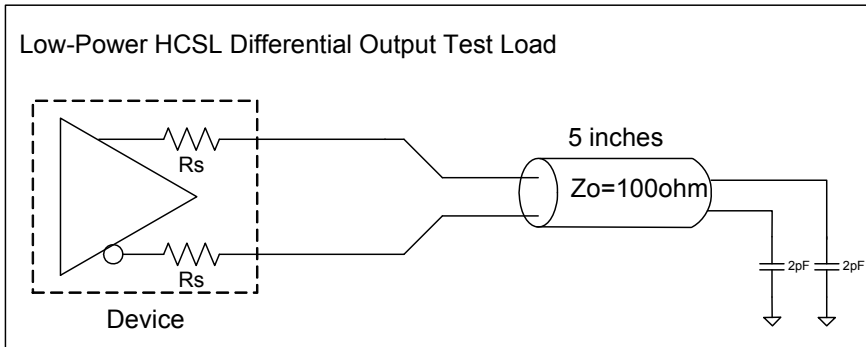
Power Connections

| Pin Number | VDD | GND | Description |
|------------|------|-------|---------------|
| 3 | 5,24 | | XTAL, REF |
| 7 | | 6 | Digital Power |
| 11,20 | | 10,21 | DIF outputs |
| 16 | | 15 | PLL Analog |

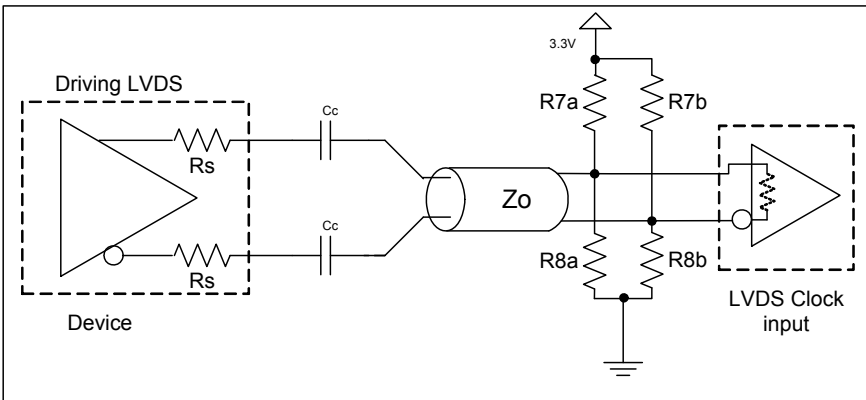
Pin Descriptions

| Pin# | Pin Name | Type | Pin Description |
|------|--------------|-------------|---|
| 1 | XIN/CLKIN_25 | IN | Crystal input or Reference Clock input. Nominally 25MHz. |
| 2 | X2 | OUT | Crystal output. |
| 3 | VDDXTAL1.5 | PWR | Power supply for XTAL, nominal 1.5V |
| 4 | vSADR/REF1.5 | LATCHED I/O | Latch to select SMBus Address/1.5V LVCMOS copy of X1/REFIN pin |
| 5 | GNDREF | GND | Ground pin for the REF outputs. |
| 6 | GNDDIG | GND | Ground pin for digital circuitry |
| 7 | VDDDIG1.5 | PWR | 1.5V digital power (dirty power) |
| 8 | SCLK_3.3 | IN | Clock pin of SMBus circuitry, 3.3V tolerant. |
| 9 | SDATA_3.3 | I/O | Data pin for SMBus circuitry, 3.3V tolerant. |
| 10 | GND | GND | Ground pin. |
| 11 | VDD1.5 | PWR | Power supply, nominally 1.5V |
| 12 | vOE0# | IN | Active low input for enabling DIF pair 0. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 13 | DIF0 | OUT | Differential true clock output |
| 14 | DIF0# | OUT | Differential Complementary clock output |
| 15 | GND | GND | Ground pin for the PLL core. |
| 16 | VDDA1.5 | PWR | 1.5V power for the PLL core. |
| 17 | DIF1 | OUT | Differential true clock output |
| 18 | DIF1# | OUT | Differential Complementary clock output |
| 19 | vOE1# | IN | Active low input for enabling DIF pair 1. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 20 | VDD1.5 | PWR | Power supply, nominally 1.5V |
| 21 | GND | GND | Ground pin. |
| 22 | ^CKPWRGD_PD# | IN | Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor. |
| 23 | vSS_EN_tri | LATCHED IN | Latched select input to select spread spectrum amount at initial power up : 1 = -0.5% spread, M = -0.25%, 0 = Spread Off |
| 24 | GNDXTAL | GND | GND for XTAL |

Test Loads



Alternate Terminations



Driving LVDS inputs

| Component | Value | | Note |
|-----------|--------------------------|------------------------------------|------|
| | Receiver has termination | Receiver does not have termination | |
| R7a, R7b | 10K ohm | 140 ohm | |
| R8a, R8b | 5.6K ohm | 75 ohm | |
| Cc | 0.1 uF | 0.1 uF | |
| Vcm | 1.2 volts | 1.2 volts | |

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9FGU0241. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---------------------------|--------------------|---------------------------|------|-----|-----------------------|-------|-------|
| Supply Voltage | VDDxx | Applies to all VDD pins | -0.5 | | 2 | V | 1,2 |
| Input Voltage | V _{IN} | | -0.5 | | V _{DD} +0.5V | V | 1,3 |
| Input High Voltage, SMBus | V _{IHSMB} | SMBus clock and data pins | | | 3.3V | V | 1 |
| Storage Temperature | T _s | | -65 | | 150 | °C | 1 |
| Junction Temperature | T _j | | | | 125 | °C | 1 |
| Input ESD protection | ESD prot | Human Body Model | 2000 | | | V | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Operation under these conditions is neither implied nor guaranteed.

³Not to exceed 2.5V.

Electrical Characteristics—Current Consumption

TA = T_{AMB}; Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|--------------------|--|-----|-----|-----|-------|-------|
| Operating Supply Current | I _{DDAOP} | VDDA, All outputs active @100MHz | | 6.6 | 9 | mA | |
| | I _{DDOP} | All VDD, except VDDA and VDDIO, All outputs active @100MHz | | 10 | 14 | mA | |
| Wake-on-LAN Current (CKPWRGD_PD# = '0' Byte 3, bit 5 = '1') | I _{DDAPD} | VDDA, DIF outputs off, REF output running | | 0.4 | 1 | mA | 2 |
| | I _{DDPD} | All VDD, except VDDA and VDDIO, DIF outputs off, REF output running | | 3.8 | 6 | mA | 2 |
| Powerdown Current (CKPWRGD_PD# = '0' Byte 3, bit 5 = '0') | I _{DDAPD} | VDDA, all outputs off | | 0.4 | 1 | mA | |
| | I _{DDPD} | All VDD, except VDDA and VDDIO, all outputs off | | 0.4 | 1 | mA | |

¹Guaranteed by design and characterization, not 100% tested in production.

²This is the current required to have the REF output running in Wake-on-LAN mode (Byte 3, bit 5 = 1)

Electrical Characteristics—DIF Output Duty Cycle, Jitter, and Skew Characteristics

TA = T_{AMB}; Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|----------------------|------------------------------------|-----|-----|-----|-------|-------|
| Duty Cycle | t _{DC} | Measured differentially, PLL Mode | 45 | 50 | 55 | % | 1,2 |
| Skew, Output to Output | t _{sk3} | Averaging on, V _T = 50% | | 32 | 50 | ps | 1 |
| Jitter, Cycle to cycle | t _{jcy-cyc} | | | 16 | 50 | ps | 1,2 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Measured from differential waveform

Electrical Characteristics–Input/Supply/Common Parameters–Normal Operating Conditions

TA = T_{AMB}; Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|-------------------------------|---------------------|---|-----------------------|---------------------|-----------------------|--------|-------|
| Supply Voltage | VDDxx | Supply voltage for core, analog and single-ended LVCMOS outputs | 1.425 | 1.5 | 1.575 | V | |
| Ambient Operating Temperature | T _{AMB} | Comercial range | 0 | 25 | 70 | °C | |
| | | Industrial range | -40 | 25 | 85 | °C | |
| Input High Voltage | V _{IH} | Single-ended inputs, except SMBus | 0.75 V _{DD} | | V _{DD} + 0.3 | V | |
| Input Mid Voltage | V _{IM} | Single-ended tri-level inputs ('_tri' suffix) | 0.4 V _{DD} | 0.5 V _{DD} | 0.6 V _{DD} | V | |
| Input Low Voltage | V _{IL} | Single-ended inputs, except SMBus | -0.3 | | 0.25 V _{DD} | V | |
| Output High Voltage | V _{IH} | Single-ended outputs, except SMBus. I _{OH} = -2mA | V _{DD} -0.45 | | | V | |
| Output Low Voltage | V _{IL} | Single-ended outputs, except SMBus. I _{OL} = -2mA | | | 0.45 | V | |
| Input Current | I _{IN} | Single-ended inputs, V _{IN} = GND, V _{IN} = VDD | -5 | | 5 | uA | |
| | I _{INP} | Single-ended inputs V _{IN} = 0 V; Inputs with internal pull-up resistors V _{IN} = VDD; Inputs with internal pull-down resistors | -200 | | 200 | uA | |
| Input Frequency | F _{in} | XTAL, or X1 input | 23 | 25 | 27 | MHz | |
| Pin Inductance | L _{pin} | | | | 7 | nH | 1 |
| Capacitance | C _{IN} | Logic Inputs, except DIF_IN | 1.5 | | 5 | pF | 1 |
| | C _{OUT} | Output pin capacitance | | | 6 | pF | 1 |
| Clk Stabilization | T _{STAB} | From V _{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock | | | 1.8 | ms | 1,2 |
| SS Modulation Frequency | f _{MOD} | Triangular Modulation | 30 | 31.6 | 33 | kHz | 1 |
| OE# Latency | t _{LATOE#} | DIF start after OE# assertion DIF stop after OE# deassertion | 1 | | 3 | clocks | 1,3 |
| Tdrive_PD# | t _{DRVPD} | DIF output enable after PD# de-assertion | | | 300 | us | 1,3 |
| Tfall | t _F | Fall time of single-ended control inputs | | | 5 | ns | 2 |
| Trise | t _R | Rise time of single-ended control inputs | | | 5 | ns | 2 |
| SMBus Input Low Voltage | V _{ILSMB} | | | | 0.6 | V | |
| SMBus Input High Voltage | V _{IHSMB} | V _{DD} SMB = 3.3V, see note 4 for V _{DD} SMB < 3.3V | 2.1 | | 3.3 | V | 4 |
| SMBus Output Low Voltage | V _{OLSMB} | @ I _{PULLUP} | | | 0.4 | V | |
| SMBus Sink Current | I _{PULLUP} | @ V _{OL} | 4 | | | mA | |
| Nominal Bus Voltage | V _{DD} SMB | | 1.425 | | 3.3 | V | |
| SCLK/SDATA Rise Time | t _{RSMB} | (Max V _{IL} - 0.15) to (Min V _{IH} + 0.15) | | | 1000 | ns | 1 |
| SCLK/SDATA Fall Time | t _{FSMB} | (Min V _{IH} + 0.15) to (Max V _{IL} - 0.15) | | | 300 | ns | 1 |
| SMBus Operating Frequency | f _{MAXSMB} | Maximum SMBus operating frequency | | | 400 | kHz | 1 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Control input must be monotonic from 20% to 80% of input swing.

³ Time from deassertion until outputs are >200 mV

⁴ For V_{DD}SMB < 3.3V, V_{IHSMB} >= 0.8xV_{DD}SMB

Electrical Characteristics–DIF Low-Power HCSL Outputs

TA = T_{AMB}; Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|------------------------|---|------|------|------|-------|-------|
| Slew rate | Trf | Scope averaging on fast setting | 1.2 | 2.4 | 3.6 | V/ns | 1,2,3 |
| | | Scope averaging on slow setting | 0.8 | 1.7 | 2.5 | V/ns | 1,2,3 |
| Slew rate matching | ΔTrf | Slew rate matching, Scope averaging on | | 9 | 20 | % | 1,2,4 |
| Voltage High | V _{HIGH} | Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on) | 600 | 750 | 850 | mV | 7 |
| Voltage Low | V _{LOW} | | -150 | 26 | 150 | | 7 |
| Max Voltage | V _{max} | Measurement on single ended signal using absolute value. (Scope averaging off) | | 763 | 1150 | mV | 7 |
| Min Voltage | V _{min} | | -300 | 22 | | | 7 |
| Vswing | Vswing | Scope averaging off | 300 | 1448 | | mV | 1,2,7 |
| Crossing Voltage (abs) | V _{cross_abs} | Scope averaging off | 250 | 390 | 550 | mV | 1,5,7 |
| Crossing Voltage (var) | ΔV _{cross} | Scope averaging off | | 11 | 140 | mV | 1,6,7 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Measured from differential waveform

³ Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

⁴ Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

⁵ V_{cross} is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

⁶ The total variation of all V_{cross} measurements in any particular system. Note that this is a subset of V_{cross_min/max} (V_{cross} absolute) allowed. The intent is to limit V_{cross} induced modulation by setting ΔV_{cross} to be smaller than V_{cross} absolute.

⁷ At default SMBus amplitude settings.

Electrical Characteristics–DIF Output Phase Jitter Parameter

TA = T_{AMB}; Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | IND. LIMIT | UNITS | Notes |
|----------------------------|--|--|-----|------|-----|------------|----------|---------|
| Phase Jitter, PLL Mode | t _{jphPCIeG1} | PCIe Gen 1 | | 27.7 | 40 | 86 | ps (p-p) | 1,2,3,5 |
| | t _{jphPCIeG2} | PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz | | 1.0 | 1.3 | 3 | ps (rms) | 1,2,3,5 |
| | | PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) | | 1.9 | 2.2 | 3.1 | ps (rms) | 1,2,3,5 |
| | t _{jphPCIeG3} | PCIe Gen 3 Common Clock Architecture (PLL BW of 2-4 or 2-5MHz, CDR = 10MHz) | | 0.4 | 0.6 | 1 | ps (rms) | 1,2,3,5 |
| t _{jphPCIeG3SRnS} | PCIe Gen 3 Separate Reference No Spread (SRnS) (PLL BW of 2-4 or 2-5MHz, CDR = 10MHz) | | 0.4 | 0.6 | 0.7 | ps (rms) | 1,2,3,5 | |

¹ Guaranteed by design and characterization, not 100% tested in production.

² See <http://www.pcisig.com> for complete specs

³ Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

⁴ Calculated from Intel-supplied Clock Jitter Tool

⁵ Applies to all differential outputs

Electrical Characteristics–REF

TA = T_{AMB}; Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | Notes |
|------------------------|-----------------------|---|------|------|------|----------|-------|
| Long Accuracy | ppm | see Tperiod min-max values | 0 | | | ppm | 1,2 |
| Clock period | T _{period} | 25 MHz output | | 40 | | ns | 2 |
| Rise/Fall Slew Rate | t _{rf1} | Byte 3 = 1F, 20% to 80% of VDDREF | 0.3 | 0.7 | 1.1 | V/ns | 1 |
| Rise/Fall Slew Rate | t _{rf1} | Byte 3 = 5F, 20% to 80% of VDDREF | 0.5 | 1.0 | 1.6 | V/ns | 1,3 |
| Rise/Fall Slew Rate | t _{rf1} | Byte 3 = 9F, 20% to 80% of VDDREF | 0.77 | 1.3 | 1.9 | V/ns | 1 |
| Rise/Fall Slew Rate | t _{rf1} | Byte 3 = DF, 20% to 80% of VDDREF | 0.84 | 1.4 | 2.0 | V/ns | 1 |
| Duty Cycle | d _{t1X} | V _T = VDD/2 V | 45 | 47.1 | 55 | % | 1,4 |
| Duty Cycle Distortion | d _{tcd} | V _T = VDD/2 V, when driven by XIN/CLKIN_25 pin | 0 | 2.0 | 4 | % | 1,5 |
| Jitter, cycle to cycle | t _{jcyc-cyc} | V _T = VDD/2 V | | 51.2 | 250 | ps | 1,4 |
| Noise floor | t _{dBc1k} | 1kHz offset | | -126 | -105 | dBc | 1,4 |
| Noise floor | t _{dBc10k} | 10kHz offset to Nyquist | | -139 | -110 | dBc | 1,4 |
| Jitter, phase | t _{jphREF} | 12kHz to 5MHz | | 1.11 | 3 | ps (rms) | 1,4 |

¹Guaranteed by design and characterization, not 100% tested in production.

²All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF is trimmed to 25.00 MHz

³Default SMBus Value

⁴When driven by a crystal.

⁵X2 should be floating.

Clock Periods–Differential Outputs with Spread Spectrum Disabled

| SSC OFF | Center Freq. MHz | Measurement Window | | | | | | | Units | Notes |
|---------|------------------|------------------------|-----------------------------|-----------------------------|----------------------|-----------------------------|-----------------------------|------------------------|-------|-------|
| | | 1 Clock | 1us | 0.1s | 0.1s | 0.1s | 1us | 1 Clock | | |
| | | -c2c jitter AbsPer Min | -SSC Short-Term Average Min | - ppm Long-Term Average Min | 0 ppm Period Nominal | + ppm Long-Term Average Max | +SSC Short-Term Average Max | +c2c jitter AbsPer Max | | |
| DIF | 100.00 | 9.94900 | | 9.99900 | 10.00000 | 10.00100 | | 10.05100 | ns | 1,2 |

Clock Periods–Differential Outputs with -0.5% Spread Spectrum Enabled

| SSC ON | Center Freq. MHz | Measurement Window | | | | | | | Units | Notes |
|--------|------------------|------------------------|-----------------------------|-----------------------------|----------------------|-----------------------------|-----------------------------|------------------------|-------|-------|
| | | 1 Clock | 1us | 0.1s | 0.1s | 0.1s | 1us | 1 Clock | | |
| | | -c2c jitter AbsPer Min | -SSC Short-Term Average Min | - ppm Long-Term Average Min | 0 ppm Period Nominal | + ppm Long-Term Average Max | +SSC Short-Term Average Max | +c2c jitter AbsPer Max | | |
| DIF | 99.75 | 9.94906 | 9.99906 | 10.02406 | 10.02506 | 10.02607 | | 10.05107 | ns | 1,2 |

¹Guaranteed by design and characterization, not 100% tested in production.

²All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF is trimmed to 25.00 MHz

General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte N through Byte N+X-1
- IDT clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

| Index Block Write Operation | | | | |
|-----------------------------|-----------|--------|----------------------|-----|
| Controller (Host) | | X Byte | IDT (Slave/Receiver) | |
| T | starT bit | | | |
| Slave Address | | | | |
| WR | WRite | | | |
| Beginning Byte = N | | | | ACK |
| | | | | ACK |
| Data Byte Count = X | | | | ACK |
| Beginning Byte N | | | | ACK |
| O | | | | O |
| O | | | | O |
| O | | | | O |
| Byte N + X - 1 | | | | ACK |
| P | stoP bit | | | |

Note: Read/Write address is determined by SADR latch.

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte N+X-1
- IDT clock sends **Byte 0 through Byte X (if X_(H) was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation | | | | |
|----------------------------|-----------------|--------|----------------------|------------------|
| Controller (Host) | | X Byte | IDT (Slave/Receiver) | |
| T | starT bit | | | |
| Slave Address | | | | |
| WR | WRite | | | |
| Beginning Byte = N | | | | ACK |
| | | | | ACK |
| RT | Repeat starT | | | |
| Slave Address | | | | |
| RD | ReaD | | | |
| | | | | ACK |
| ACK | | | | |
| ACK | | | | Beginning Byte N |
| O | | | | O |
| O | | | O | |
| O | | | O | |
| ACK | | | | |
| | | | Byte N + X - 1 | |
| N | Not acknowledge | | | |
| P | stoP bit | | | |

SMBus Table: Output Enable Register

| Byte 0 | Name | Control Function | Type | 0 | 1 | Default |
|--------|---------|------------------|------|---------|---------|---------|
| Bit 7 | | Reserved | | | | 1 |
| Bit 6 | | Reserved | | | | 1 |
| Bit 5 | | Reserved | | | | 1 |
| Bit 4 | | Reserved | | | | 1 |
| Bit 3 | | Reserved | | | | 1 |
| Bit 2 | DIF OE1 | Output Enable | RW | Low/Low | Enabled | 1 |
| Bit 1 | DIF OE0 | Output Enable | RW | Low/Low | Enabled | 1 |
| Bit 0 | | Reserved | | | | 1 |

SMBus Table: SS Readback and Vhigh Control Register

| Byte 1 | Name | Control Function | Type | 0 | 1 | Default |
|--------|--------------|-----------------------------|-----------------|--|--------------------------------------|---------|
| Bit 7 | SSENRB1 | SS Enable Readback Bit1 | R | 00' for SS_EN_tri = 0, '01' for SS_EN_tri = 'M', '11 for SS_EN_tri = '1' | | Latch |
| Bit 6 | SSENRB1 | SS Enable Readback Bit0 | R | | | Latch |
| Bit 5 | SSEN_SWCNTRL | Enable SW control of SS | RW | SS control locked | Values in B1[4:3] control SS amount. | 0 |
| Bit 4 | SSENSW1 | SS Enable Software Ctl Bit1 | RW ¹ | 00' = SS Off, '01' = -0.25% SS, | | 0 |
| Bit 3 | SSENSW0 | SS Enable Software Ctl Bit0 | RW ¹ | '10' = Reserved, '11' = -0.5% SS | | 0 |
| Bit 2 | | Reserved | | | | 1 |
| Bit 1 | AMPLITUDE 1 | Controls Output Amplitude | RW | 00 = 0.55V | 01 = 0.65V | 1 |
| Bit 0 | AMPLITUDE 0 | | RW | 10 = 0.7V | 11 = 0.8V | 0 |

1. B1[5] must be set to a 1 for these bits to have any effect on the part.

SMBus Table: DIF Slew Rate Control Register

| Byte 2 | Name | Control Function | Type | 0 | 1 | Default |
|--------|------------------|--------------------------|------|--------------|--------------|---------|
| Bit 7 | | Reserved | | | | 1 |
| Bit 6 | | Reserved | | | | 1 |
| Bit 5 | | Reserved | | | | 1 |
| Bit 4 | | Reserved | | | | 1 |
| Bit 3 | | Reserved | | | | 1 |
| Bit 2 | SLEWRATESEL DIF1 | Adjust Slew Rate of DIF1 | RW | Slow Setting | Fast Setting | 1 |
| Bit 1 | SLEWRATESEL DIF0 | Adjust Slew Rate of DIF0 | RW | Slow Setting | Fast Setting | 1 |
| Bit 0 | | Reserved | | | | 1 |

SMBus Table: REF Control Register

| Byte 3 | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------------------------|----------------------------|------|--------------------------------|------------------------|---------|
| Bit 7 | REF | Slew Rate Control | RW | 00 = Slowest | 01 = Slow | 0 |
| Bit 6 | | | RW | 10 = Fast | 11 = Faster | 1 |
| Bit 5 | REF Power Down Function | Wake-on-Lan Enable for REF | RW | REF does not run in Power Down | REF runs in Power Down | 0 |
| Bit 4 | REF OE | REF Output Enable | RW | Low | Enabled | 1 |
| Bit 3 | | Reserved | | | | 1 |
| Bit 2 | | Reserved | | | | 1 |
| Bit 1 | | Reserved | | | | 1 |
| Bit 0 | | Reserved | | | | 1 |

Byte 4 is reserved and reads back 'hFF'.

SMBus Table: Revision and Vendor ID Register

| Byte 5 | Name | Control Function | Type | 0 | 1 | Default |
|--------|------|------------------|------|--------------|---|---------|
| Bit 7 | RID3 | Revision ID | R | A rev = 0000 | | 0 |
| Bit 6 | RID2 | | R | | | 0 |
| Bit 5 | RID1 | | R | | | 0 |
| Bit 4 | RID0 | | R | | | 0 |
| Bit 3 | VID3 | VENDOR ID | R | 0001 = IDT | | 0 |
| Bit 2 | VID2 | | R | | | 0 |
| Bit 1 | VID1 | | R | | | 0 |
| Bit 0 | VID0 | | R | | | 1 |

SMBus Table: Device Type/Device ID

| Byte 6 | Name | Control Function | Type | 0 | 1 | Default |
|--------|--------------|------------------|------|---|---|---------|
| Bit 7 | Device Type1 | Device Type | R | 00 = FGx, 01 = DBx ZDB/FOB, 10 = DMx, 11 = DBx FOB | | 0 |
| Bit 6 | Device Type0 | | R | | | 0 |
| Bit 5 | Device ID5 | Device ID | R | 00010 binary or 02 hex | | 0 |
| Bit 4 | Device ID4 | | R | | | 0 |
| Bit 3 | Device ID3 | | R | | | 0 |
| Bit 2 | Device ID2 | | R | | | 0 |
| Bit 1 | Device ID1 | | R | | | 1 |
| Bit 0 | Device ID0 | | R | | | 0 |

SMBus Table: Byte Count Register

| Byte 7 | Name | Control Function | Type | 0 | 1 | Default |
|--------|------|------------------------|------|---|---|---------|
| Bit 7 | | Reserved | | | | 0 |
| Bit 6 | | Reserved | | | | 0 |
| Bit 5 | | Reserved | | | | 0 |
| Bit 4 | BC4 | Byte Count Programming | RW | Writing to this register will configure how many bytes will be read back, default is = 8 bytes. | | 0 |
| Bit 3 | BC3 | | RW | | | 1 |
| Bit 2 | BC2 | | RW | | | 0 |
| Bit 1 | BC1 | | RW | | | 0 |
| Bit 0 | BC0 | | RW | | | 0 |

Recommended Crystal Characteristics (3225 package)

| PARAMETER | VALUE | UNITS | NOTES |
|--|-------------|---------|-------|
| Frequency | 25 | MHz | 1 |
| Resonance Mode | Fundamental | - | 1 |
| Frequency Tolerance @ 25°C | ±20 | PPM Max | 1 |
| Frequency Stability, ref @ 25°C Over Operating Temperature Range | ±20 | PPM Max | 1 |
| Temperature Range (commercial) | 0~70 | °C | 1 |
| Temperature Range (industrial) | -40~85 | °C | 2 |
| Equivalent Series Resistance (ESR) | 50 | Ω Max | 1 |
| Shunt Capacitance (C ₀) | 7 | pF Max | 1 |
| Load Capacitance (C _L) | 8 | pF Max | 1 |
| Drive Level | 0.3 | mW Max | 1 |
| Aging per year | ±5 | PPM Max | 1 |

Notes:

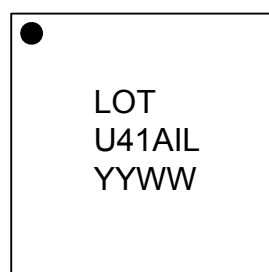
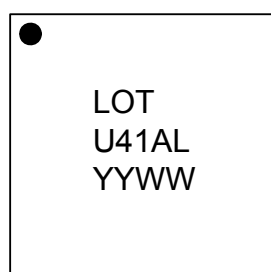
1. FOX 603-25-150.
2. For I-temp, FOX 603-25-261.

Thermal Characteristics

| PARAMETER | SYMBOL | CONDITIONS | PKG | TYP VALUE | UNITS | NOTES |
|--------------------|----------------|---------------------------------|-------|-----------|-------|-------|
| Thermal Resistance | θ_{JC} | Junction to Case | NLG24 | 62 | °C/W | 1 |
| | θ_{Jb} | Junction to Base | | 5.4 | °C/W | 1 |
| | θ_{JA0} | Junction to Air, still air | | 50 | °C/W | 1 |
| | θ_{JA1} | Junction to Air, 1 m/s air flow | | 43 | °C/W | 1 |
| | θ_{JA3} | Junction to Air, 3 m/s air flow | | 39 | °C/W | 1 |
| | θ_{JA5} | Junction to Air, 5 m/s air flow | | 38 | °C/W | 1 |

¹ePad soldered to board

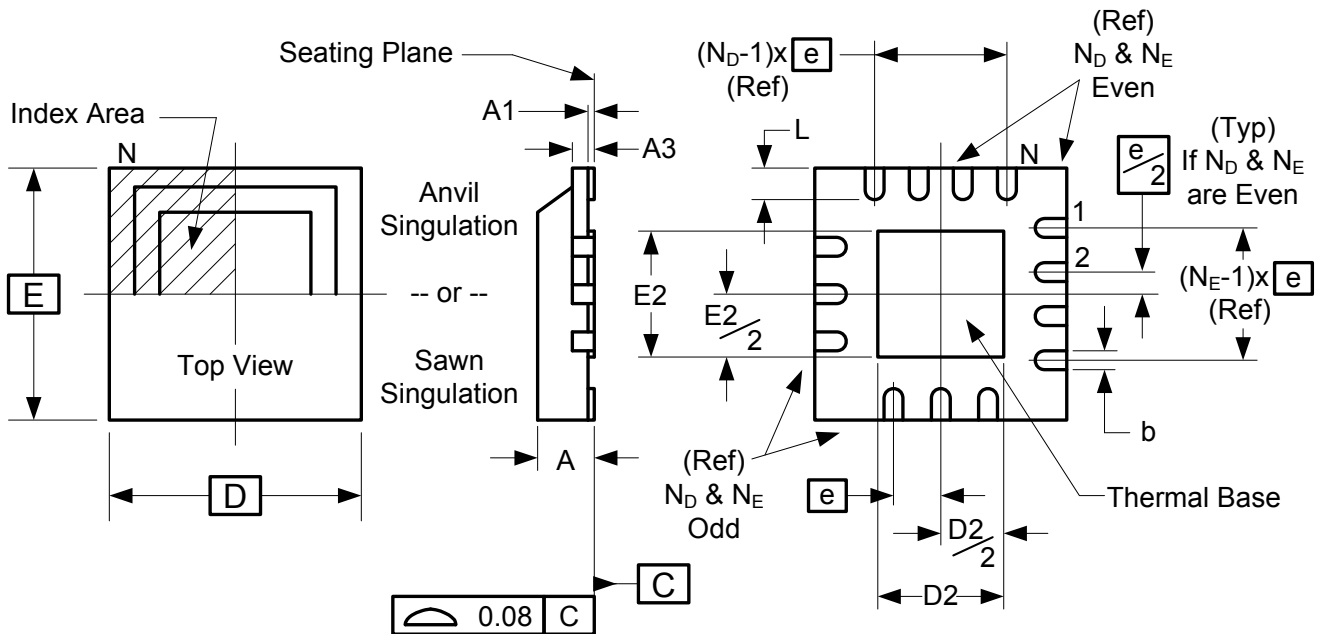
Marking Diagrams



Notes:

1. "LOT" is the lot number.
2. "YYWW" is the last two digits of the year and week that the part was assembled.
3. "L" denotes RoHS compliant package.
4. "I" denotes industrial temperature grade.

Package Outline and Package Dimensions (NLG24)



| Symbol | Millimeters | |
|----------------|----------------|------|
| | Min | Max |
| A | 0.80 | 1.00 |
| A1 | 0 | 0.05 |
| A3 | 0.25 Reference | |
| b | 0.18 | 0.30 |
| e | 0.50 BASIC | |
| D x E BASIC | 4.00 x 4.00 | |
| D2 MIN./MAX. | 2.3 | 2.60 |
| E2 MIN./MAX. | 2.3 | 2.60 |
| L MIN./MAX. | 0.30 | 0.50 |
| N | 24 | |
| N _D | 6 | |

Ordering Information

| Part / Order Number | Shipping Packaging | Package | Temperature |
|---------------------|--------------------|---------------|---------------|
| 9FGU0241AKLF | Tubes | 24-pin VFQFPN | 0 to +70° C |
| 9FGU0241AKLFT | Tape and Reel | 24-pin VFQFPN | 0 to +70° C |
| 9FGU0241AKILF | Tubes | 24-pin VFQFPN | -40 to +85° C |
| 9FGU0241AKILFT | Tape and Reel | 24-pin VFQFPN | -40 to +85° C |

“LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

“A” is the device revision designator (will not correlate with the datasheet revision).

Revision History

| Rev. | Issue Date | Initiator | Description | Page # |
|------|------------|-----------|---|---------|
| A | 9/24/2014 | RDW | <ol style="list-style-type: none"> 1. Updated electrical tables with latest versions for release 2. Updated SMBus nomenclature for consistency with the family 3. Removed references to Suspend Mode. This is replaced by Power Down with Wake-on-LAN Modes in the current consumption table. 4. Updated GenDes tab for front page consistency 5. All Electrical tables updated with characterization data. 6. Move to final. | Various |
| B | 10/18/2016 | RDW | Removed IDT crystal part number | |

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.