MOBILE ACCESS™—CLOCK SYNTHESIZER & TEMPERATURE SENSOR FOR PORTABLE DEVICES

9TCS1082

Description

The 9TCS1082 is a highly programmable IC that integrates clock synthesizers and a temperature sensor for hardware thermal protection.

The device has an ultra-low-power 32.768 kHz frequency generator to support Real Time Clocks (RTC). This device can generate the 32.768 kHz frequency up to four years of life powered by a CR2032 coin cell battery. The 9TCS1082 can output computer system clock frequencies of 25, 27, and 48 MHz which will reduce the component count on the circuit board.

The 9TCS1082 includes temperature monitor function that measures through external diode. The temperature sensor is optimized to be accurate within ±1°C between the temperature range of 60°C to 100°C. This device is highly programmable through the use of I2C to set high and low limits for all the temperature channels as well as setting critical limits. The hardware limits drive dedicated Alert and Therm pins for system shutdown.

The 9TCS1082 is available in a 32-pin QFN package and is available for commercial temperature range

Applications

- Notebook Computers
- Netbook Computers
- Smartbook Computers
- Consumer Portable Devices
- Embedded Systems
- Networking Equipment (i.e. Routers, Switches)
- Network Area Storage

Features

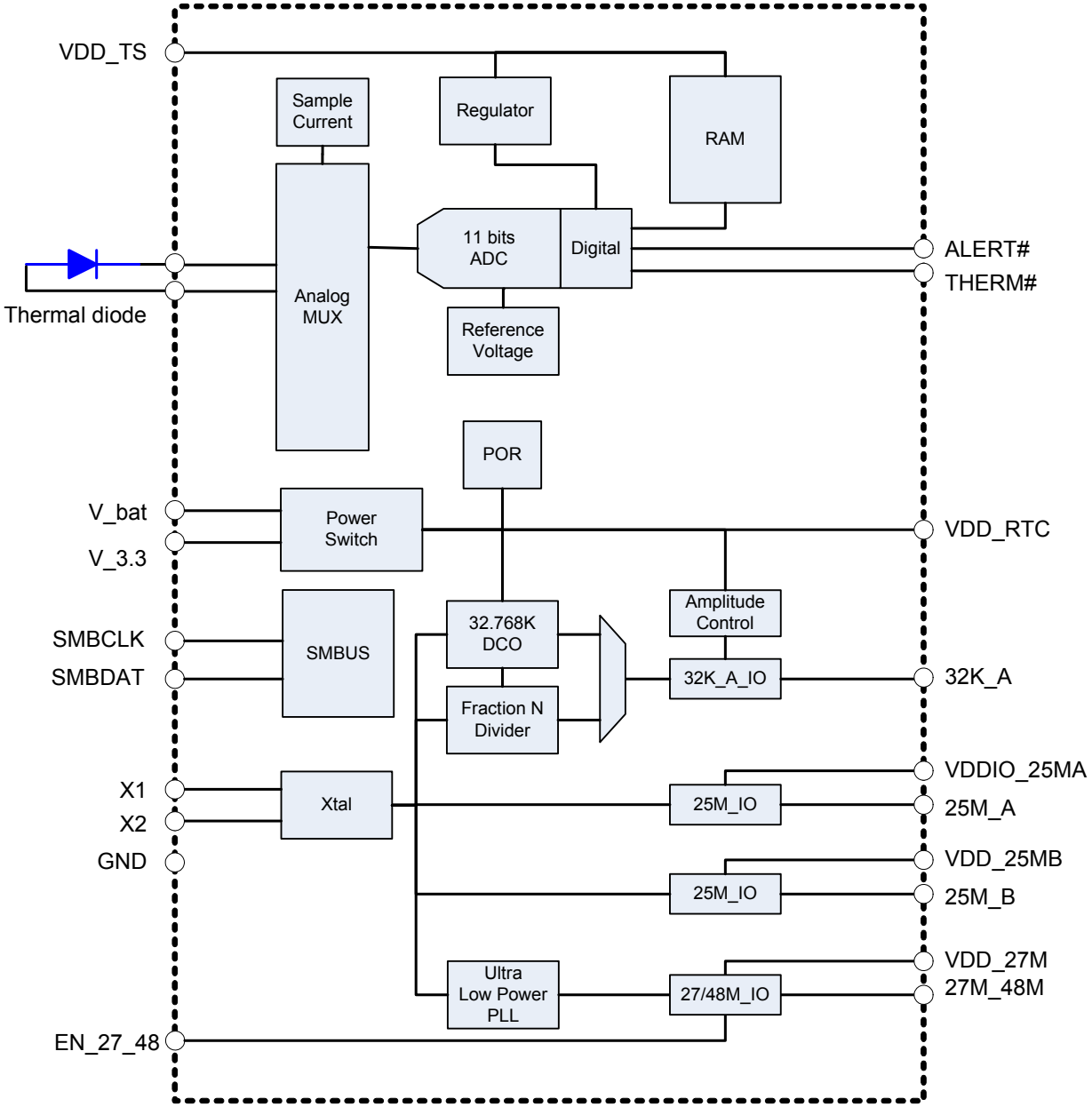
Thermal Sensor

- One channel thermal sensor
- Both H/W & S/W programmable over/under temperature alarms
- No Calibration required in application
- Diode failure detection
- Support SMBUS Alert
- Accuracy: ±1°C (+60°C to +100°C, remote); ±2°C (0°C to + 100°C, remote and local)
- Offset register for system calibration
- Series resistor cancellation feature

System Clock PLL Synthesizers

- Scalable Low Voltage VDD I/O (1.5V to 1.05V) to reduce power consumption (apply to 25MHz output)
- Integrated series termination resistors
- Selectable – Single-ended 27MHz/48MHz clock output @ VDD3.3V
- 2 – single ended 25MHz clock outputs (buffer out)
- 32.768 kHz outputs with < 1.8µA power consumption for system RTC circuit

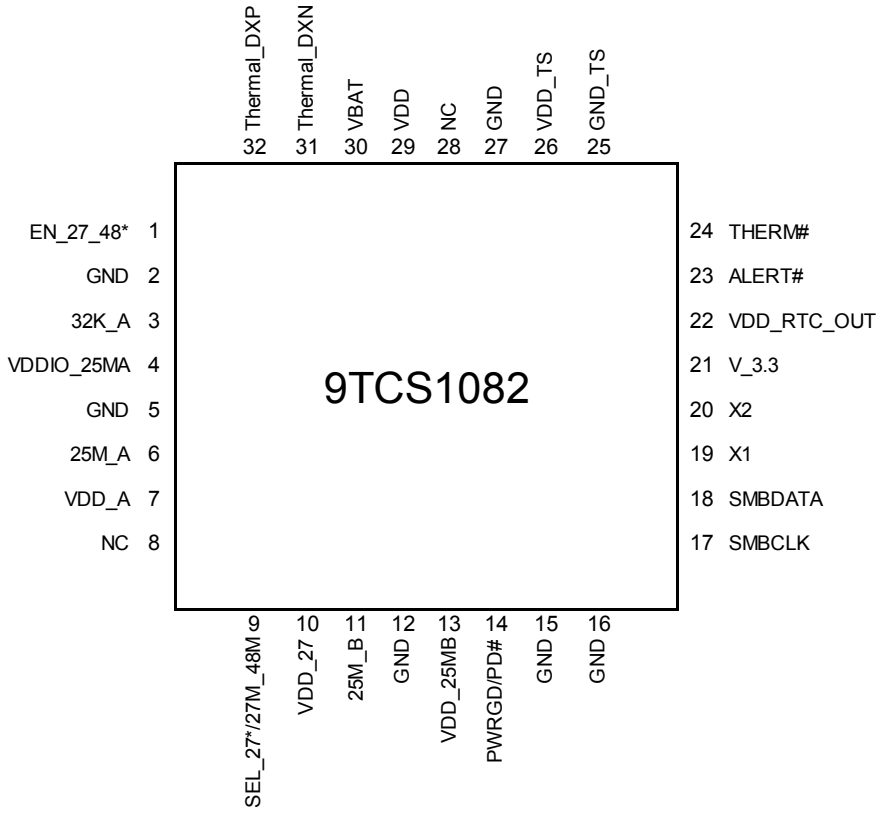
Block Diagram



Preferred drive strengths for single-ended outputs.
Transmission lines to load do not share series resistors.
Desktop (Zo=50Ω) and mobile (Zo=55Ω) have the same drive strength.

	Number of Loads to Drive	Match Point for N & P Voltage / Current (mA)	Number of Loads Actually Driven.		
			1 Load Rs =	2 Loads Rs=	3 Loads Rs =
D.C.Drive Strength	1	0.56 / 33 (17Ω)	33Ω [39Ω]	-	-
	2	0.92 / 66 (14Ω)	39Ω [43Ω]	22Ω [27Ω]	-
	3	1.15 / 99 (11.6Ω)	43Ω [43Ω]	27Ω [33Ω]	15Ω [22Ω]

Pin Assignment



Power Group

Pin Number		Description
VDD	GND	
4	33	VDDIO_25MA IO power
7	5	VDD_A power
10	12	VDDIO_27
13	33	VDDIO_25B IO Power
21	33	V3.3
22	27	VDD_RTC_Out
26	25	VDD_TS power
30	27	VBAT power

* pin33: thermal pad

Pin Descriptions

PIN #	PIN NAME	TYPE	DESCRIPTION
1	EN_27_48*	PWR	Real time control pin for 27_48M output. 0 = disable 1 = Enable (default)
2	GND	OUT	Ground pin
3	32K_A	OUT	RTC clock 32.768KHz output, typical 1V peak to peak.
4	VDDIO_25MA	PWR	Power for 25MHz_A output, typical 1.05V to 1.5V.
5	GND	PWR	Ground pin
6	25M_A	OUT	25MHz_A Output, typical 1.05V to 1.5V pending on VDDIO25_MA voltage.
7	VDD_A	PWR	Power pin
8	NC	NC	No Connection
9	SEL_27*/27M_48M	I/O	27MHz enable latched Input / Programmable free-running 27/48M clock output. SEL_27 selects the functionality of 27_48M output as the following: 1 = 27M output (default) 0 = 48M output
10	VDD_27M	PWR	Power for 27/48 MHz output, typical 3.3V.
11	25M_B	OUT	25MHz_B output, typical 3.3V peak to peak.
12	GND	PWR	Ground pin
13	VDD_25MB	PWR	Power for LDO and main circuit , connect to system standby power for WOL supports
14	PWRGD/PD#	IN	This 3.3V LVTTL input notifies device to sample latched inputs and start up on first high assertion, or exit Power Down Mode on subsequent assertions. Low enters Power Down Mode or called Wake On LAN mode.
15	GND	PWR	Ground pin
16	GND	PWR	Ground pin
17	SMBCLK	IN	SMBUS clock. 3.3V tolerant.
18	SMBDAT	I/O	SMBUS data. 3.3V tolerant.
19	X1	IN	Crystal input. Connect to 25MHz crystal.
20	X2	OUT	Crystal output. Connect to 25MHz crystal.
21	V_3.3	PWR	Power for 32K PLL core, connect to system 3.3V standby power rail.
22	VDD_RTC_OUT	OUT	Power for chipset RTC circuit
23	ALERT#	OUT	Open drain interrupt output for SMBUS
24	FAULT#	OUT	Open drain interrupt output for external hardware connection
25	GND_TS	PWR	Ground pin for thermal sensor function
26	VDD_TS	PWR	Power for thermal sensor function
27	GND	PWR	Ground pin
28	NC	NC	No Connection
29	VDD	PWR	Connect to 3.3V typical.
30	VBAT	PWR	Power for 32kHz_A output. Connect to coin cell battery
31	Thermal_DXN	IN	external thermal diode N
32	Thermal_DXP	IN	external thermal diode P
33	Thermal Pad	PWR	Connect to GND.

Frequency and Output Selection Tables

Clock Output Selection Table

Pin number	Setting	Output	Remark
9	L	48MHz	
	H	27MHz	default, internal pull high

Output Selection Table A

Power Supply		VDDIO_Control			Outputs		
V_Bat	V_3.3	VDDIO_25A	VDD_25B	32K_A	25M_A	25M_B	VDD_RTC
2.3~3.0	0	0	0	ON	OFF	OFF	Vbat
2.3~3.0	3.3[1]	0	0	ON	OFF	OFF	V3.3
2.3~3.0	3.3[1]	0	0	ON	OFF	OFF	V3.3
2.3~3.0	3.3[1]	1.05~1.5[2]	0	ON	ON	OFF	V3.3
2.3~3.0	3.3[1]	1.05~1.5[2]	3.3	ON	ON	ON	V3.3

Note 1: When V3.3 is applied, XTAL will always be ON. 32K source will switch to an analog PLL.
Note 2: If amplitude greater than 1.5V is required on 25MHz_A output, please contact IDT support.

Output Selection Table B

Power Supply			Outputs		
V_3.3	VDD_27M[1]	VDD_TS[1]	27_48M	Fan Control	Thermal Sensor
3.3	0	0	OFF	ON	OFF
3.3	0	0	OFF	ON	OFF
3.3	3.3	0	ON	ON	OFF
3.3	3.3	3.3	ON	ON	ON

Note 1: When either VDD_27M or VDD_TS is ON, V_3.3 should be ON.

Thermal Conversion Time

Conversion Rate Select	OFF_Time(ms)	Conversion rate @ 1channel	Power (uA)
0	50ms	10/s	250
1	50ms	10/s	250
10	100ms	6/s	160
11	200ms	4/s	100
100	400ms	2/s	60
101	800ms	1/s	30
110	1.6s	1/2s	15
111	3.2s	1/4s	7.5
1000	6.4s	1/8s	3.75
1001	12.8s	1/16s	1.9
1010	25.6s	1/32s	1
1011	Reserve	Reserve	Reserve
1100	Reserve	Reserve	Reserve
1101	Reserve	Reserve	Reserve
1110	Reserve	Reserve	Reserve
1111	Reserve	Reserve	Reserve

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9TCS1082. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Maximum Supply Voltage	VDDxxx	Core/Logic Supply		3.6	V	1,2
Maximum Supply Voltage	VDDIOxxx	Core/Logic Supply		3.6	V	1,2
Maximum Input Voltage	V_{IH}	3.3V LVCMOS Inputs		3.6	V	1,2,3
Minimum Input Voltage	V_{IL}	Any Input	GND - 0.5		V	1,2
Storage Temperature	Ts	-	-65	150	°C	1,2
Case Temperature	Tcase	-		115	°C	1,2

[1] Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.
[2] Operation under these conditions is neither implied, nor guaranteed.
[3] Maximum input voltage is not to exceed maximum VDD

Electrical Characteristics–SMBus Interface

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
SMBus Voltage	V_{DD}		2.7	3.6	V	1
Low-level Output Voltage	V_{OLSMB}	@ I_{PULLUP}		0.4	V	1
Current sinking at V_{OLSMB} = 0.4 V	I_{PULLUP}	SMB Data Pin	4		mA	1
SCLK/SDATA Clock/Data Rise Time	T_{RI2C}	(Max VIL - 0.15) to (Min VIH + 0.15)		1000	ns	1
SCLK/SDATA Clock/Data Fall Time	T_{FI2C}	(Min VIH + 0.15) to (Max VIL - 0.15)		300	ns	1
Maximum SMBus Operating Frequency	F_{SMBUS}	Block Mode		400	kHz	1

[1] Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

AC Electrical Characteristics–Input/Common Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Clk Stabilization	T_{STAB}	From VDD Power-Up or de-assertion of PD# to 1st clock		1.8	ms	1
Tdrive_PD#	T_{DRPD}	Differential output enable after PD# de-assertion		300	us	1

[1] Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics–Input/Supply/Common Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Ambient Operating Temp	Tambient	-	0	70	°C	
Supply Voltage	V_3.3	Supply Voltage	3.135	3.465	V	
Supply Voltage	VDD_xx	Other Supply Voltages	3.135	3.465	V	
Supply Voltage	VDDIO_25MA	Supply Voltage	0.9975	1.575	V	
Supply Voltage	V_bat	Supply Voltage	2.3	3.465	V	
Input High Voltage	V_{IHSE}	Single-ended inputs	2	V_{DD} + 0.3	V	1,4
Input Low Voltage	V_{ILSE}	Single-ended inputs	V_{SS} - 0.3	0.8	V	1,4
Low Threshold Input-High Voltage	V_{IH_FS}	3.3 V +/-5%	0.7	V_{DD} + 0.3	V	1
Low Threshold Input-Low Voltage	V_{IL_FS}	3.3 V +/-5%	V_{SS} - 0.3	0.35	V	1
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$, V_{IN} = GND	-5	5	uA	1,3
Input Leakage Current	I_{INRES}	Inputs with pull or pull down resistors $V_{IN} = V_{DD}$, V_{IN} = GND	-200	200	uA	1
Output High Voltage	V_{OHSE}	Single-ended outputs, I_{OH} = -1mA	2.4		V	1,2
Output Low Voltage	V_{OLSE}	Single-ended outputs, I_{OL} = 1 mA		0.4	V	1,2
3.3V Operating Supply Current	$I_{DD3.3OP}$	Full active mode, C_L = Full load, 3.3V Rail		50	mA	1
	$I_{DD3.3PD\#}$	Complete Power-Down, 3.3V Rail		10	mA	1
	$I_{DD3.3WOL}$	WOL Mode with 25MA running, 3.3V Rail		25	mA	1
	$I_{DD3.3RTC}$	RTC Mode with 32KA running, 3.3V Rail		0.1	uA	1
VDDIO Operating Supply Current	I_{DDIO_OP}	Full active mode, C_L = Full load, VDDIO Rails		5	mA	1
	$I_{DDIO\_PD\#}$	Complete Power-Down, VDDIO Rails		1	mA	1
	I_{DDDIO_WOL}	WOL Mode with 25MA running, VDDIO Rails		10	mA	1
	I_{DDIO_RTC}	RTC Mode with only 32KA running, VDDIO Rails		0.5	uA	1
V_bat Operating Supply Current	IDD_V_bat	RTC Mode with 32KA running, V_bat Rail		1.8	uA	1
Input Frequency	F_i	V_{DD} = 3.3 V	25MHz Typical		MHz	1
Pin Inductance	L_{pin}			7	nH	1
Input Capacitance	C_{IN}	Logic Inputs	1.5	5	pF	1
	C_{OUT}	Output pin capacitance		6	pF	1
	C_{INX}	X1 & X2 pins		6	pF	1

*TA = 0 - 70°C; Supply Voltage V_3.3 = VDD_TS = 3.3 V +/-5%, VDD_27M = VDD_25MB = 3.3V +/- 5%, VDD_25MA = 1.05V +/- 5%, CL = 5pF with Rs = 0 Ω (unless otherwise specified)

[1] Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

[2]Signal is required to be monotonic in this region.

[3] Input leakage current does not include inputs with pull-up or pull-down resistors

[4] 3.3V referenced inputs are: SCLK, SDATA, SEL_27, PWRGD.

AC Electrical Characteristics–Power Management

Output Clock Power Consumption Table

Power Supply		Power Consumption @ 2' transmission line			
V_bat / V_3.3	Outputs	I_V_bat	I_V_3.3	I_VDD_32KB	I_VDD_25M
2.3~3.3	32K_A	1.8uA	0	0	0
2.3~3.3	32K_A	0	2mA	0	0
2.3~3.3	32K_A+B	0	2mA	1uA	0
2.3~3.3	32K, 25M_A	0	2mA	1uA	1mA
2.3~3.3	32K_A+B,25MA+B	0	2mA	1uA	2mA

Note: When V_3.3 is applied, XTAL will always be ON. 32K source will switch to an analog PLL. Fan control will be ON

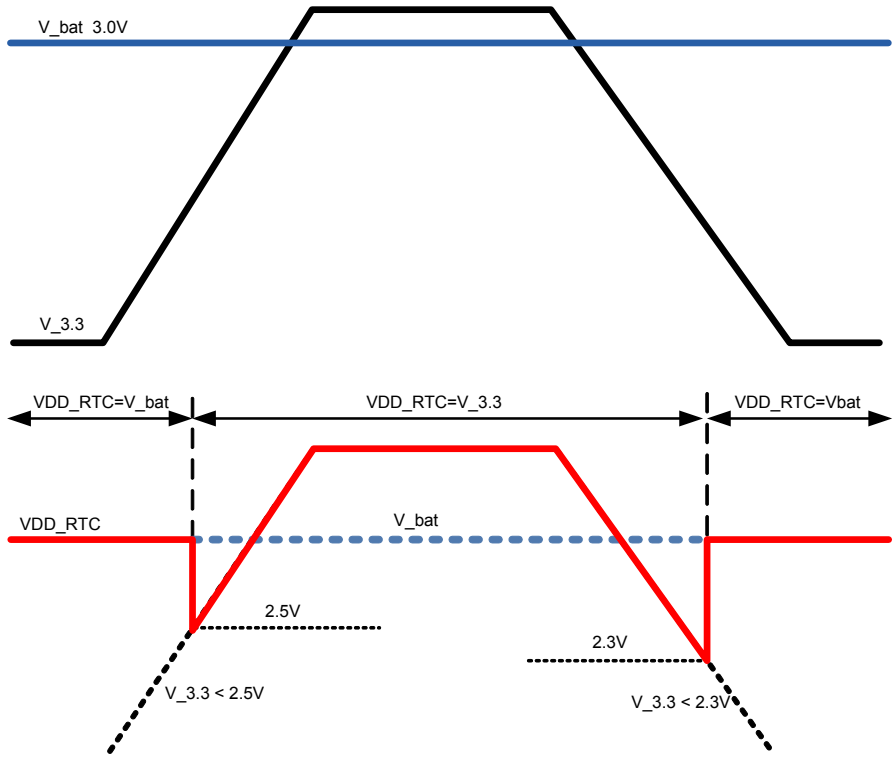
Power Supply		Power consumption @ 2' transmission line		
V_3.3	VDD_24/27/TS	I_V3.3	I_VDD_27M	I_VDD_TS
3.3	0	2mA	0	0
3.3	27Mhz	2mA	1mA	0
3.3	27Mhz+Thermal+Fan	2mA	1mA	0.8mA

Note: When either VDD_24M/VDD_27M/VDD_TS is ON, V3.3 should be ON

Power Switch (VBAT/V33 -> VDD_RTC)

Integrated power switch detects the VDD_RTC SW to coin cell battery (VBAT) or main power supply (V33).

When there is no V33 (V33=0), the SW will connect the VDD_RTC to VBAT; when V33 goes higher than 2.5V, the VDD_RTC will be switched to V33 with no delay. After V33 goes lower than 2.3V, the VDD_RTC will be switched to VBAT, no delay.



When VDD_RTC = VBAT, the power SW circuit consumes < 100nA.

When VDD_RTC = V33, the power consumption on VBAT needs to be “0”.

Electrical Characteristics–48MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Output Impedance	R_{DSP}	$V_O = V_{DD}*(0.5)$	12	55	Ω	1
Clock period	T_{period}	48.00MHz output nominal	20.8313	20.8354	ns	1,2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4		V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA		0.4	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-33		mA	1
		V_{OH}@MAX = 3.135 V		-33	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	30		mA	1
		V_{OL} @ MAX = 0.4 V		38	mA	1
Rising Edge Slew Rate	t_{SLR}	Measured from 0.8 to 2.0 V	0.5	2.5	V/ns	1
Falling Edge Slew Rate	t_{SLR}	Measured from 2.0 to 0.8 V	0.5	2.5	V/ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45	55	%	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V		350	ps	1

*TA = 0 - 70°C; Supply Voltage V_3.3 = VDD_TS = 3.3 V +/-5%, VDD_27M = VDD_25MB = 3.3V +/- 5%, VDD_25MA = 1.05V +/- 5%, CL = 5pF with Rs = 0 Ω (unless otherwise specified)

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 25.000000MHz

Electrical Characteristics–25MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-100	100	ppm	1,2
CLK Low time	T_{LOW}		7.816563	10.95198	V	1
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4		V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA		0.4	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-29		mA	1
		V_{OH}@MAX = 3.135 V		-23	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	29		mA	1
		V_{OL} @ MAX = 0.4 V		27	mA	1
Rising Edge Slew Rate	t_{SLR}	Measured from 0.8 to 2.0 V	0.5	4	V/ns	1
Falling Edge Slew Rate	t_{SLR}	Measured from 2.0 to 0.8 V	0.5	4	V/ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	40	60	%	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V		500	ps	1

*TA = 0 - 70°C; Supply Voltage V_3.3 = VDD_TS = 3.3 V +/-5%, VDD_27M = VDD_25MB = 3.3V +/- 5%, VDD_25MA = 1.05V +/- 5%, CL = 5pF with Rs =0 Ω (unless otherwise specified)

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 25.000000MHz

Electrical Characteristics–27MHz

Long Accuracy	ppm	see Tperiod min-max values	-50	50	ppm	1,2
Clock period	T_{period}	27.000MHz output nominal	37.0365	37.0376	ns	1,2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4		V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA		0.4	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-29		mA	1
		V_{OH}@MAX = 3.135 V		-23	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	29		mA	1
		V_{OL} @ MAX = 0.4 V		27	mA	1
Rising Edge Slew Rate	t_{SLR}	Measured from 0.8 to 2.0 V	1	4	V/ns	1
Falling Edge Slew Rate	t_{FLR}	Measured from 2.0 to 0.8 V	1	4	V/ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45	55	%	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	Cycle to Cycle, V_T = 1.5 V		200	ps	1

*TA = 0 - 70°C; Supply Voltage V_3.3 = VDD_TS = 3.3 V +/-5%, VDD_27M = VDD_25MB = 3.3V +/- 5%, VDD_25MA = 1.05V +/- 5%, CL = 5pF with Rs = 0 Ω (unless otherwise specified)

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 25.000000MHz

Electrical Characteristics–32kHz

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	32.768 Typical		kHz	1,2
Output High Voltage	V_{OH}	32K_A Output	0.8	1.2	V	1
Output Low Voltage	V_{OL}	32K_A Output		0.3	V	1
Initial Frequency Error	$32K_{INI}$	0C to 70C		+/-10	ppm	1
				0.86	sec/day	1
RTC Frequency Error	$32K_{RTC\_7D}$	7-day measurement		8	sec	1
Rising Edge Slew Rate	t_{SLR}	Measured from 20% to 80%	0.03 typ		V/ns	1
Falling Edge Slew Rate	t_{FLR}	Measured from 80% to 20%	0.03 typ		V/ns	1
Duty Cycle	d_{t1}	VT = V_bat/2	40	60	%	1

*TA = 0 - 70°C; Supply Voltage V_3.3 = VDD_TS = 3.3 V +/-5%, VDD_27M = VDD_25MB = 3.3V +/- 5%, VDD_25MA = 1.05V +/- 5%, CL = 2pF with Rs = 0 Ω (unless otherwise specified)

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 25.000000MHz

Recommended 25MHz Crystal Specifications

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Frequency Accuracy	Faccur	@25C		+/-10	ppm	1
Frequency Error over temperature	Ferrt	-10C ~ 70C		+/-10	ppm	1
Frequency Aging	Faging	1 year		+/-1	ppm	1
Driver Level	DL			100	uW	1
Crystal Load Capacitance	CL	Parallel Resonance	8pF Typical		pF	1

*TA = 0 - 70°C; Supply Voltage V_3.3 = VDD_TS = 3.3 V +/-5%, VDD_27M = VDD_25MB = 3.3V +/- 5%, VDD_25MA = 1.05V +/- 5%,

[1]Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics – Thermal Sensor Controller

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Remote Sensor Accuracy	Raccu	0C<TA<60C		2	C	1
		60C<TA<100C		1	C	1
Resolution	Rs			1	C	1
Conversion Rate	CR		16	1/64	Sec	1

*TA = 0 - 70°C; Supply Voltage V_3.3 = VDD_TS = 3.3 V +/-5%, VDD_27M = VDD_25MB = 3.3V +/- 5%, VDD_25MA = 1.05V +/- 5%, (unless otherwise specified)

[1]Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics – Fan Controller

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
PWM frequency	PWM		25	27	kHz	1
Output Impedance		I_{OUT} =100uA, V_{OUT}=0.8V, Frequency=100kHz				
Current Overshoot Reduction Speed		Time Interval per Current Step				
PWM Duty Cycle	DUTY			100	%	1
Tachometer Range	TACH		1	4	POLE	1

*TA = 0 - 70°C; Supply Voltage V_3.3 = VDD_TS = 3.3 V +/-5%, VDD_27M = VDD_25MB = 3.3V +/- 5%, VDD_25MA = 1.05V +/- 5%, (unless otherwise specified)

[1]Guaranteed by design and characterization, not 100% tested in production.

General SMBus Serial Interface Information for 9TCS1082

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- IDT clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a Stop bit

Index Block Write Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Read Address	Write Address
$D3_{H)}$	$D2_{(H)}$

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte **N+X-1**
- IDT clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

Byte0	Name	Control Function	Type	0	1	PWD
Bit7	ALERT_TH1	CH1 Diode ALERT High Temperature Limit	RW	-	SIGN	0
Bit6					64C	1
Bit5					32C	1
Bit4					16C	1
Bit3					8C	1
Bit2					4C	1
Bit1					2C	1
Bit0					1C	1

Note: Register readback uses 2's Complement

Byte 1,2 Reserved Register

Byte3	Name	Control Function	Type	0	1	PWD
Bit7	ALERT_TL1	CH1 Diode ALERT Low Temperature Limit	RW	-	SIGN	1
Bit6					64C	0
Bit5					32C	0
Bit4					16C	0
Bit3					8C	0
Bit2					4C	0
Bit1					2C	0
Bit0					1C	1

Note: Register readback uses 2's Complement

Byte 4,5 Reserved Register

Byte6	Name	Control Function	Type	0	1	PWD
Bit7	Thermal_EN	Enable Temp-Sensor	RW	Disable	Enable	0
Bit6	Reserved	Reserved	RW	-	-	0
Bit5	Reserved	Reserved	RW	-	-	1
Bit4	Reserved	Reserved	RW	-	-	0
Bit3	Consecutive ALERT	Consecutive ALERT Report	RW	00 = 1	01 = 2	0
Bit2			RW	10 = 3	11 = 4	0
Bit1	Average_Fact	Average the converted temperature	RW	00 = 1	01 = 4	0
Bit0			RW	10 = 8	11 = 16	0

Byte7	Name	Control Function	Type	0	1	PWD
Bit7	THERMAL1	CH1 Diode THERMALTemperature Limit	RW	-	Reserved	0
Bit6					64C	1
Bit5					32C	1
Bit4					16C	1
Bit3					8C	1
Bit2					4C	1
Bit1					2C	1
Bit0					1C	1

Byte 8 ~ 9 Reserved Registers

Byte10	Name	Control Function	Type	0	1	PWD
Bit7	D_A1	CH1 Gain (Slope) Coefficient	RW	-	1.28C	1
Bit6			RW		0.64C	0
Bit5			RW		0.32C	0
Bit4			RW		0.16C	0
Bit3	D_B1	CH1 Offset Coefficient	RW		4C	1
Bit2			RW		2C	0
Bit1			RW		1C	0
Bit0			RW		0.5C	0

Byte 11 Reserved Register

Byte12	Name	Control Function	Type	0	1	PWD
Bit7	Reserved	Reserved	RW	-	-	0
Bit6	Reserved	-	RW	-	-	0
Bit5	MASK1	MASK Channel1 ALERT	RW	Non-Mask	Mask	0
Bit4	THERMAL_HYS	THERMAL Limit Hysteresis	RW	-	16C	0
Bit3			RW		8C	0
Bit2			RW		4C	1
Bit1			RW		2C	0
Bit0			RW		1C	0

Byte13	Name	Control Function	Type	0	1	PWD
Bit7	Reserved	Reserved	R	-	-	0
Bit6	Reserved	Reserved	R	-	-	0
Bit5	Reserved	-	R	-	-	0
Bit4	Reserved	-	R	-	-	0
Bit3	Thermal High	ALERT High Alarm	R	Non-Flag	Flag	0
Bit2	Thermal Low	ALERT Low Alarm	R	Non-Flag	Flag	0
Bit1	Thernal diode Fault	(Open/Short)	R	Non-Flag	Flag	0
Bit0	Reserved	-	R	-	-	0

Byte14	Name	Control Function	Type	0	1	PWD
Bit7	BUSY	ADC is converting	R	Non-Flag	Flag	0
Bit6	HIGH	ALERT High	R	Non-Flag	Flag	0
Bit5	LOW	ALERT Low	R	Non-Flag	Flag	0
Bit4	FAULT	Open/Short	R	Non-Flag	Flag	0
Bit3	Reserved	Reserved	R	-	-	0
Bit2	THERMAL Alarm	THERMAL Alarm	R	Non-Flag	Flag	0
Bit1	Reserved	Reserved	R	-	-	0
Bit0	Reserved	Reserved	R	-	-	0

Byte15	Name	Control Function	Type	0	1	PWD
Bit7	Fault_Clear	Clear all the Alarm Flag	RW	No Clear	Clear	0
Bit6	One-Shot	One-Shot Temperature Conversion	RW	Disable Oneshot	Do OneShot	0
Bit5	DYN_AVE_EN	Enable Dynamic average	RW	Disable Dynamic Average	Enable Dynamic Average	0
Bit4	Conv. Rate 3		RW	See Detail From Convert Ratio Table		0
Bit3	Conv. Rate 2		RW			0
Bit2	Conv. Rate 1		RW			1
Bit1	Conv. Rate 0		RW			0
Bit0	Reserved	Reserved	RW	-	-	0

Byte16	Name	Control Function	Type	0	1	PWD
Bit7	TEMP_CH1<10:3>	MSB of Temperature	R	-	SIGN	0
Bit6			R		64	0
Bit5			R		32	0
Bit4			R		16	0
Bit3			R		8	0
Bit2			R		4	0
Bit1			R		2	0
Bit0			R		1	0

Byte17	Name	Control Function	Type	0	1	PWD
Bit7	Reserved	Reserved	R	-	-	0
Bit6	Reserved	Reserved	R	-	-	0
Bit5	Reserved	Reserved	R	-	-	0
Bit4	Reserved	Reserved	R	-	-	0
Bit3	Reserved	Reserved	R	-	-	0
Bit2	TEMP_CH1<2:0>	LSB of Temperature	R	-	0.5	0
Bit1			R		0.25	0
Bit0			R		0.125	0

Byte 18 ~ Byte 40 Reserved Registers

Byte41	Name	Control Function	Type	0	1	PWD
Bit7	STOP_27M_48M	Stop 27M_48M output	RW	Stopped	Run	1
Bit6	Reserve	Reserve	RW	Reserve	Reserve	1
Bit5	Reserve	Reserve	RW	Reserve	Reserve	1
Bit4	Reserve	Reserve	RW	Reserve	Reserve	1
Bit3	EN_STOP25M_A	25M_A free run control	RW	Free-Run	Stoppable	0
Bit2	Reserve	Reserve	RW	Reserve	Reserve	1
Bit1			RW		Reserve	1
Bit0			RW		Run	1

Byte42	Name	Control Function	Type	0	1	PWD
Bit7	BYTE COUNT Register Bit[7:0]	MSB	RW	-	-	0
Bit6		-	RW	-	-	0
Bit5		-	RW	-	-	0
Bit4		-	RW	-	-	1
Bit3		-	RW	-	-	1
Bit2		-	RW	-	-	1
Bit1		-	RW	-	-	1
Bit0		LSB	RW	-	-	1

Byte 43 ~ Byte 46 Reserved Registers

Byte47	Name	Control Function	Type	0	1	PWD
Bit7	REV_ID	Revision ID	RW	-	-	0
Bit6			RW	-	-	0
Bit5			RW	-	-	0
Bit4			RW	-	-	0
Bit3	VENDOR_ID	Vendor ID (IDT=0001)	RW	-	-	0
Bit2			RW	-	-	0
Bit1			RW	-	-	0
Bit0			RW	-	-	1

Byte 48 ~ Byte 63 Reserved Registers

Byte64	Name	Control Function	Type	0	1	PWD
Bit7	Reserved	-	RW	-	-	1
Bit6	REF COUNT<6:0>	PLL M Counter	RW	-	-	0
Bit5			RW	-	-	0
Bit4			RW	-	-	1
Bit3			RW	-	-	1
Bit2			RW	-	-	0
Bit1			RW	-	-	0
Bit0			RW	-	-	1

Byte65	Name	Control Function	Type	0	1	PWD
Bit7	VCO COUNT<9:2>	PLL N COUNTER	RW	-	-	0
Bit6			RW	-	-	0
Bit5			RW	-	-	0
Bit4			RW	-	-	1
Bit3			RW	-	-	1
Bit2			RW	-	-	0
Bit1			RW	-	-	1
Bit0			RW	-	-	1

Byte 66 Reserved Register

Byte67	Name	Control Function	Type	0	1	PWD
Bit7	SL<1:0>(25MHzB)	25M_B Slew Rate Control	RW	00 = 0.5V/ns	01 = 1.0V/ns	0
Bit6			RW	10 = 1.0V/ns	11 = 1.5V/ns	1
Bit5	SL<1:0>(25MHzA)	25M_A Slew Rate Control	RW	00 = 1,0V/ns	01 = 1.5V/ns	0
Bit4			RW	10 = 1.5V/ns	11 = 2.0V/ns	1
Bit3	SL<1:0>(27MHz)	27M Slew Rate Control	RW	00 = 1,0V/ns	01 = 1.5V/ns	0
Bit2			RW	10 = 1.5V/ns	11 = 2.0V/ns	1
Bit1	SL<1:0>(24MHz)	24M Slew Rate Control	RW	00 = 1,0V/ns	01 = 1.5V/ns	0
Bit0			RW	10 = 1.5V/ns	11 = 2.0V/ns	1

****

All Reserved bits and Reserved bytes in this SMBus table should not be overwritten at any instance. Writing to these Reserved bits and bytes may cause unexpected behavior. IDT does not warrant any application issue going forward if continuing to overwrite these Reserve bits and bytes.

****

Frequency Generator 32.768 kHz

Recommended 25MHz Quartz Crystal Specifications

SMD 25MHz AT cut crystal and maximum driver level at 100μΩ, for example TXC.

VBAT Battery Recommendations and Connection Considerations

Recommended to use coin cell battery CR2032, CR2025 or equivalent.

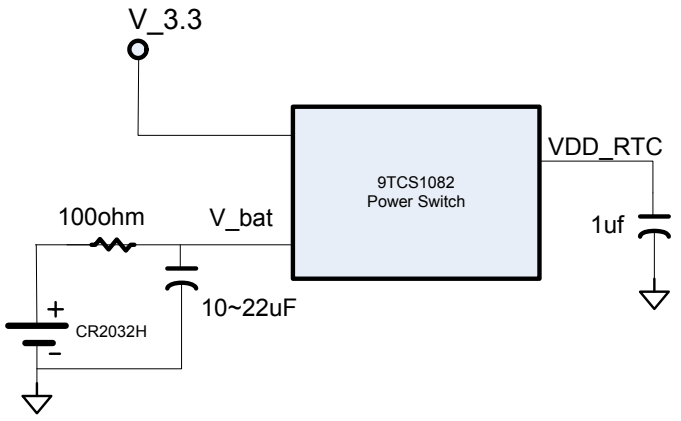
The normal coin cell battery storage capacity is 170 mAh to 220mAh and the average total RTC circuit current required 5uA, the battery life will be at least:

170,000 μAh / 5 μA = 34,000 hours = 3.88 years

The RTC circuit (PCH) usually consumes 3μA power, thus the 32.768kHz clock generator circuit needs be less than 2μA. The 9TCS1082 32.768kHz generator averaged operation current is less than 2μA.

The coin cell battery with 9TCS1082 VBAT power pin connection requires a 100 ohm and 22μF ceramic capacitor current limitation and noise filtering. The RC needs to be added to the battery to limit the current spikes effects.

The VDD_RTC connect to the Intel PCH/ICH chip and the 9TCS1082 provide seamless power switching between main V_3.3 and V_bat.



32.768K Clocks Operation

The 9TCS1082 32.768K clock output operates in two modes:

1. When the system is not power ON, V_3.3 is not ready and 9TCS1082 is powered with the coin cell battery. The 32kHz comes from the DCO with the digital calibration to keep the accuracy.

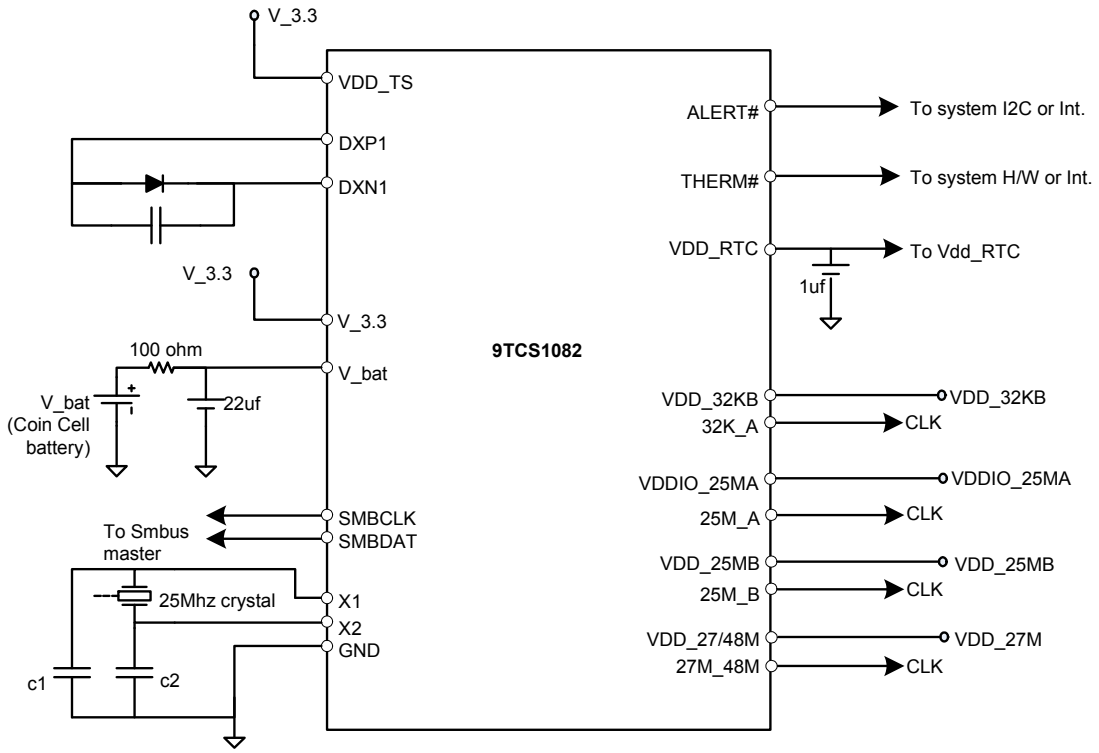
2. After V_3.3 is ready, the 9TCS1082 creates a seamless switch power from V_bat to V_3.3 and the calibration will go to full speed: this will happen every 2~3ms to keep the accuracy and the 32K source will be switched to 25MHz oscillator with Fraction-N divider to get to 0ppm.

32.768K DCO uses a 25Mhz crystal oscillator for calibration reference, thus the 25MHz oscillator must be fine tuned in order to get the best 32.768kHz accuracy.

RTC Routing Guidelines

Single	Trace impedance	Length	Notes
X1	50 ohm	6 inches	
X2	50 ohm	6 inches	

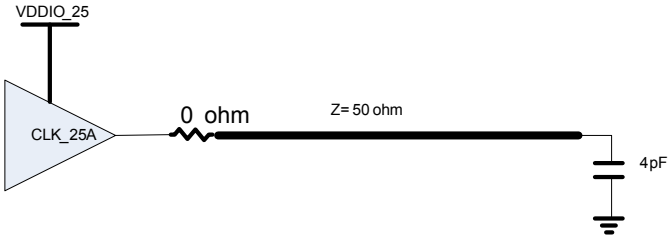
Reference Schematic For VBAT and VDD_RTC



Frequency Synthesizer – 48/27/25 MHz

The 9TCS1082 includes a low power PLL to generate 27/48 MHz clock outputs. The PLL uses an external 25MHz crystal for reference clock input, thus all 25MHz clock outputs are through a fanout buffer directly for optimal performance. Fine tuning on the external crystal cap load is required to get an accurate 25MHz reference clock.

25MHz_A Connection Recommendations



a. VDDIO_25A range is from 1.05V to 3.3V.

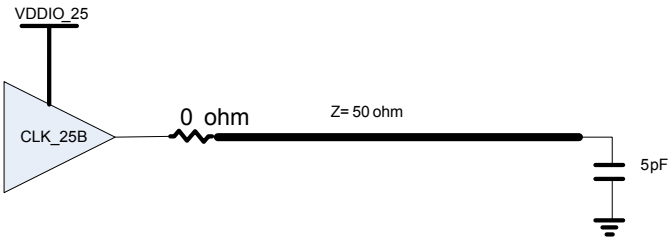
b. Optimize range is 1.05V to 1.5V.

c. Pull up strength is 50 ohm@VDDIO_25A=1.5V

d. Pull down strength is 50 ohm.

e. No on-board 33 ohm series resistor is required.

25MHz_B Connection Recommendations



a. VDD_25B range is from 1.05V to 3.3V.

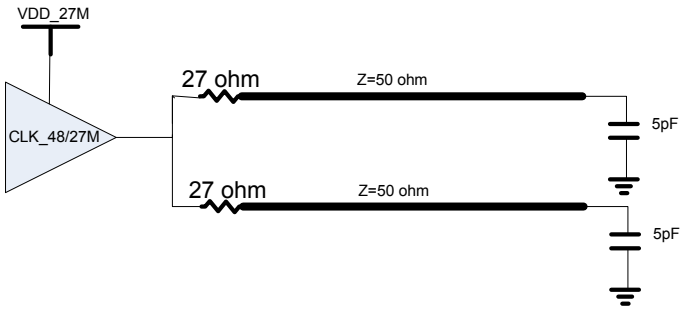
b. Optimized for 3.3V VDDIO.

c. Pull up strength is 50 ohm@VDD_25B=3.3V

d. Pull down strength is 50 ohm.

e. No on-board 33 ohm series resistor is required.

27/48MHz Connection Recommendations



a. Default 2X push-pull IO drive strength for 48/27MHz.

b. On board 27 ohm series resistor for each path.

c. Rising/falling slew rate: 1v/ns~4v/ns

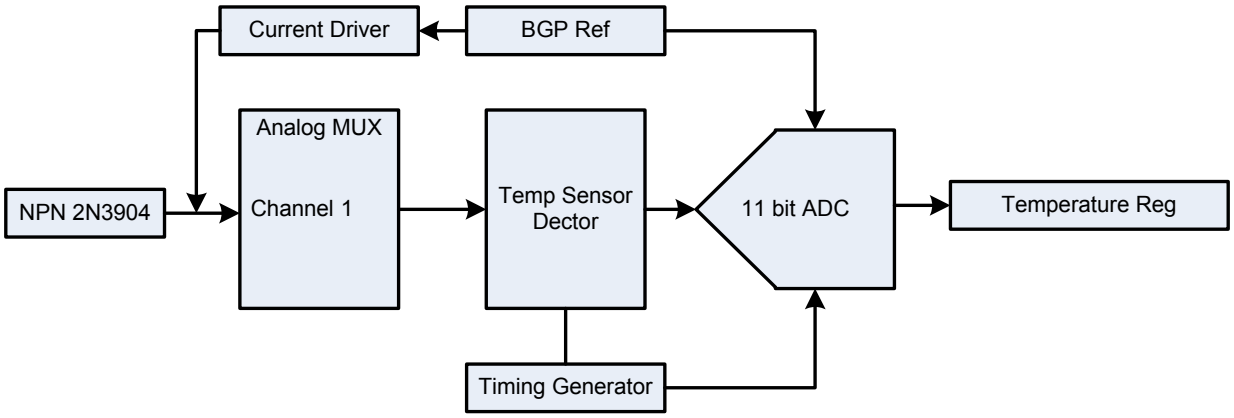
d. 2 bits (3 steps) I2C for the Slew Rate.

Thermal Sensor

The thermal sensor in the 9TCS1082 is a low power and highly accurate temperature sensor. It is optimized to operate between 60°C to 100°C. There is one external thermal diode connection input and one internal diode temperature sensor. The chip supports diode faults and temperature alerts for the thermal sensor; Moreover, the thermal sensor has the capability to go into standby mode for power savings.

The temperature sensor's analog to digital converter (ADC) has 11 bits of resolution. One LSB is equal to 0.125°C. The accuracy of the temperature sensor is ±1°C between 60°C - 100°C.

The 9TCS1082 temperature sensor has the ability to cancel the series resistance on the remote diode inputs. Parasitic resistances to the DXP and DXN inputs seen in series with the remote diode are caused by PCB trace resistance along with the overall length, bulk parasitic resistance in the remote temperature transistor junctions, and series resistance in the CPU. This resistance appears as a temperature offset in the thermal sensor measurement and is approximately +0.7°C per Ohm. The 9TCS1082 has the ability to cancel up to 100Ω of series resistance.



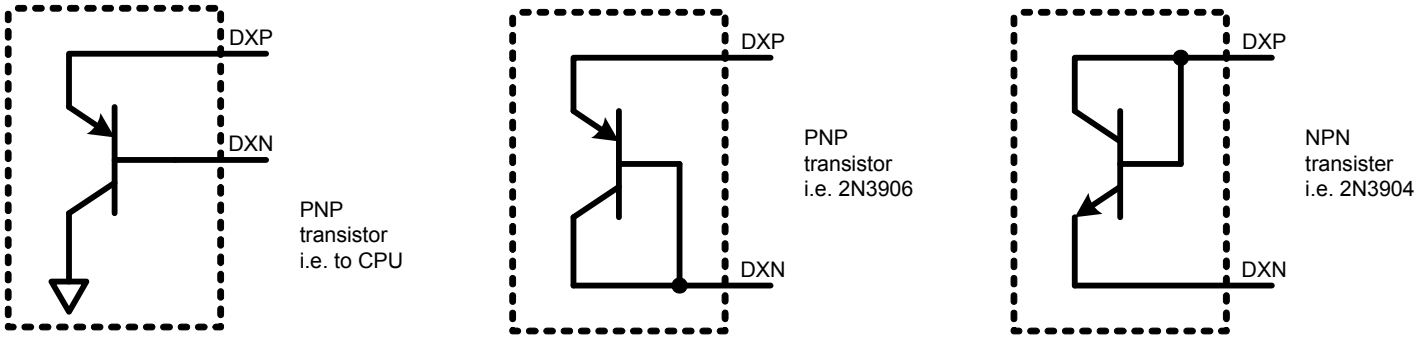
The thermal sensor in 9TCS1082 outputs the measured temperature from a beta compensated temperature reading from an external diode. The temperature sensor architecture uses an on-chip ADC as shown to convert the analog temperature into an 11-bit digital code. Using averaging techniques along with the ADC architecture allows accurate temperature measurements. The ability to have programmable conversion rates and adjustable averaging schemes allow the user the flexibility to balance accuracy versus conversion speed per the system requirements.

The temperature measurement relies on the characteristics of a semiconductor junction operating at a fixed current level. Forcing a fixed current through the temperature diodes and detecting the changes in VBE, the forward voltage of the diode, the temperature proportionality can be determined.

External Thermal Diode Selection

The 9TCS1082 supports the following temperature diodes:

- Typical remote substrate transistor (i.e. CPU substrate PNP intrinsic diode)
- Discrete PNP transistor diode (i.e. 2N3906)
- Discrete NPN transistor diode (i.e. 2N3904)



When the thermal sensor is used in a noisy environment, a capacitor can be connected across DXP and DXN to provide some noise filtering capabilities. However, large capacitances affect the accuracy of the temperature measurement. A maximum capacitance of 300pF can be used to help mitigate the noise.

Thermal Diode Fault Conditions

9TCS1082 has the ability to detect an open or a short condition for each temperature sensor diode. An external diode fault is defined as one of the following:

- An open between DXP and DXN
- A short from VDD to DXP
- A short from VDD to DXN

The diode fault monitoring is enabled at the start of every temperature measurement. When an external diode fault is detected, the ALERT# pin asserts and the temperature data reads 00h in the MSB and LSB of the corresponding temperature registers:

- DX1 MSB - byte[17], bit[2:0]
- DX1 LSB - byte[16], bit[7:0]

During the fault condition, byte[13], bit[1] or bit[0], will be set depending on the channel that has the fault. Bit[1] corresponds to DX1, and furthermore, an open/short fault flag will be set in register byte[14], bit[4].

Temperature Threshold Alerts

Through register writes, the high and low temperature limits can be set such that it will trigger an alert. This alert can be monitored through the registers or can be sent to the ALERT# pin. The programmable register to set the thresholds is as follows:

(1) High Temperature Alert (default 127°C)

Byte[2:0], Bit[7:0]	Temperature
Bit[7]	Sign Bit
Bit[6]	64°C
Bit[5]	32°C
Bit[4]	16°C
Bit[3]	8°C
Bit[2]	4°C
Bit[1]	2°C
Bit[0]	1°C

Where byte[0] is the high temperature alert for DX1.

(2) Low Temperature Alert (default 127°C)

Byte[5:3], Bit[7:0]	Temperature
Bit[7]	Sign Bit
Bit[6]	64°C
Bit[5]	32°C
Bit[4]	16°C
Bit[3]	8°C
Bit[2]	4°C
Bit[1]	2°C
Bit[0]	1°C

Where byte[3] is the low alert for DX1.

Temperature Threshold Alert Status

When a temperature threshold alert is activated, a status indicator bit is also set. Register byte[14], bit[6:5] will be set depending on the high or low alert. Bit[6] is the high and bit[5] is the low alert flag. To clear the alert, register byte[15], bit[7] needs to be written with a "1". Writing this bit will also clear the critical thermal warnings.

Temperature Threshold ALERT# Pin

The temperature threshold alerts are sent to the ALERT# pin. To mask this alert being sent to the ALERT# pin, set register byte[12], bit7 to logic 1. Bit7 corresponds to channel 1.

Consecutive Alerts

The number of temperature threshold alerts before the assertion of the ALERT# pin can be set by the user through register byte[6], bit[3:2] as follows:

Byte[6], Bit[3:2]	Number of Alert Events
[00] (default)	1
[01]	2
[10]	3
[11]	4

Temperature Threshold Alert Alarm Register

The temperature channel has a readable register, byte[13], bit[3:2] that is set when a temperature threshold alert has occurred.

Critical Thermal Warnings

The 9TCS1082 will have register programmable critical thermal threshold warnings for temperature sensor. Similar to the temperature threshold alerts, the critical high temperatures can be set such that a warning can be dispatched to the THERM# pin and the readable registers. The thermal warnings also have programmable hysteresis. Each channel has its own programmable register to set the thresholds as follows:

(1) Critical Thermal Warning (default 127°C)

Byte[9:7], Bit[6:0]	Temperature
Bit[6]	64°C
Bit[5]	32°C
Bit[4]	16°C
Bit[3]	8°C
Bit[2]	4°C
Bit[1]	2°C
Bit[0]	1°C

Where byte[7] is the critical thermal warning for DX1.

(2) Critical Thermal Warning Temperature Hysteresis (default 4°C)

Byte[12], Bit[4:0]	Temperature
Bit[4]	16°C
Bit[3]	8°C
Bit[2] (default)	4°C
Bit[1]	2°C
Bit[0]	1°C

Critical Thermal Warning Status

When a critical warning is activated, a status indicator bit is also set. Register byte[14], bit2 will be set depending on the thermal sensor has detected the critical event.

Critical Thermal Warning THERM# Pin

The critical thermal warnings are sent to the THERM# pin and requires a system register write to byte[15], bit[7] to reset. This fault clear I2C write will also clear the temperature threshold alerts

Active/Standby Mode

The thermal sensor has two modes in the temperature conversion process:

(1) Active mode – In this mode the ADC will have a selectable conversion rate for the temperature sensing.

(2) Standby mode – The system will command via I2C the 9TCS1082 to sample the temperature sensors. Once the temperature reading from the ADC is updated, the temperature sensor will be on stand-by awaiting the next system request.

Register byte[15], bit[6] controls whether the thermal sensor is in active or standby mode.

The conversion rate programmable register detail is as follows:

Byte[17], Bit[4:1]	Conversion Rate
[0000]	16/sec
[0001]	8/sec
[0010] (default)	4/sec
[0011]	2/sec
[0100]	1/sec
[0101]	1/2 sec
[0110]	1/4 sec
[0111]	1/8 sec
[1000]	1/16 sec
[1001]	1/32 sec
[1010]	1/64 sec

The thermal sensor architecture has dynamic averaging to smooth out the temperature conversion readings. To select the number of temperature reading averages requires the dynamic averaging function to be enabled, register byte[15], bit[5]. The number of averages is then selected as follows:

Byte[6], Bit[1:0]	Average the ADC Temperature
[00]	1
[01]	4
[10]	8
[11]	16

Marking Diagram (NLG32)

Notes:

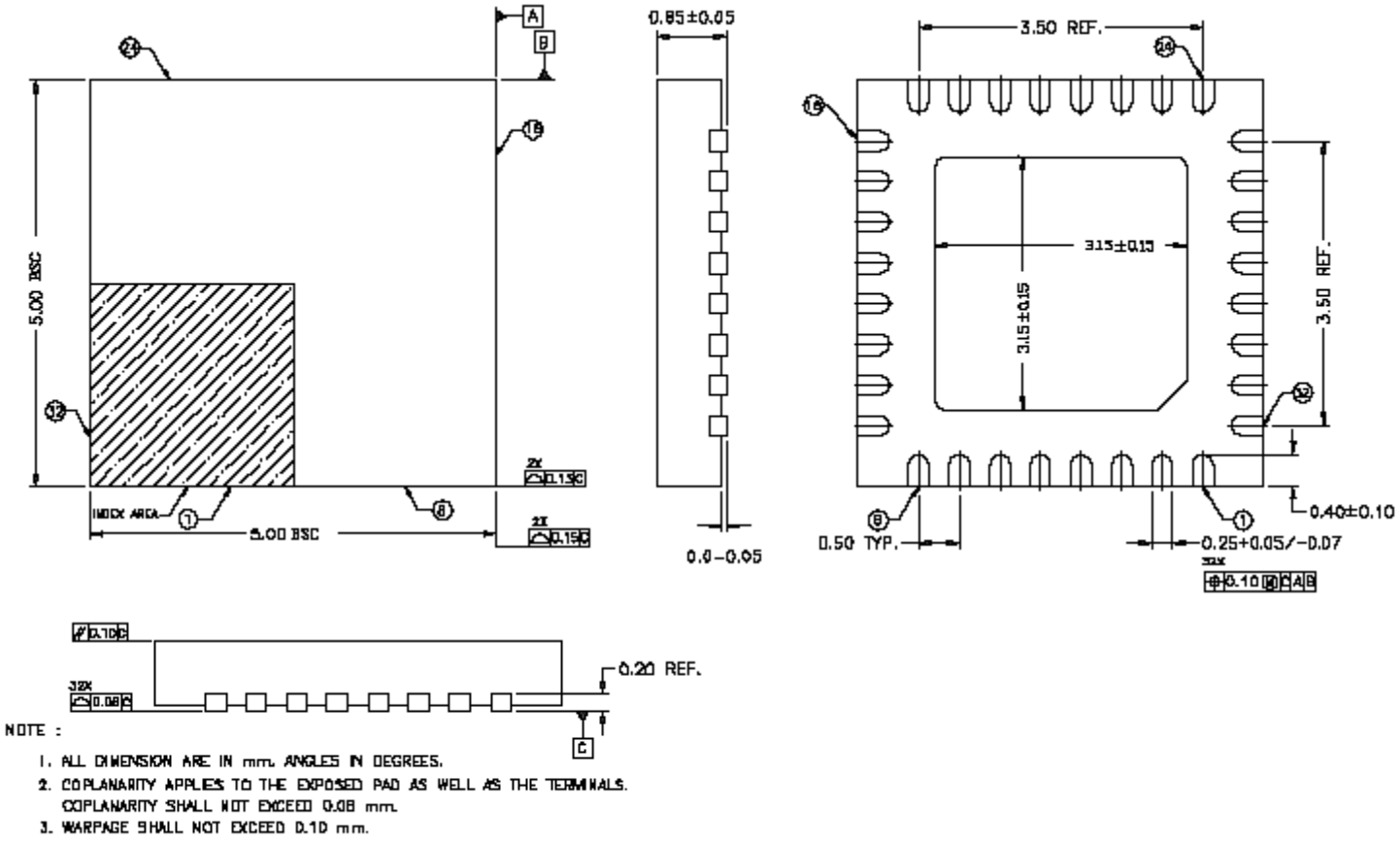
1. “######” is the lot number.
2. YYWW is the last two digits of the year and week that the part was assembled.
3. “$$$” is the assembly mark code.
4. “B” at the end of the part number is the device revision designator; does not correlate with the datasheet revision.
5. Bottom marking: country of origin if not USA.

Thermal Characteristics 32-pin VFQFPN

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		34		°C/W
	θ_{JA}	1 m/s air flow		29		°C/W
	θ_{JA}	3 m/s air flow		27		°C/W
Thermal Resistance Junction to Case	θ_{JC}			32		°C/W

Package Outline and Package Dimensions (32-pin VFQFPN, 0.50mm pitch)

Package dimensions are kept current with JEDEC Publication No. 95



Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
9TCS1082BNLG	see page 25	Trays	32-pin VFQFPN	0 to +70° C
9TCS1082BNLG8		Tape and Reel	32-pin VFQFPN	0 to +70° C

“G” after the two-letter package code are the Pb-Free configuration and are RoHS compliant.

“B” is the device revision designator – will not correlate to the datasheet revision.

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