

## CA3224E

Automatic Picture Tube Bias Control Circuit

FN1553  
Rev 2.00  
October 2002

### Description

The CA3224E is an automatic picture tube bias control circuit used in color TV receiver CRT drive circuits. It is used to provide dynamic bias control of the grey scale both initially and over the CRT operating life, compensating for CRT cut-off changes.

The CA3224E provides automatic continuous control of the cutoff current in each gun of a three-gun color CRT. From an input pulse amplitude proportional to the difference between the desired and the actual CRT cutoff, a gated sample/hold circuit generates a DC correction voltage which correctly biases the CRT driver circuit. The sample/hold bias correction takes place each frame following the vertical blanking. Figure 1 shows a block diagram of the CA3224E. The functions include three identical servo loop transconductance amplifiers with a sample/hold switch and buffer amplifier plus control logic, internal bias and a mode.

### Features

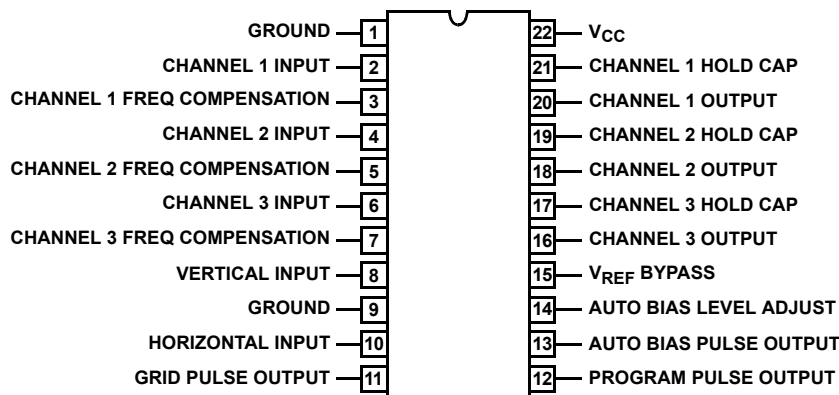
- Automatic Picture Tube Bias Cutoff Control
- Automatic Background Color Balance
- Eliminates Grey Scale Adjustments
- Compensates for Cathode-to-Heater Leakage
- Electrostatic Protection on All Pins
- Servo Loop Design
- Wide Dynamic Range
- Three-Gun Control
- Minimal External Components

### Part Number Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3224E	-40 to 85	22 Ld PDIP	E22.4

### Pinout

CA3224E  
(PDIP)  
TOP VIEW



**Absolute Maximum Ratings**  $T_A = 25^\circ\text{C}$ 

Supply Voltage ( $V_{CC}$ ) ..... 11V  
 DC Input Voltage ..... -1 to  $V_{CC}$   
 Output Current ..... Short Circuit Protected

**Operating Conditions**

Temperature Range .....  $-40^\circ\text{C}$  to  $85^\circ\text{C}$   
 Supply Voltage Range (Typical) .....  $10V \pm 10\%$

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

**NOTE:**

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

**Thermal Information**

Thermal Resistance (Typical, Note 1)  $\theta_{JA}$  ( $^\circ\text{C}/\text{W}$ )  
 PDIP Package ..... 60  
 Maximum Junction Temperature (Plastic Package) .....  $150^\circ\text{C}$   
 Maximum Storage Temperature Range .....  $-65^\circ\text{C}$  to  $150^\circ\text{C}$   
 Maximum Lead Temperature (Soldering 10s) .....  $300^\circ\text{C}$

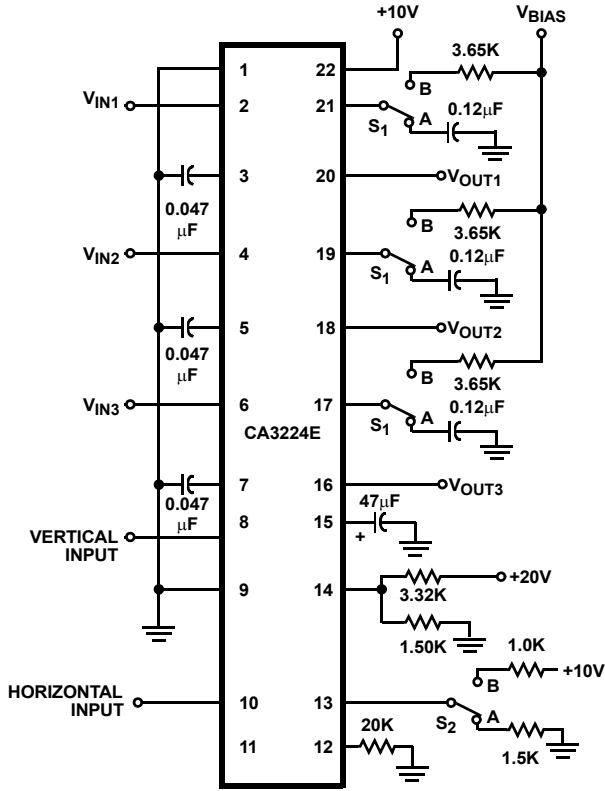
**Electrical Specifications** At  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 10V$ ,  $V_{BIAS} = 3.75V$ ,  $V_V$  (Pin 8) =  $V_H$  (Pin 10) =  $6.0V$ ,  $S_1 = A$ ,  $S_2 = A$ ,  
 See Test Circuit and Timing Diagrams

PARAMETER		TEST PIN NO.	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current		22	$I_{CC}$		-	-	65	mA
Reference Voltage		2, 4, 6	$V_{REF}$	Measure at $t_4$	5.6	6.0	6.4	V
Input Current		2, 4, 6	$I_I$	$V_{IN} = 7.2V$ , $S_1 = B$	-	-	250	nA
Output Current	Source	17, 19, 21	$I_{OM+}$	$V_{BIAS} = 0.5V$ , Measure at $t_6$ , $S_1 = B$	-	-	-0.8	mA
	Sink		$I_{OM-}$	$V_{BIAS} = 7.0V$ , Measure at $t_6$ , $S_1 = B$	0.8	-	-	mA
Output Buffer	Input Current	17, 19, 21	$I_I$	$V_{OUT} = 6.5V$ , $V_{IN}$ At pins 16, 18, 20, Measure at $t_4$ , $S_1 = B$	-	-	150	nA
	Voltage Gain		$A_V$		0.97	-	1.07	-
Transconductance		17, 19, 21	$g_M$	Measure at $t_6$ , $V_{IN} = 8mV_{P-P}$ at 40kHz, $S_1 = B$	50	-	100	mS
Auto Bias Pulse	Output Low	13	$V_{OL}$	Measure at $t_1$	-	-	0.3	V
	High		$V_{OH}$	Measure at $t_4$	6.05	-	-	V
	Current Sink		$I_{OM-}$	Measure at $t_4$ , $S_2 = B$	2.5	-	-	mA
Grid Pulse Output	Low	11	$V_{OL}$	Measure at $t_4$	-	-	0.4	V
	High		$V_{OH}$	Measure at $t_1$	4.2	-	-	V
Program Pulse Output	Low	12	$V_{OL}$	Measure at $t_6$	-	-	0.4	V
	High		$V_{OH}$	Measure at $t_1$	8.2	-	-	V
Vertical Input		8	$V_V$	See Figure 3	-	6.0	-	V
Horizontal Input		10	$V_H$	See Figure 3	-	6.0	-	V
Auto Bias Pulse Timing	Start	13		$t_0$ to $t_2$ , Note 2	835	-	842	$\mu\text{s}$
	Finish			$t_0$ to $t_7$ , Note 2	1270	-	1275	$\mu\text{s}$
Grid Pulse Timing	Start	11		$t_0$ to $t_3$ , Note 2	899	-	905	$\mu\text{s}$
	Finish			$t_0$ to $t_5$ , Note 2	1080	-	1084	$\mu\text{s}$
Program Pulse Timing	Start	12		$t_0$ to $t_5$ , Note 2	1080	-	1084	$\mu\text{s}$
	Finish			$t_0$ to $t_7$ , Note 2	1270	-	1275	$\mu\text{s}$

**NOTE:**

- All time measurements are made from 50% point to 50% point.

**Test Circuit**



**Device Description and Operation** (See Figures

1, 2, 4 and 5)

During the vertical retrace interval, 13 horizontal sync pulses are counted. On the 14th sync pulse the auto-bias pulse

output goes high. This is used to set the RGB drive of the companion chroma/luma circuit to black level. The auto-bias pulse stays high for 7 horizontal periods during the auto-bias cycle.

On the 15th horizontal sync pulse, the internal logic initiates the setup interval. During the setup interval, the cathode current is increased to a reference value (A in Figure 5) through the action of the grid pulse. The cathode current causes a voltage drop across  $R_S$ . This voltage drop, together with the program pulse output results in a reference voltage at  $V_S$  (summing point) which causes capacitor  $C_1$  to charge to a voltage proportional to the reference cathode current. The setup interval lasts for 3 horizontal periods.

On the 18th horizontal sync pulse the grid pulse output goes high, which through the grid pulse amplifier/inverter, causes the cathode current to decrease. The decrease in cathode current results in a positive recovered voltage pulse with respect to the setup reference level at the  $V_S$  summing point. The positive recovered voltage pulse is summed with a negative voltage pulse caused by the program pulse output going low (cutting off Diode D1 and switching in resistors R1 and R2). Any difference between the positive and negative pulses is fed through capacitor  $C_1$  to the transconductance amplifier. The difference signal is amplified in the transconductance amplifier and charges the hold capacitor  $C_2$ , which, through the buffer amplifier, adjusts the bias on the driver circuit.

Components  $R_S$ , R1, and R2 must be chosen such that the program pulse and the recovered pulse just cancel at the desired cathode cutoff level.

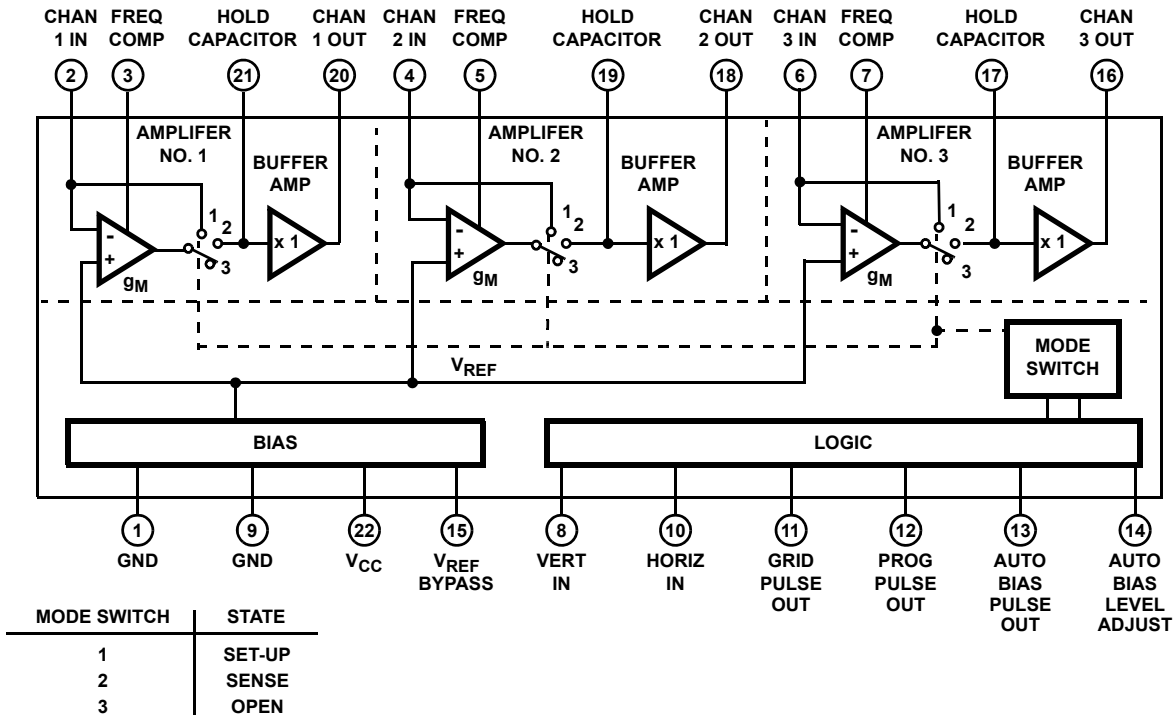


FIGURE 1. FUNCTIONAL BLOCK DIAGRAM

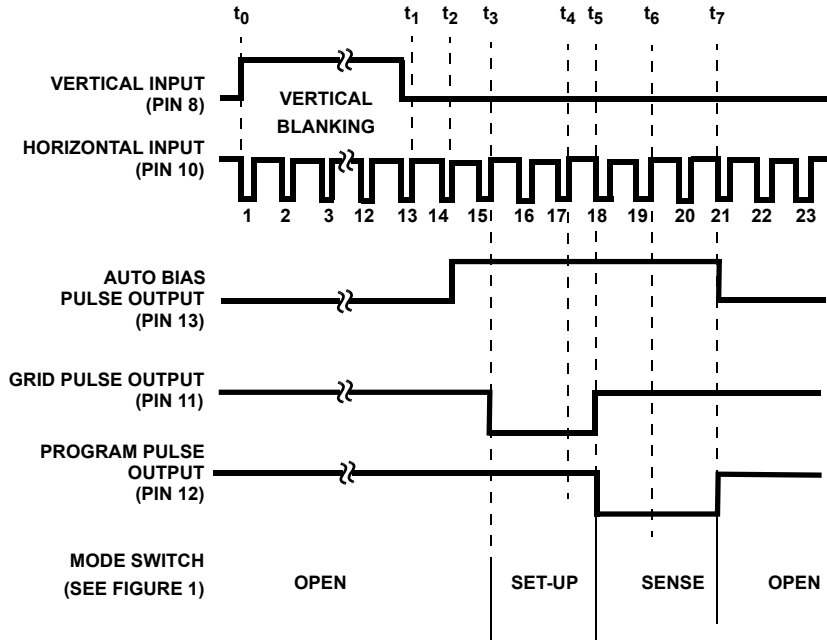


FIGURE 2. FUNCTIONAL TIMING DIAGRAMS

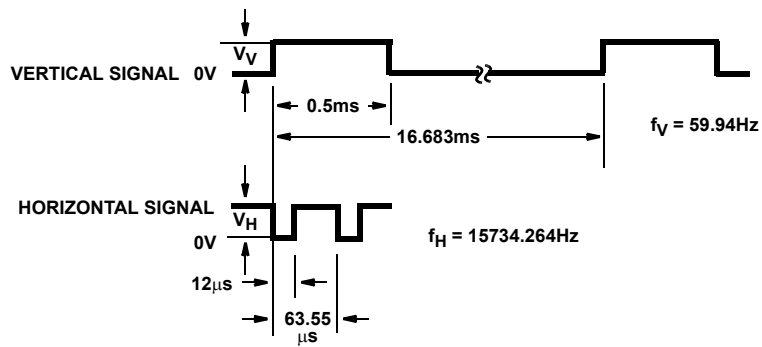
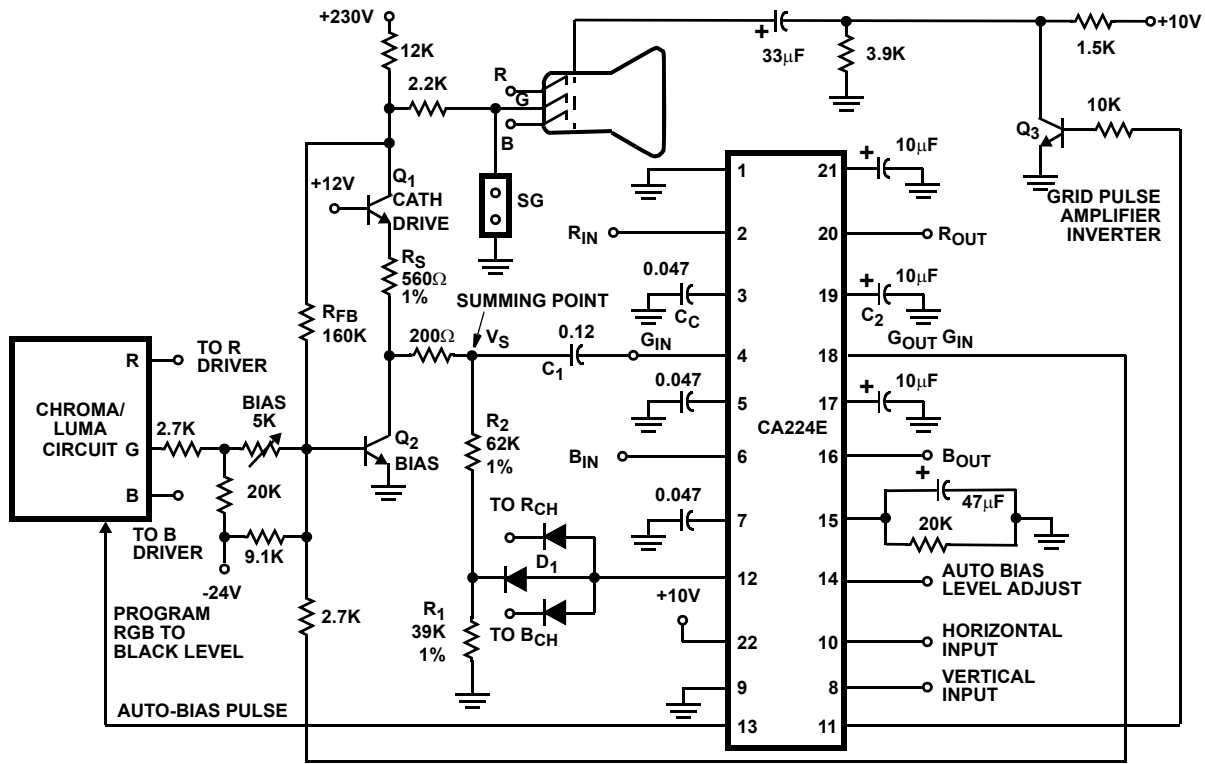


FIGURE 3. VERTICAL AND HORIZONTAL INPUT SIGNALS



NOTE:

3. One of three identical driver circuits shown.

FIGURE 4. TYPICAL APPLICATION CIRCUIT

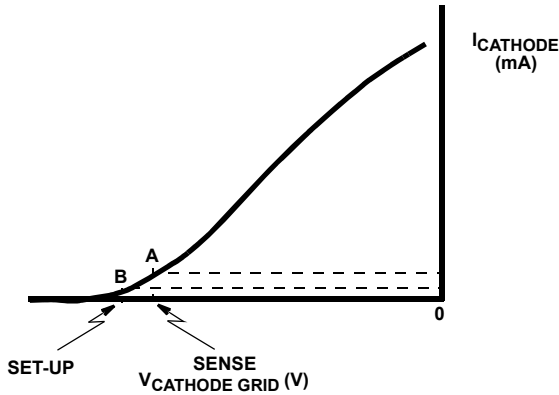


FIGURE 5. PICTURE TUBE V-I CURVE

**Electrostatic Protection** (Note)

When correctly designed for ESD protection, SCRs can be highly effective, enabling circuits to be protected to well in excess of 4kV. The SCR ESD-EOS protection structures used on each terminal of the CA3224E are shown schematically in either Figures 6A or 6B. Although ESD-EOS protection is included in the CA3224E, proper circuit board layout and grounding techniques should be observed.

NOTE: For further information on CA3224E protection structures refer to: AN7304, "Using SCRs as Transient Protection Structures in Integrated Circuits", by L.R. Avery.

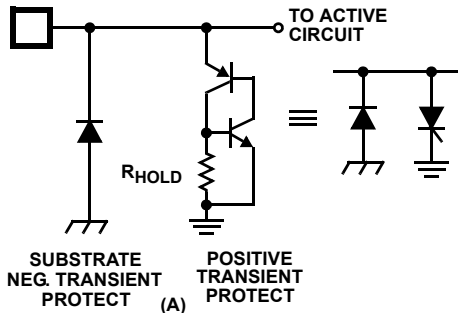


FIGURE 6A.

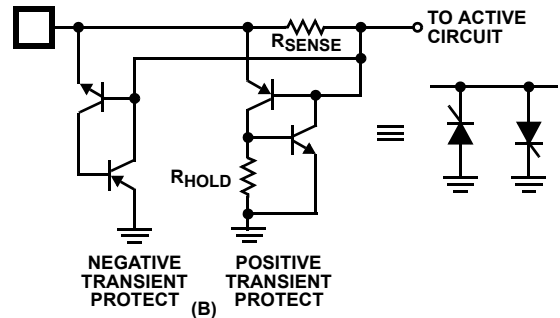
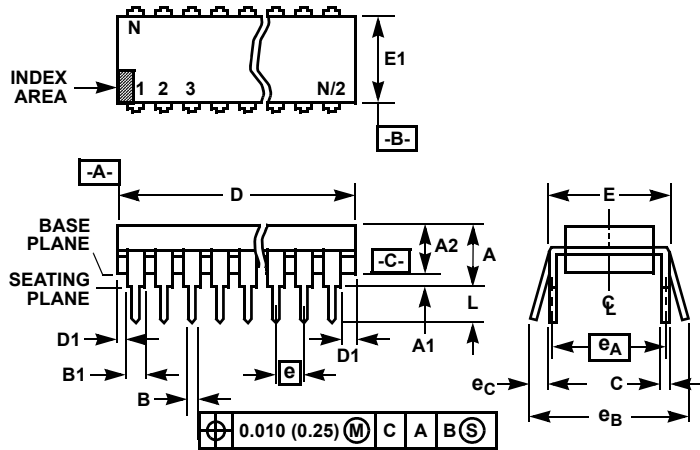


FIGURE 6B.

FIGURE 6. TRANSIENT PROTECTION

**Dual-In-Line Plastic Packages (PDIP)**



**NOTES:**

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e<sub>A</sub> are measured with the leads constrained to be perpendicular to datum -C-.
7. e<sub>B</sub> and e<sub>C</sub> are measured at the lead tips with the leads unconstrained. e<sub>C</sub> must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

**E22.4 (JEDEC MS-010-AA ISSUE C)  
22 LEAD DUAL-IN-LINE PLASTIC PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.065	1.15	1.65	8
C	0.009	0.015	0.229	0.381	-
D	1.065	1.120	27.06	28.44	5
D1	0.005	-	0.13	-	5
E	0.390	0.425	9.91	10.79	6
E1	0.330	0.390	8.39	9.90	5
e	0.100 BSC		2.54 BSC		-
e <sub>A</sub>	0.400 BSC		10.16 BSC		6
e <sub>B</sub>	-	0.500	-	12.70	7
L	0.115	0.160	2.93	4.06	4
N	22		22		9

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