2.5V PHASE LOCKED LOOP CLOCK DRIVER

IDTCSPT855

FEATURES:

- **PLL clock driver for DDR (Double Data Rate) synchronous DRAM applications**
- **Spread spectrum clock compatible**
- **Operating frequency: 60MHz to 220MHz**
- **Low jitter (cycle-to-cycle): ±50ps**
- **Distributes one differential clock input to four differential clock outputs**
- **Enters low power mode and 3-state outputs when input CLK signal is less than 20MHz or PWRDWN is low**
- **Operates from a 2.5V supply**
- **Consumes <200µA quiescent current**
- **External feedback pins (FBIN, $\overline{\text{FBIN}}$) are used to synchronize outputs to input clocks**
- **Available in TSSOP package**

APPLICATIONS:

- **For all DDR1 speeds: PC1600 (DDR200), PC2100 (DDR266), PC2700 (DDR333), PC3200 (DDR400)**

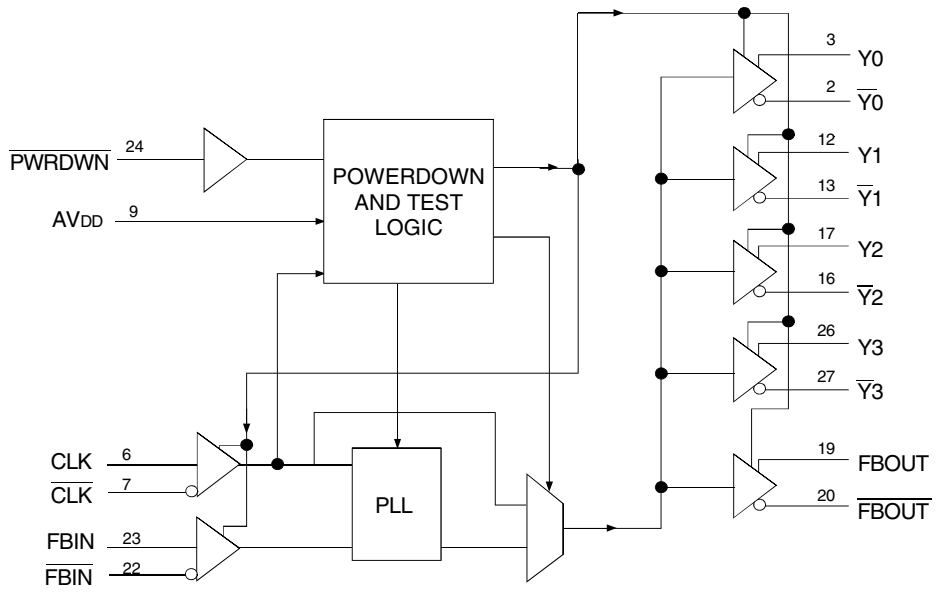
DESCRIPTION:

The CSPT855 is a high-performance, low-skew, low-jitter zero delay buffer that distributes one differential clock input pair(CLK, $\overline{\text{CLK}}$) to four differential output pairs ($Y_{[0:3]}$, $\overline{Y}_{[0:3]}$) and one differential pair of feedback clock outputs (FBOUT, $\overline{\text{FBOUT}}$). When $\overline{\text{PWRDWN}}$ is high, the outputs switch in phase and frequency with CLK. When $\overline{\text{PWRDWN}}$ is low, all outputs are disabled to a high-impedance state (3-state), and the PLL is shut down (low-power mode). The device also enters this low-power mode when the input frequency falls below a suggested detection frequency that is below 20MHz (typical 10MHz). An input frequency detection circuit detects the low-frequency condition, and after applying a >20MHz input signal, this detection circuit reactivates the PLL and enables the outputs.

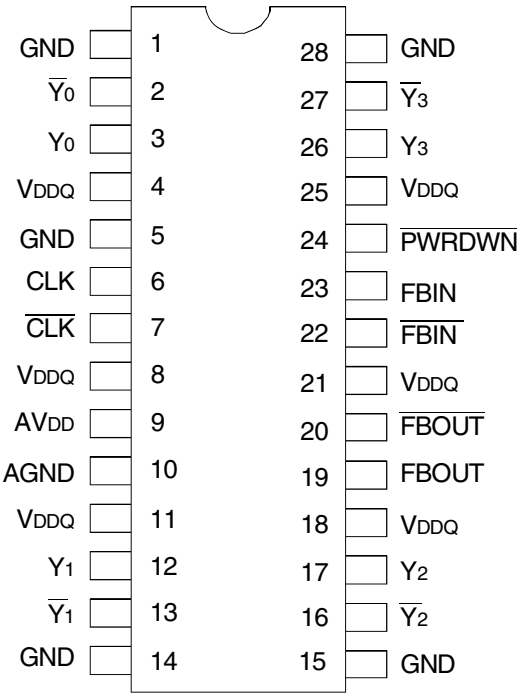
When AV_{DD} is tied to GND, the PLL is turned off and bypassed for test purposes. The CSPT855 is also able to track spread spectrum clocking for reduced EMI.

Since the CSPT855 is based on PLL circuitry, it requires a stabilization time to achieve phase-lock of the PLL. This stabilization time is required following power up.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Max	Unit
V_{DDQ}, AV_{DD}	Supply Voltage Range	–0.5 to +3.6	V
V_I(2)	Input Voltage Range	–0.5 to V_{DDQ} + 0.5	V
V_O(2)	Output Voltage Range	–0.5 to V_{DDQ} + 0.5	V
I_{IK} (V_I < 0 or V_I < V_{DDQ})	Input Clamp Current	±50	mA
I_{OK} (V_O < 0 or V_O > V_{DDQ})	Output Clamp Current	±50	mA
I_O (V_O = 0 to V_{DDQ})	Continuous Output Current	±50	mA
V_{DDQ} or GND	Continuous Current	±100	mA
θ_{JA}(3)	Package Thermal Impedance	105.8	°C/W
T_{STG}	Storage Temperature Range	– 65 to +150	° C

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed. This value is limited to 3.6V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

PIN DESCRIPTION

Pin Name	Pin Number	I/O	Description
AGND	10		Ground for analog supply
AV_{DD}	9		Analog supply
CLK, $\overline{CLK}$	6, 7	I	Differential clock input
$\overline{FBIN}$, FBIN	22, 23	I	Feedback differential clock input
FBOUT, $\overline{FBOUT}$	19, 20	O	Feedback differential clock output
GND	1, 5, 14, 15, 28		Ground
$\overline{PWRDWN}$	24	I	Control input to turn device in the power-down mode
V_{DDQ}	4, 8, 11, 18, 21, 25		I/O supply
$Y_{[0:3]}$	3, 12, 17, 26	O	Buffered output copies of input clock, CLK
$\overline{Y_{[0:3]}}$	2, 13, 16, 27	O	Buffered output copies of input clock, $\overline{CLK}$

FUNCTION TABLE(1)

INPUTS				OUTPUTS				
AVDD	$\overline{PWRDWN}$	CLK	$\overline{CLK}$	Y	$\overline{Y}$	FBOUT	$\overline{FBOUT}$	PLL
GND	H	L	H	L	H	L	H	Bypassed/OFF
GND	H	H	L	H	L	H	L	Bypassed/OFF
X	L	L	H	Z	Z	Z	Z	OFF
X	L	H	L	Z	Z	Z	Z	OFF
2.5V (nom)	H	L	H	L	H	L	H	ON
2.5V (nom)	H	H	L	H	L	H	L	ON
2.5V (nom)	X	<20MHz(2)	<20MHz(2)	Z	Z	Z	Z	OFF

NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   Z = High-Impedance OFF-State
   X = Don't Care
2. Typically 10MHz.

RECOMMENDED OPERATING CONDITIONS(1)

Symbol	Parameter		Min.	Typ.	Max.	Unit
AVDD, VDDQ	Supply Voltage		2.3	—	2.7	V
VIL	Input Voltage LOW	CLK, $\overline{CLK}$, FBIN, $\overline{FBIN}$	—	—	VDDQ/2 - 0.18	V
		$\overline{PRWDWN}$	- 0.3	—	0.7	
VIH	Input Voltage HIGH	CLK, $\overline{CLK}$, FBIN, $\overline{FBIN}$	VDDQ/2 + 0.18	—	—	V
		$\overline{PRWDWN}$	1.7	—	VDDQ + 0.3	
	DC Input Signal Voltage(2)		- 0.3	—	VDDQ	V
VID	Differential Input Signal Voltage(3)	CLK, FBIN	0.36	—	VDDQ + 0.6	V
VO(X)	Output Differential Cross-Voltage(4)		VDDQ/2 - 0.2	VDDQ/2	VDDQ/2 + 0.2	V
VI(X)	Input Differential Pair Cross-Voltage(4)		VDDQ/2 - 0.2	—	VDDQ/2 + 0.2	V
IOH	HIGH-Level Output Current		—	—	- 12	mA
IOL	LOW-Level Output Current		—	—	12	mA
SR	Input Slew Rate, see figure 8		1	—	4	V/ns
TA	Operating Free-Air Temperature	Commercial	0	—	+70	°C
		Industrial	-40	—	+85	

NOTES:
1. Unused inputs must be held HIGH or LOW to prevent them from floating.
2. DC input signal voltage specifies the allowable DC execution of differential input.
3. Differential input signal voltage specifies the differential voltage | VTR - VCP | required for switching, where VTR is the true input level and VCP is the complementary input level.
4. Differential cross-point voltage is expected to track variations of VDDQ and is the voltage at which the differential signals must be crossing.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C; Industrial: T_A = –40°C to +85°C

Symbol	Parameter		Conditions	Min.	Typ.[1]	Max.	Unit
V_{IK}	Input Voltage (All Inputs)		V_{DDQ} = 2.3V, I_I = -18mA	—	—	–1.2	V
V_{OH}	HIGH-Level Output Voltage		V_{DDQ} = Min. to Max., I_{OH} = -1mA	V_{DDQ} – 0.1	—	—	V
			V_{DDQ} = 2.3V, I_{OH} = -12mA	1.7	—	—	
V_{OL}	LOW-Level Output Voltage		V_{DDQ} = Min. to Max., I_{OL} = 1mA	—	—	0.1	V
			V_{DDQ} = 2.3V, I_{OL} = 12mA	—	—	0.6	
I_{OH}	HIGH-Level Output Current		V_{DDQ} = 2.3V, V_O = 1V	–18	–32	—	mA
I_{OL}	LOW-Level Output Current		V_{DDQ} = 2.3V, V_O = 1.2V	26	35	—	mA
V_{OD}	Output Voltage Swing		Differential outputs are terminated with 120Ω	1.1	—	V_{DDQ} – 0.4	V
V_{OX}	Output Differential Cross Voltage[2]		Differential outputs are terminated with 120Ω	V_{DDQ}/2 – 0.2	V_{DDQ}/2	V_{DDQ}/2 + 0.2	V
I_I	Input Current		V_{DDQ} = 2.7V, V_I = 0V to 2.7V	—	—	±10	µA
I_{OZ}	High-Impedance State Output Current		V_{DDQ} = 2.7V, V_O = V_{DDQ} or GND	—	—	±10	µA
$I_{DD(PD)}$	Power-Down Current on V_{DDQ} and AV_{DD}		CLK and $\overline{CLK}$ = 0MHz, $\overline{PWRDWN}$ = LOW, Σ of I_{DD} and AI_{DD}	—	100	200	µA
I_{DD}	Dynamic Current on V_{DDQ}	C_L = 14pF	f_O = 167MHz, Differential outputs terminated with 120Ω	—	150	180	mA
		C_L = 0pF	f_O = 167MHz, Differential outputs terminated with 120Ω	—	130	160	
AI_{DD}	Supply Current on AV_{DD}		f_O = 167MHz	—	8	10	mA
C_I	Input Capacitance		V_{DDQ} = 2.5V, V_I = V_{DDQ} or GND	2	2.5	3	pF
C_O	Output Capacitance		V_{DDQ} = 2.5V, V_I = V_{DDQ} or GND	2.5	3	3.5	pF

NOTES:
1. All typical values are at respective nominal V_{DDQ}.
2. Differential cross-point voltage is expected to track variation of V_{DDQ} and is the voltage at which the differential signals must be crossing.

TIMING REQUIREMENTS

Symbol	Parameter	Min.	Max.	Unit
f_{CLK}	Operating Clock Frequency	60	220	MHz
t_{DC}	Input Clock Duty Cycle	40	60	%
t_L	Stabilization Time (PLL Mode)[1]	—	10	µs
t_L	Stabilization Time (Bypass Mode)[2]	—	30	ns

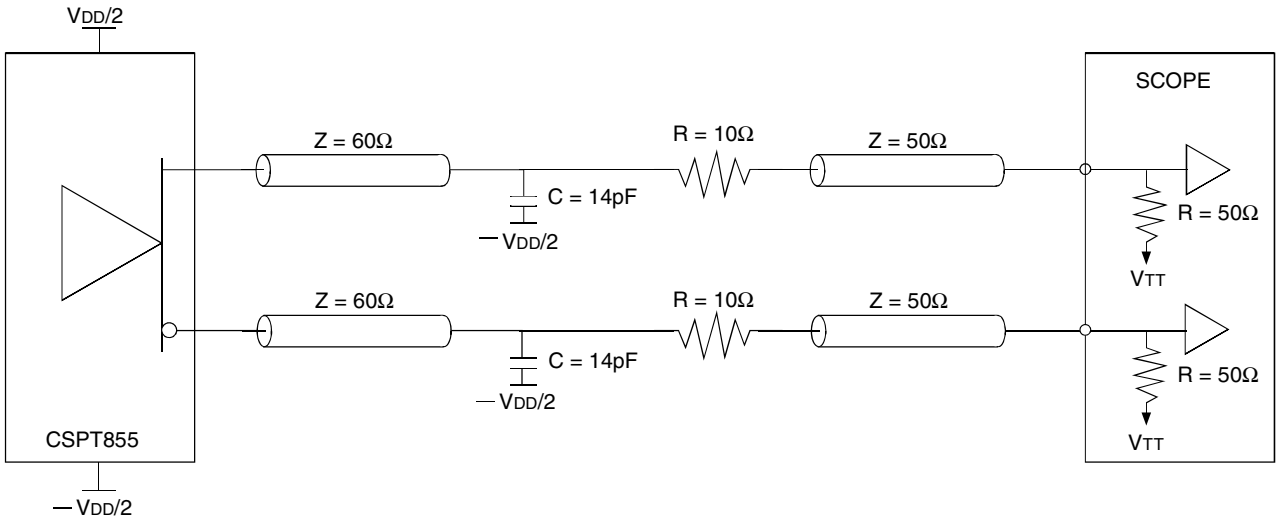
NOTES:
1. Recovery time required when the device goes from power-down mode into bypass mode (test mode with AV_{DD} at GND).
2. Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable. This parameter does not apply for input modulation under SSC application.

SWITCHING CHARACTERISTICS

Symbol	Description		Test Conditions	Min.	Typ.(1)	Max.	Unit
t_{PLH}(2)	LOW to HIGH Level Propagation Delay Time		Test mode, CLK to any output	—	4.5	—	ns
t_{PHL}(2)	HIGH to LOW Level Propagation Delay Time		Test mode, CLK to any output	—	4.5	—	ns
$t_{JIT(PER)}$(3)	Jitter (period), see figure 6		66MHz	–55	—	55	ps
			100/ 133/ 167/ 200 MHz	–35	—	35	
$t_{JIT(CC)}$(3)	Jitter (cycle-to-cycle), see figure 2		66MHz	–60	—	60	ps
			100/ 133/ 167/ 200 MHz	–50	—	50	
$t_{JIT(HPER)}$(3)	Half-Period Jitter, see figure 7		66MHz	–130	—	130	ps
			100MHz	–90	—	90	
			133/ 167/ 200 MHz	–75	—	75	
$t_{SLR(O)}$	Output Clock Slew Rate (single-ended), see figure 8		Load: 120Ω / 14pF	1	—	2	V/ns
			Load: 120Ω / 4pF	1	—	3	
$t_{D(\varnothing)}$(3)	Dynamic Phase Offset (includes jitter) see figure 4	SSC Off	66MHz	–180	—	180	ps
			100/ 133 MHz	–130	—	130	
			167/ 200 MHz	–90	—	90	
		SSC On	66MHz	–230	—	230	
			100/ 133 MHz	–170	—	170	
			167/ 200 MHz	–100	—	100	
$t_{(\varnothing)}$	Static Phase Offset, see figure 3		66MHz	–150	—	150	ps
			100/ 133/ 167 MHz	–100	—	100	
			200MHz	–50	—	50	
$t_{SK(O)}$(4)	Output Skew, see figure 5			—	—	50	ps
t_R, t_F	Output Rise and Fall Times (20% to 80%)		Load: 120Ω / 14pF	650	—	900	ps

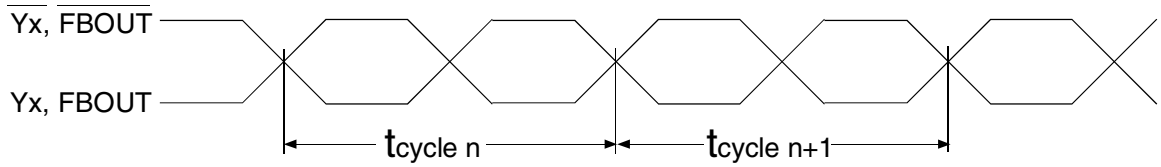
NOTES:
1. All typical values are at respective nominal V_{DDQ}.
2. Refers to transition of non-inverting output.
3. This parameter guaranteed by design but not production tested.
4. All differential output pins are terminated with 120Ω / 14pF.

TEST CIRCUIT AND SWITCHING WAVEFORMS



NOTE:
1. V(TT) = GND

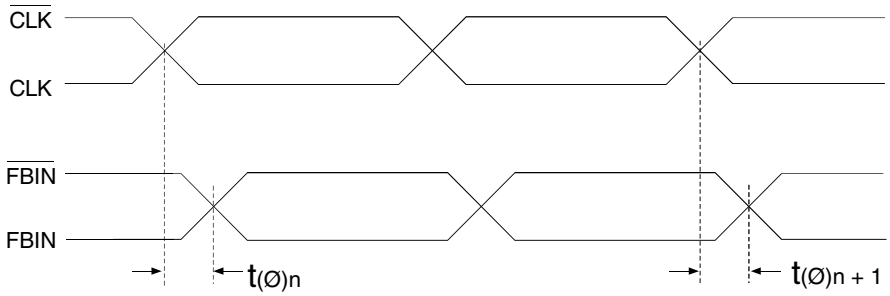
Figure 1. Output Load Test Circuit



$$t_{jit(cc)} = t_{cycle\ n} - t_{cycle\ n+1}$$

Figure 2. Cycle-to-Cycle jitter

TEST CIRCUIT AND SWITCHING WAVEFORMS



$$t_{(Ø)} = \frac{\sum_{1}^{n=N} t_{(Ø)n}}{N}$$

(N is a large number of samples)

Figure 3. Static Phase Offset

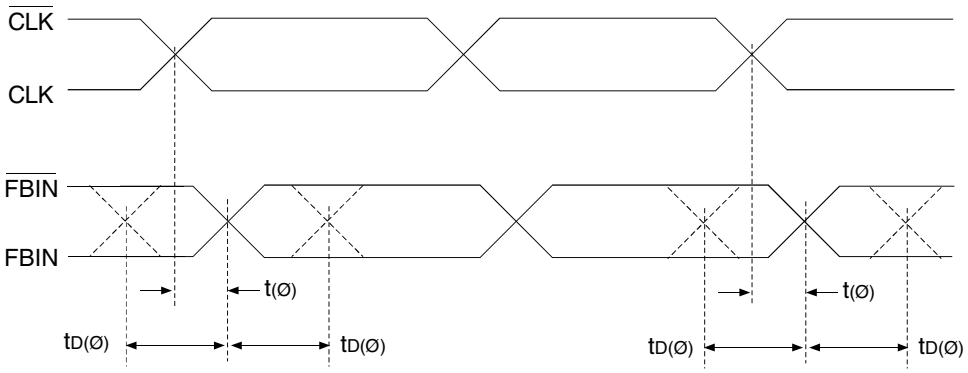


Figure 4. Dynamic Phase Offset

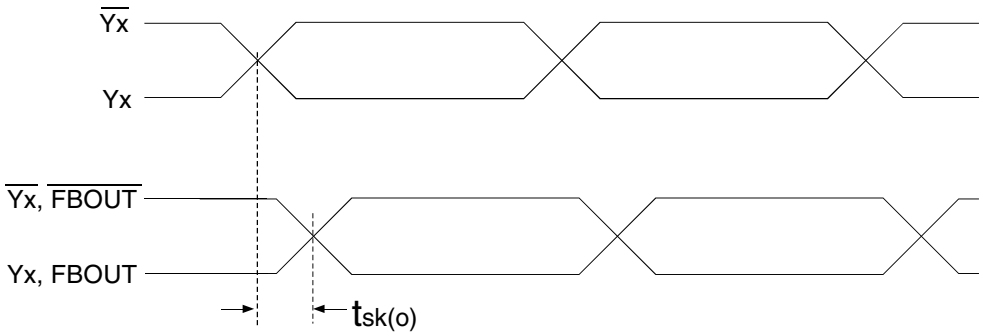
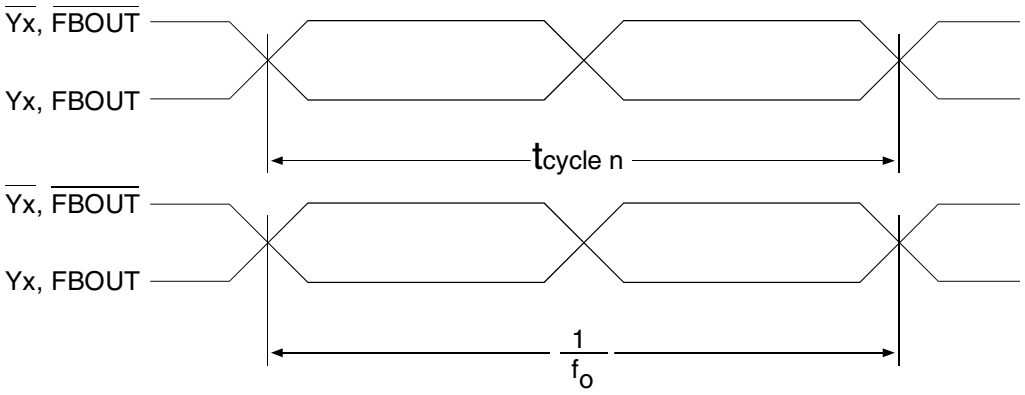


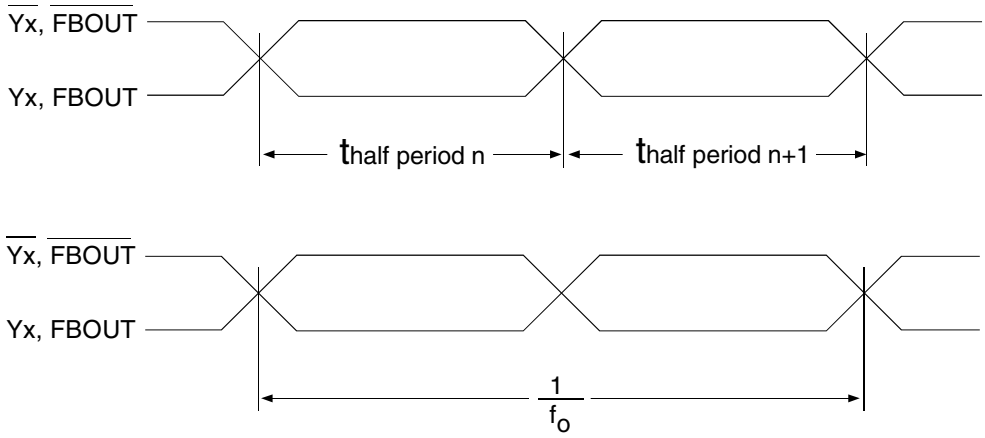
Figure 5. Output Skew

TEST CIRCUIT AND SWITCHING WAVEFORMS



$$t_{jit(per)} = t_{cycle\ n} - \frac{1}{f_o}$$

Figure 6. Period jitter



$$t_{jit(hper)} = t_{half\ period\ n} - \frac{1}{2*f_o}$$

Figure 7. Half-Period jitter

TEST CIRCUIT AND SWITCHING WAVEFORMS

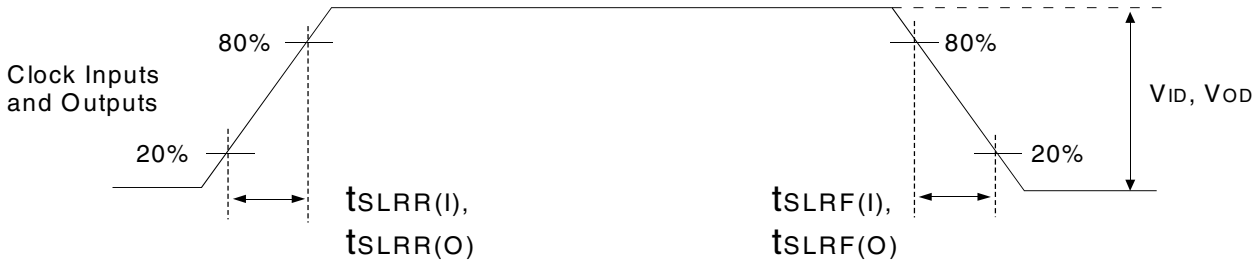
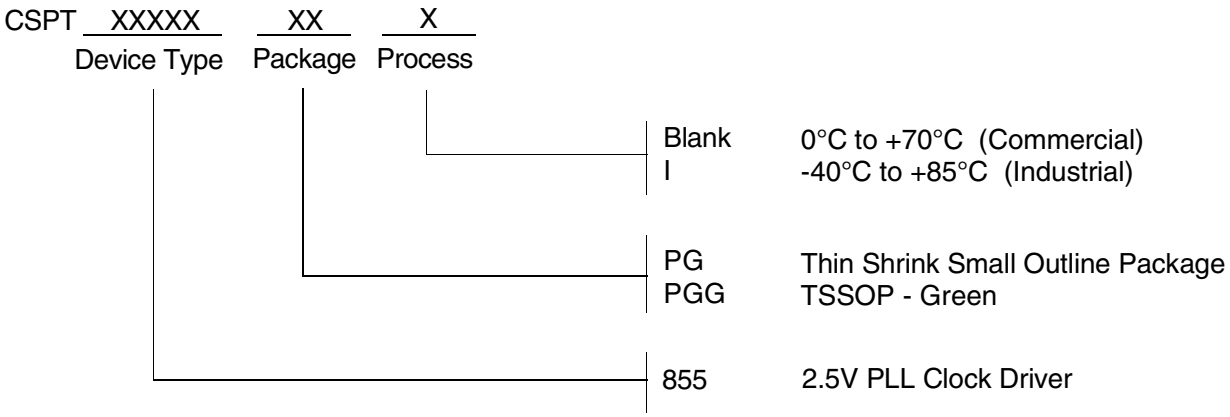


Figure 8. Input and Output Slew Rates

ORDERING INFORMATION



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