2.5V - 2.6V PHASE LOCKED LOOP DIFFERENTIAL 1:10 SDRAM CLOCK DRIVER

IDTCSPT857C

FEATURES:

- **1 to 10 differential clock distribution**
- **Optimized for clock distribution in DDR (Double Data Rate) SDRAM applications**
- **Operating frequency: 60MHz to 220MHz**
- **Very low skew:**
  - *<100ps for PC1600 - PC2700*
  - *<75ps for PC3200*
- **Very low jitter:**
  - *<75ps for PC1600 - PC2700*
  - *<50ps for PC3200*
- **2.5V AV_{DD} and 2.5V V_{DDQ} for PC1600-PC2700**
- **2.6V AV_{DD} and 2.6V V_{DDQ} for PC3200**
- **CMOS control signal input**
- **Test mode enables buffers while disabling PLL**
- **Low current power-down mode**
- **Tolerant of Spread Spectrum input clock**
- **Available in 48-pin TSSOP, 40-pin VFQFPN, and 56-pin VFBGA packages**

APPLICATIONS:

- **Meets or exceeds JEDEC standard JESD 82-1A for registered DDR clock driver**
- **Meets proposed DDR1-400 specification**
- **For all DDR1 speeds: PC1600 (DDR200), PC2100 (DDR266), PC2700 (DDR333), PC3200 (DDR400)**
- **Along with SSTV16857, SSTVF16857, SSTV16859, SSTVM16859, SSTVF16859, DDR1 register, provides complete solution for DDR1 DIMMs**

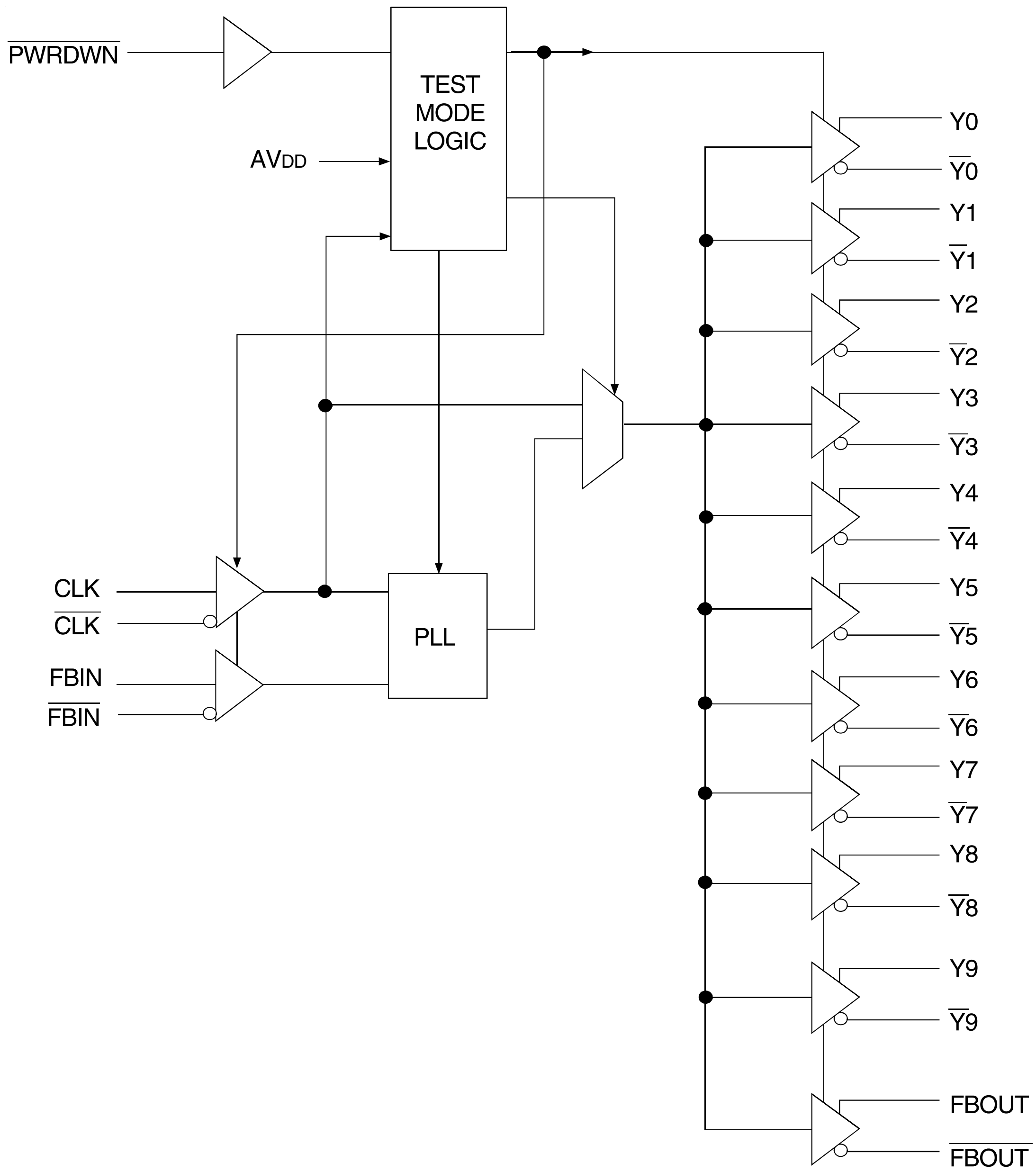
DESCRIPTION:

The CSPT857C is a PLL based clock driver that acts as a zero delay buffer to distribute one differential clock input pair(CLK, $\overline{CLK}$) to 10 differential output pairs ($Y_{[0:9]}$, $\overline{Y}_{[0:9]}$) and one differential pair of feedback clock output (FBOUT, $\overline{FBOUT}$). External feedback pins (FBIN, $\overline{FBIN}$) for synchronization of the outputs to the input reference is provided. A CMOS Enable/Disable pin is available for low power disable. When the input frequency falls below approximately 20MHz, the device will enter power down mode. In this mode, the receivers are disabled, the PLL is turned off, and the output clock drivers are tristated, resulting in a current consumption of less than 200µA.

The CSPT857C requires no external components and has been optimised for very low I/O phase error, skew, and jitter, while maintaining frequency and duty cycle over the operating voltage and temperature range. The CSPT857C, designed for use in both module assemblies and system motherboard based solutions, provides an optimum high-performance clock source.

The CSPT857C is available in Commercial Temperature Range (0°C to +70°C) and Industrial Temperature Range (-40°C to +85°C). See Ordering Information for details.

FUNCTIONAL BLOCK DIAGRAM

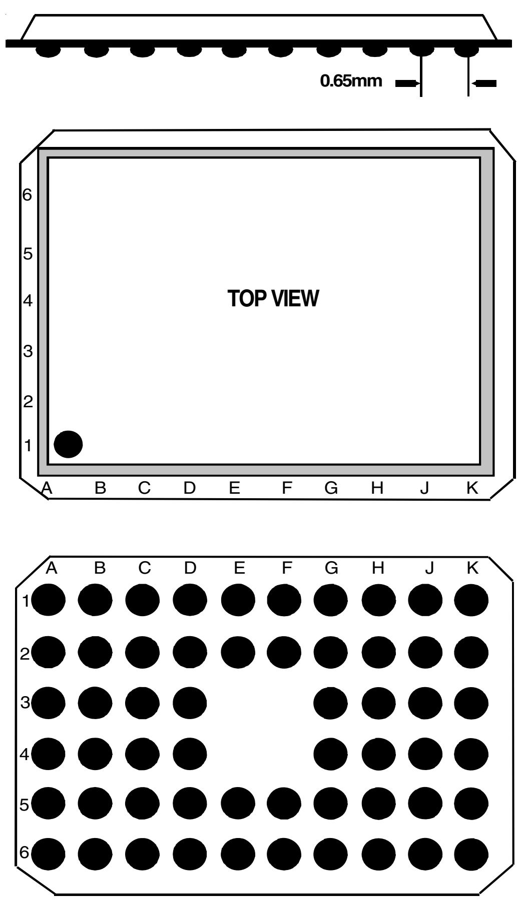


PIN CONFIGURATIONS

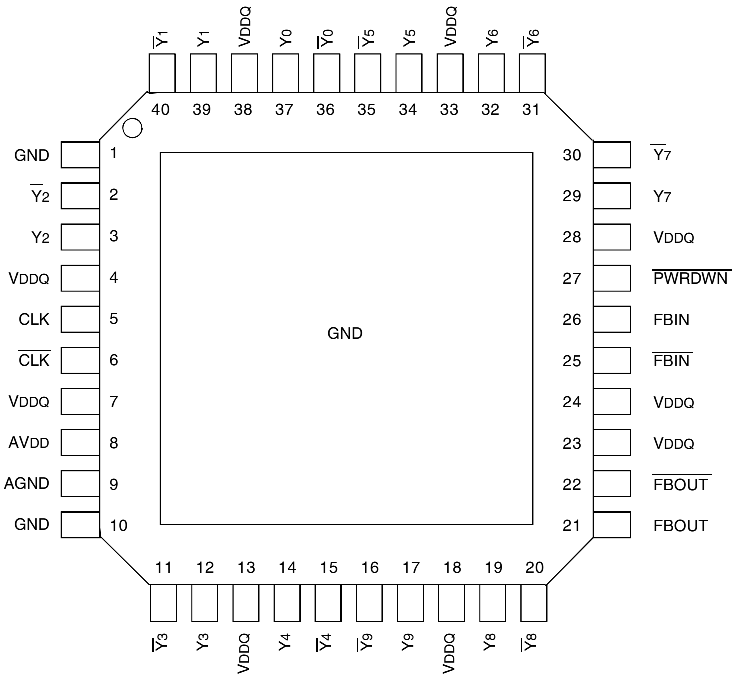
	A	B	C	D	E	F	G	H	J	K
6	Y_5	$\overline{Y_6}$	GND	Y_7	$\overline{\text{PWRDWN}}$	FBIN	V_{DDQ}	FBOUT	$\overline{Y_8}$	Y_9
5	$\overline{Y_5}$	Y_6	GND	$\overline{Y_7}$	V_{DDQ}	$\overline{\text{FBIN}}$	$\overline{\text{FBOUT}}$	GND	Y_8	$\overline{Y_9}$
4	GND	V_{DDQ}	NC	NC			NC	NC	V_{DDQ}	GND
3	GND	V_{DDQ}	NC	NC			NC	NC	V_{DDQ}	GND
2	$\overline{Y_0}$	Y_1	GND	$\overline{Y_2}$	V_{DDQ}	$\overline{\text{CLK}}$	AV_{DD}	GND	Y_3	$\overline{Y_4}$
1	Y_0	$\overline{Y_1}$	GND	Y_2	V_{DDQ}	CLK	V_{DDQ}	AGND	$\overline{Y_3}$	Y_4

VFBGA
TOP VIEW

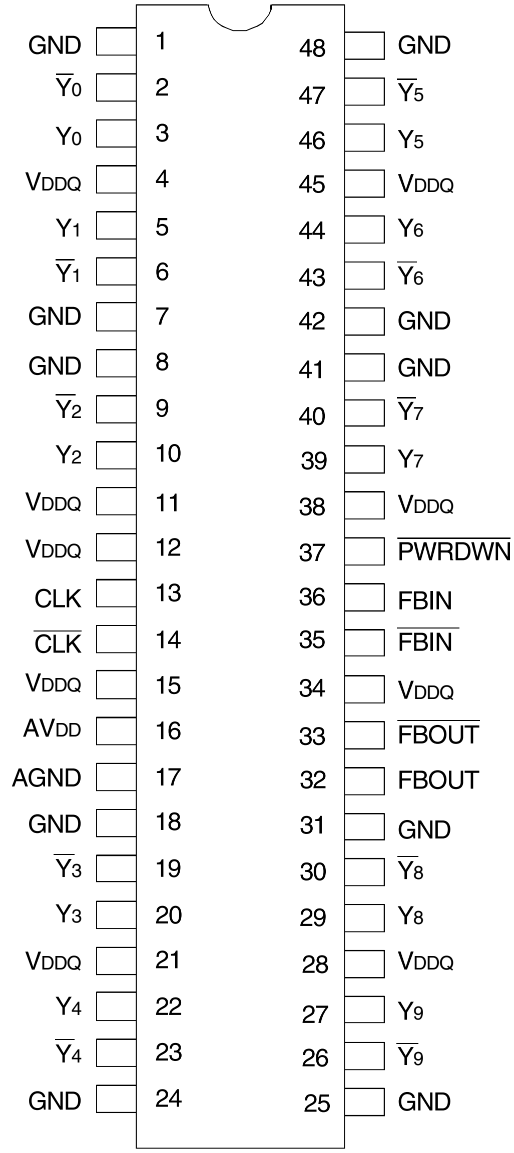
56 BALL VFBGA PACKAGE LAYOUT



PIN CONFIGURATIONS



VFQFPN
TOP VIEW



TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Max	Unit
V_{DDQ}, AV_{DD}	Supply Voltage Range	–0.5 to +3.6	V
V_I(2)	Input Voltage Range	–0.5 to V_{DDQ} + 0.5	V
V_O(2)	Voltage range applied to any output in the high or low state	–0.5 to V_{DDQ} + 0.5	V
I_{IK} (V_I <0)	Input Clamp Current	–50	mA
I_{OK} (V_O <0 or V_O > V_{DDQ})	Output Clamp Current	±50	mA
I_O (V_O =0 to V_{DDQ})	Continuous Output Current	±50	mA
V_{DDQ} or GND	Continuous Current	±100	mA
TSTG	Storage Temperature Range	– 65 to +150	°C

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

CAPACITANCE(1)

Parameter	Description	Min.	Typ.	Max.	Unit
C_{IN}	Input Capacitance V_I = V_{DDQ} or GND	2.5	—	3.5	pF
$C_{I(\Delta)}$	Delta Input Capacitance V_I = V_{DDQ} or GND	-0.25	—	0.25	pF
C_L	Load Capacitance	—	14	—	pF

NOTE:
1. Unused inputs must be held high or low to prevent them from floating.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min.	Typ.	Max.	Unit
AVDD	Supply Voltage		VDDQ – 0.12	VDDQ	2.7	V
VDDQ	I/O Supply Voltage	PC1600-PC2700	2.3	2.5	2.7	V
		PC3200	2.5	2.6	2.7	
TA	Operating Free-Air Temperature		-40	—	+85	°C

PIN DESCRIPTION (TSSOP/TVSOP)

Pin Name	Pin Number	Description
AGND	17	Ground for analog supply
AVDD	16	Analog supply
CLK, $\overline{\text{CLK}}$	13, 14	Differential clock input
$\overline{\text{FBIN}}$, FBIN	35, 36	Feedback differential clock input
FBOUT, $\overline{\text{FBOUT}}$	32, 33	Feedback differential clock output
GND	1, 7, 8, 18, 24, 25, 31, 41, 42, 48	Ground
$\overline{\text{PWRDWN}}$	37	Output enable for Y and $\overline{\text{Y}}$
VDDQ	4, 11, 12, 15, 21, 28, 34, 38, 45	I/O supply
Y[0:9]	3, 5, 10, 20, 22, 27, 29, 39, 44, 46	Buffered output of input clock, CLK
$\overline{\text{Y[0:9]}}$	2, 6, 9, 19, 23, 26, 30, 40, 43, 47	Buffered output of input clock, $\overline{\text{CLK}}$

PIN DESCRIPTION (VFBGA)

Pin Name	Pin Number	Description
AGND	H1	Ground for analog supply
AVDD	G2	Analog supply
CLK, $\overline{\text{CLK}}$	F1, F2	Differential clock input
$\overline{\text{FBIN}}$, FBIN	F5, F6	Feedback differential clock input
FBOUT, $\overline{\text{FBOUT}}$	H6, G5	Feedback differential clock output
GND	A3, A4, C1, C2, C5, C6, H2, H5, K3, K4	Ground
$\overline{\text{PWRDWN}}$	E6	Output enable for Y and $\overline{\text{Y}}$
VDDQ	B3, B4, E1, E2, E5, G1, G6, J3, J4	I/O supply
Y[0:9]	A1, A6, B2, B5, D1, D6, J2, J5, K1, K6	Buffered output of input clock, CLK
$\overline{\text{Y[0:9]}}$	A2, A5, B1, B6, D2, D5, J1, J6, K2, K5	Buffered output of input clock, $\overline{\text{CLK}}$

PIN DESCRIPTION (MLF)

Pin Name	Pin Number	Description
AGND	9	Ground for analog supply
AVDD	8	Analog supply
CLK, $\overline{\text{CLK}}$	5, 6	Differential clock input
$\overline{\text{FBIN}}$, FBIN	25, 26	Feedback differential clock input
FBOUT, $\overline{\text{FBOUT}}$	21, 22	Feedback differential clock output
GND	1, 10	Ground
$\overline{\text{PWRDWN}}$	27	Output enable for Y and $\overline{\text{Y}}$
VDDQ	4, 7, 13, 18, 23, 24, 28, 33, 38	I/O supply
Y[0:9]	3, 12, 14, 17, 19, 29, 32, 34, 37, 39	Buffered output of input clock, CLK
$\overline{\text{Y[0:9]}}$	2, 11, 15, 16, 20, 30, 31, 35, 36, 40	Buffered output of input clock, $\overline{\text{CLK}}$

FUNCTION TABLE[1]

INPUTS				OUTPUTS				
AV_{DD}	$\overline{\text{PWRDWN}}$	CLK	$\overline{\text{CLK}}$	Y	$\overline{\text{Y}}$	FBOUT	$\overline{\text{FBOUT}}$	PLL
GND	H	L	H	L	H	L	H	Bypassed/OFF
GND	H	H	L	H	L	H	L	Bypassed/OFF
X	L	L	H	Z	Z	Z	Z	OFF
X	L	H	L	Z	Z	Z	Z	OFF
Nominal[2]	H	L	H	L	H	L	H	ON
Nominal[2]	H	H	L	H	L	H	L	ON
Nominal[2,3]	X	<20MHz	<20MHz	Z	Z	Z	Z	OFF

NOTES:

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   Z = High-Impedance OFF-State
   X = Don't Care
2. AV_{DD} nominal is 2.5V for PC1600, PC2100, and PC2700. AV_{DD} nominal is 2.6V for PC3200.
3. Additional feature that senses when the clock input is less than approximately 20MHz and places the part in sleep mode. Reciever inputs and PLL are turned off and outputs = tristate.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE FOR PC1600 - PC2700

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C; Industrial: T_A = -40°C to +85°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IK}	Input Clamp Voltage (All Inputs)	V_{DDQ} = 2.3V, I_I = -18mA	—	—	– 1.2	V
$V_{IL\,(dc)}$	Static Input LOW Voltage	$\overline{\text{PWRDWN}}$	– 0.3	—	0.7	V
$V_{IH\,(dc)}$	Static Input HIGH Voltage	$\overline{\text{PWRDWN}}$	1.7	—	V_{DDQ} + 0.3	
$V_{IL\,(ac)}$	Dynamic Input LOW Voltage	CLK, $\overline{\text{CLK}}$, FBIN, $\overline{\text{FBIN}}$	—	—	0.7	V
$V_{IH\,(ac)}$	Dynamic Input HIGH Voltage	CLK, $\overline{\text{CLK}}$, FBIN, $\overline{\text{FBIN}}$	1.7		V_{DDQ}	
V_{OL}	Output LOW Voltage	AV_{DD}/V_{DDQ} = Min., I_{OL} = 100µA	—		0.1	V
		AV_{DD}/V_{DDQ} = Min., I_{OL} = 12mA	—		0.6	
V_{OH}	Output HIGH Voltage	AV_{DD}/V_{DDQ} = Min., I_{OH} = -100µA	V_{DDQ} – 0.1			V
		AV_{DD}/V_{DDQ} = Min., I_{OH} = -12mA	1.7			
V_{IX}	Input Differential Cross Voltage		V_{DDQ}/2 – 0.2		V_{DDQ}/2 + 0.2	V
$V_{ID(DC)}$[1]	DC Input Differential Voltage		0.36		V_{DDQ} + 0.6	V
$V_{ID(AC)}$[1]	AC Input Differential Voltage		0.7		V_{DDQ} + 0.6	V
I_{IN}	Input Current	V_{DDQ} = 2.7V, V_I = 0V to 2.7V			±10	µA
I_{DDPD}	Power-Down Current on V_{DDQ} and AV_{DD}	AV_{DD}/V_{DDQ} = Max., CLK = 0MHz or $\overline{\text{PWRDWN}}$ = L	—	100	200	µA
I_{DDQ}	Dynamic Power Supply Current on V_{DDQ}	AV_{DD}/V_{DDQ} = Max., CLK = 200MHz, 120Ω/14pF	—	320	360	mA
		AV_{DD}/V_{DDQ} = Max., CLK = 170MHz, 120Ω/14pF	—	250	300	
I_{ADD}	Dynamic Power Supply Current on AV_{DD}	AV_{DD}/V_{DDQ} = Max., CLK = 170MHz	—		12	mA

NOTE:

1. V_{ID} is the magnitude of the difference between the input level on CLK and the input level on $\overline{\text{CLK}}$.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE FOR PC3200

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C; Industrial: T_A = -40°C to +85°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IK}	Input Clamp Voltage (All Inputs)	V_{DDQ} = 2.5V, I_I = -18mA	—	—	– 1.2	V
$V_{IL(dc)}$	Static Input LOW Voltage	$\overline{\text{PWRDWN}}$	– 0.3	—	0.7	V
$V_{IH(dc)}$	Static Input HIGH Voltage	$\overline{\text{PWRDWN}}$	1.7	—	V_{DDQ} + 0.3	
$V_{IL(ac)}$	Dynamic Input LOW Voltage	CLK, $\overline{\text{CLK}}$, FBIN, $\overline{\text{FBIN}}$	—	—	0.7	V
$V_{IH(ac)}$	Dynamic Input HIGH Voltage	CLK, $\overline{\text{CLK}}$, FBIN, $\overline{\text{FBIN}}$	1.7		V_{DDQ}	
V_{OL}	Output LOW Voltage	AV_{DD}/V_{DDQ} = Min., I_{OL} = 100µA	—		0.1	V
		AV_{DD}/V_{DDQ} = Min., I_{OL} = 12mA	—		0.6	
V_{OH}	Output HIGH Voltage	AV_{DD}/V_{DDQ} = Min., I_{OH} = -100µA	V_{DDQ} – 0.1			V
		AV_{DD}/V_{DDQ} = Min., I_{OH} = -12mA	1.7			
V_{IX}	Input Differential Cross Voltage		V_{DDQ}/2 – 0.2		V_{DDQ}/2 + 0.2	V
$V_{ID(DC)}$(1)	DC Input Differential Voltage		0.36		V_{DDQ} + 0.6	V
$V_{ID(AC)}$(1)	AC Input Differential Voltage		0.7		V_{DDQ} + 0.6	V
I_{IN}	Input Current	V_{DDQ} = 2.7V, V_I = 0V to 2.7V			±10	µA
I_{DDPD}	Power-Down Current on V_{DDQ} and AV_{DD}	AV_{DD}/V_{DDQ} = Max., CLK = 0MHz or $\overline{\text{PWRDWN}}$ = L	—	100	200	µA
I_{DDQ}	Dynamic Power Supply Current on V_{DDQ}	AV_{DD}/V_{DDQ} = Max., CLK = 200MHz, 120Ω/14pF	—	320	360	mA
		AV_{DD}/V_{DDQ} = Max., CLK = 200MHz, 120Ω/14pF	—	250	300	
I_{ADD}	Dynamic Power Supply Current on AV_{DD}	AV_{DD}/V_{DDQ} = Max., CLK = 200MHz	—		12	mA

NOTE:
1. V_{ID} is the magnitude of the difference between the input level on CLK and the input level on $\overline{\text{CLK}}$.

TIMING REQUIREMENTS FOR PC1600 - PC2700

Symbol	Parameter	Min.	Max.	Unit
f_{CLK}	Operating Clock Frequency(1,2)	60	200	MHz
	Application Clock Frequency(1,3)	60	200	MHz
t_{DC}	Input Clock Duty Cycle	40	60	%
t_L	Stabilization Time(4)	—	100	µs

NOTES:
1. The PLL will track a spread spectrum clock input.
2. Operating clock frequency is the range over which the PLL will lock, but may not meet all timing specifications.
3. Application clock frequency is the range over which timing specifications apply.
4. Stabilization time is the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal after power up.

TIMING REQUIREMENTS FOR PC3200

Symbol	Parameter	Min.	Max.	Unit
f_{CLK}	Operating Clock Frequency(1,2)	60	220	MHz
	Application Clock Frequency(1,3)	60	220	MHz
t_{DC}	Input Clock Duty Cycle	40	60	%
t_L	Stabilization Time(4)	—	100	µs

NOTES:
1. The PLL will track a spread spectrum clock input.
2. Operating clock frequency is the range over which the PLL will lock, but may not meet all timing specifications.
3. Application clock frequency is the range over which timing specifications apply.
4. Stabilization time is the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal after power up.

SWITCHING CHARACTERISTICS FOR PC1600 - PC2700

Symbol	Description	Test Conditions	Min.	Typ.[1]	Max.	Unit
t_{PLH}[1]	LOW to HIGH Level Propagation Delay Time	Test mode, CLK to any output		4.5		ns
t_{PHL}[1]	HIGH to LOW Level Propagation Delay Time	Test mode, CLK to any output		4.5		ns
$t_{JIT(PER)}$	Jitter (period), see figure 6	66MHz	–90		90	ps
		100/ 133/ 167/ 200 MHz	–75		75	
$t_{JIT(CC)}$	Jitter (cycle-to-cycle), see figure 3	66MHz	–180		180	ps
		100/ 133/ 167/ 200 MHz	–75		75	
$t_{JIT(HPER)}$	Half-Period Jitter, see figure 7	66MHz	–160		160	ps
		100/ 133/ 167/ 200 MHz	–100		100	
$t_{SLR(O)}$	Output Clock Slew Rate (Single-Ended)	100/ 133/ 167/ 200 MHz (20% to 80%)	1		2.5	V/ns
$t_{SLR(I)}$	Input Clock Slew Rate		1		4	V/ns
$t_{(\varnothing)}$	Static Phase Offset, see figure 4[2,3]	66/ 100/ 133/ 167/ 200 MHz	–50		50	ps
$t_{SK(O)}$	Output Skew, see figure 5				75	ps
t_R, t_F	Output Rise and Fall Times (20% to 80%)	Load: 120Ω / 14pF	650		900	ps
V_{OX}[5]	Output Differential Voltage	Differential outputs are terminated with 120Ω	$V_{DDQ}/2 - 0.15$		$V_{DDQ}/2 + 0.15$	V
The PLL on the CSPT857 will meet all the above test parameters while supporting SSC synthesizers[4] with the following parameters:						
SSC	Modulation Frequency	—	30	—	50	KHz
SSC	Clock Input Frequency Deviation	—	0	—	-0.5	%
f_{3dB}	PLL Loop Bandwidth	—	—	5	—	MHz

NOTES:
1. Refers to transition of non-inverting output.
2. Static phase offset does not include jitter.
3. $t(\phi)$ is measured with input clock slew rate $t_{SLR(I)}$ = 2V/ns and an input differential voltage V_{ID} of 1.75V.
4. The SSC requirements meet the Intel PC100 SDRAM Registered DIMM specification.
5. V_{OX} is specified at the SDRAM clock input or test load.

SWITCHING CHARACTERISTICS FOR PC3200

Symbol	Description	Test Conditions	Min.	Typ.[1]	Max.	Unit
t_{PLH}[1]	LOW to HIGH Level Propagation Delay Time	Test mode, CLK to any output		4.5		ns
t_{PHL}[1]	HIGH to LOW Level Propagation Delay Time	Test mode, CLK to any output		4.5		ns
$t_{JIT(PER)}$	Jitter (period), see figure 6	66MHz	–90		90	ps
		200 MHz	–50		50	
$t_{JIT(CC)}$	Jitter (cycle-to-cycle), see figure 3	66MHz	–180		180	ps
		200 MHz	–75		75	
$t_{JIT(HPER)}$	Half-Period Jitter, see figure 7	66MHz	–160		160	ps
		200 MHz	–75		75	
$t_{SLR(O)}$	Output Clock Slew Rate (Single-Ended)	200 MHz (20% to 80%)	1		2.5	V/ns
$t_{SLR(I)}$	Input Clock Slew Rate		1		4	V/ns
$t(\varnothing)$	Static Phase Offset, see figure 4[2,3]	200 MHz	–50		50	ps
$t_{SK(O)}$	Output Skew, see figure 5				75	ps
t_R, t_F	Output Rise and Fall Times (20% to 80%)	Load: 120Ω / 14pF	650		900	ps
V_{OX}[5]	Output Differential Voltage	Differential outputs are terminated with 120Ω	$V_{DDQ}/2 - 0.15$		$V_{DDQ}/2 + 0.15$	V
The PLL on the CSPT857 will meet all the above test parameters while supporting SSC synthesizers[4] with the following parameters:						
SSC	Modulation Frequency	—	30	—	50	KHz
SSC	Clock Input Frequency Deviation	—	0	—	-0.5	%
f_{3dB}	PLL Loop Bandwidth	—	—	5	—	MHz

NOTES:
1. Refers to transition of non-inverting output.
2. Static phase offset does not include jitter.
3. $t(\phi)$ is measured with input clock slew rate $t_{SLR(I)}$ = 2V/ns and an input differential voltage V_{ID} of 1.75V.
4. The SSC requirements meet the Intel PC100 SDRAM Registered DIMM specification.
5. V_{OX} is specified at the SDRAM clock input or test load.

TEST CIRCUIT AND SWITCHING WAVEFORMS

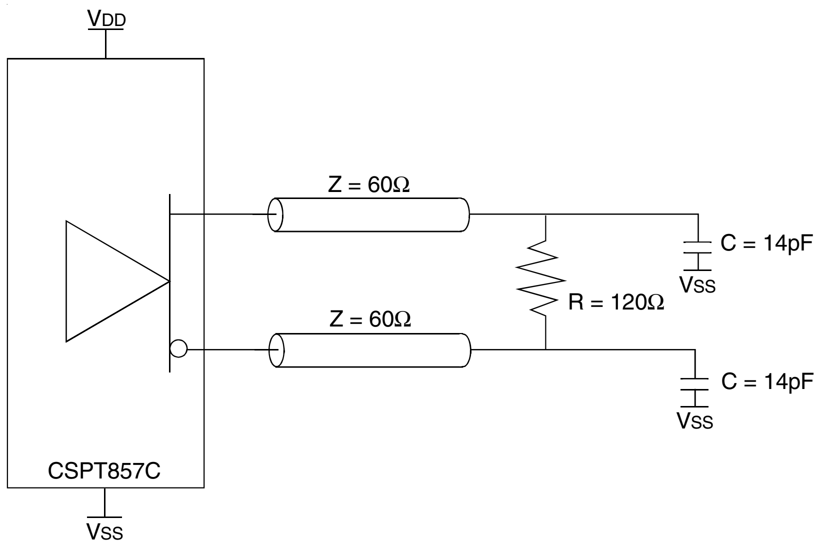


Figure 1. Output Load

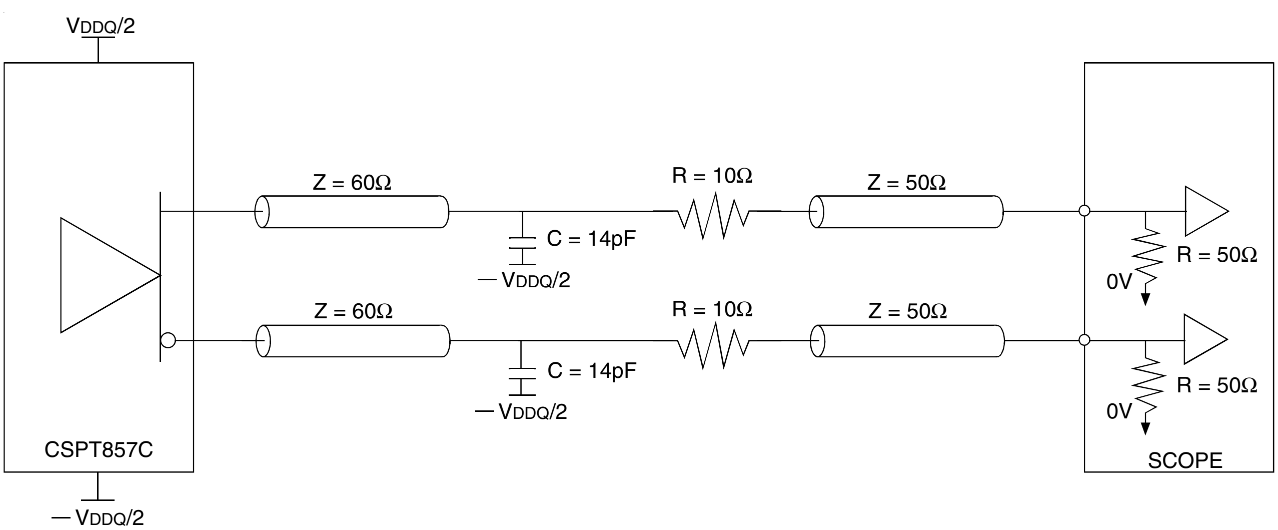
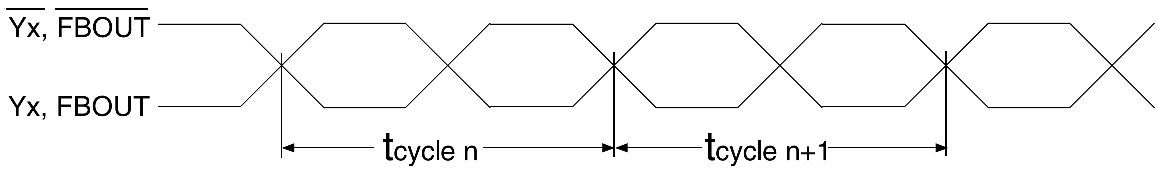


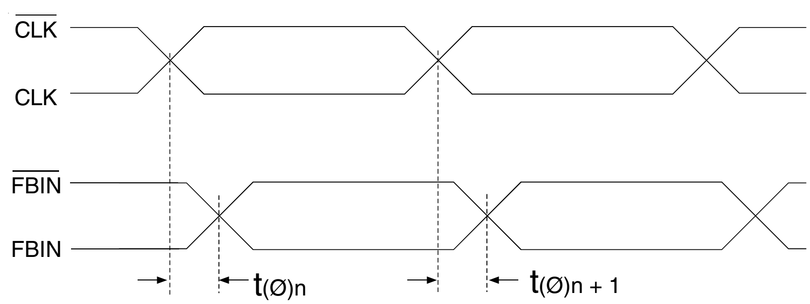
Figure 2. Output Load Test Circuit

TEST CIRCUIT AND SWITCHING WAVEFORMS



$$t_{jit(cc)} = t_{cycle\ n} - t_{cycle\ n+1}$$

Figure 3. Cycle-to-Cycle jitter



$$t_{(\varnothing)} = \frac{\sum_{1}^{n=N} t_{(\varnothing)n}}{N}$$

(N is a large number of samples)

Figure 4. Static Phase Offset

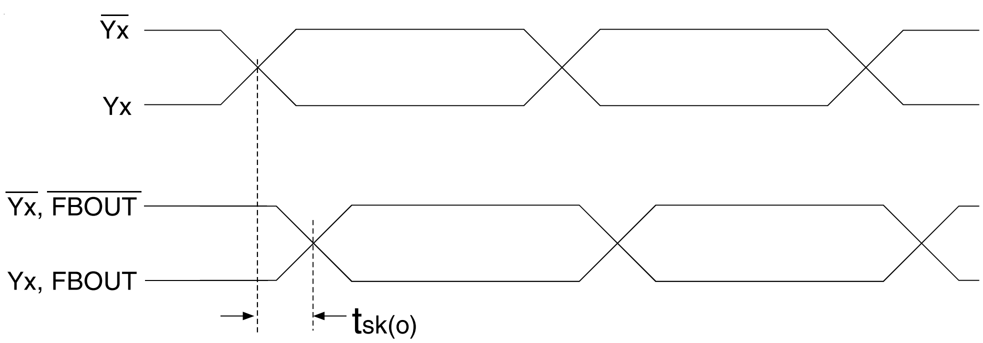
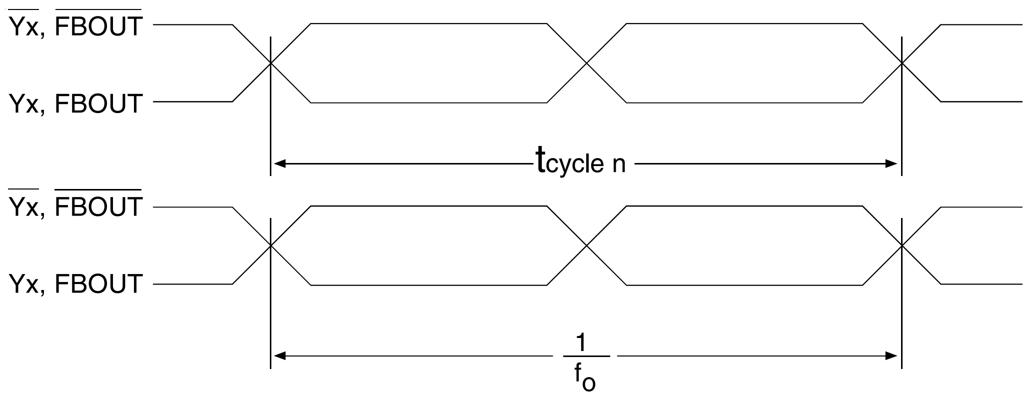


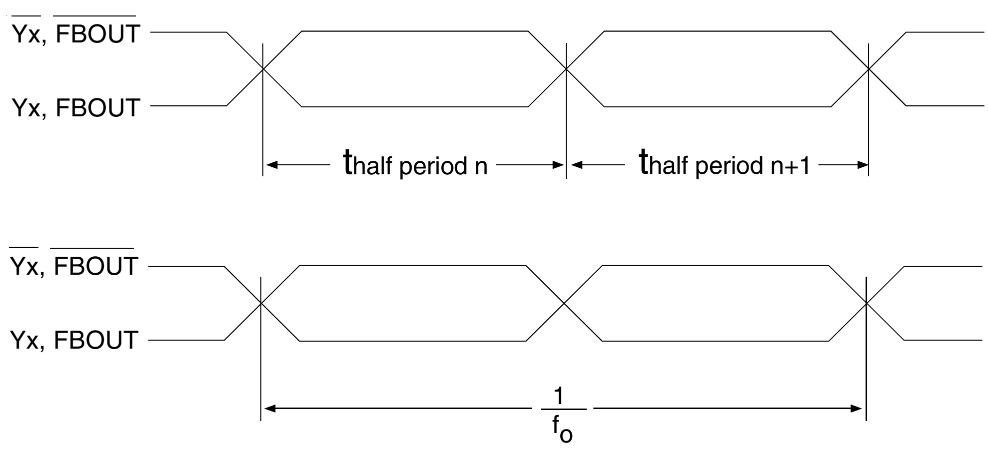
Figure 5. Output Skew

TEST CIRCUIT AND SWITCHING WAVEFORMS



$$t_{jit(per)} = t_{cycle\ n} - \frac{1}{f_o}$$

Figure 6. Period jitter



$$t_{jit(hper)} = t_{half\ period\ n} - \frac{1}{2*f_o}$$

Figure 7. Half-Period jitter

TEST CIRCUIT AND SWITCHING WAVEFORMS

Figure 8. Input and Output Slew Rates

APPLICATION INFORMATION

Clock Structure	# of SDRAM Loads per Clock	Clock Loading on the PLL outputs (pF)	
		Min.	Max.
#1	2	4	7
#2	4	8	14

APPLICATION INFORMATION

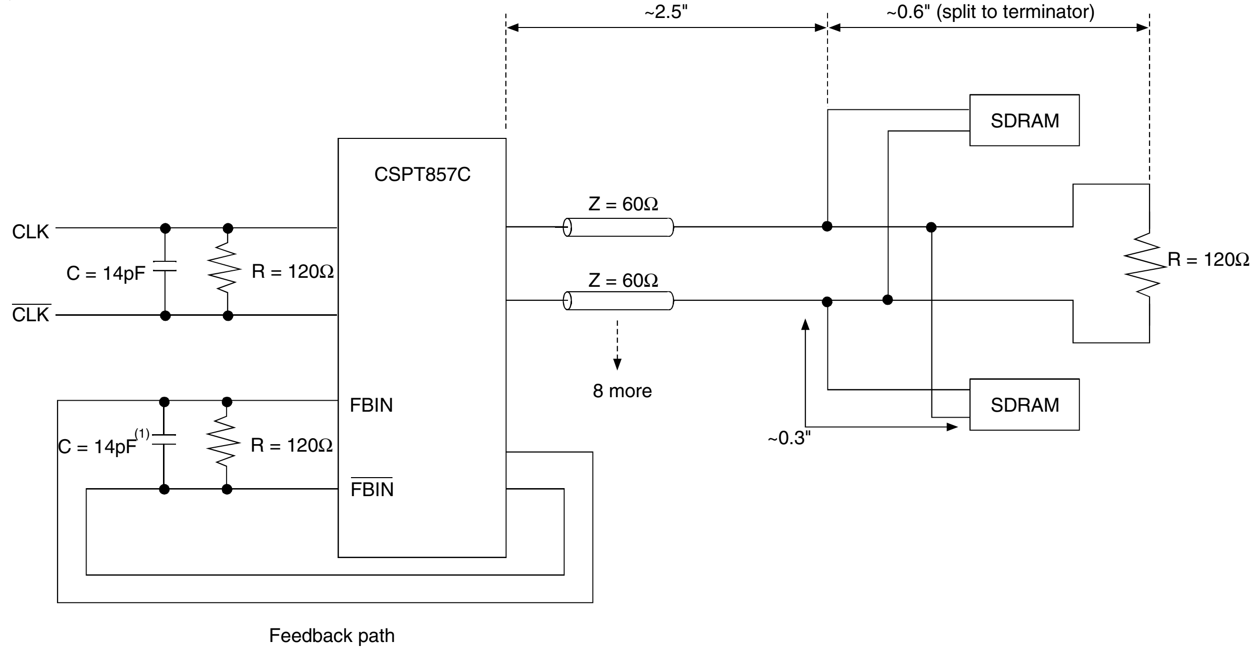


Figure 9. Clock Structure 1

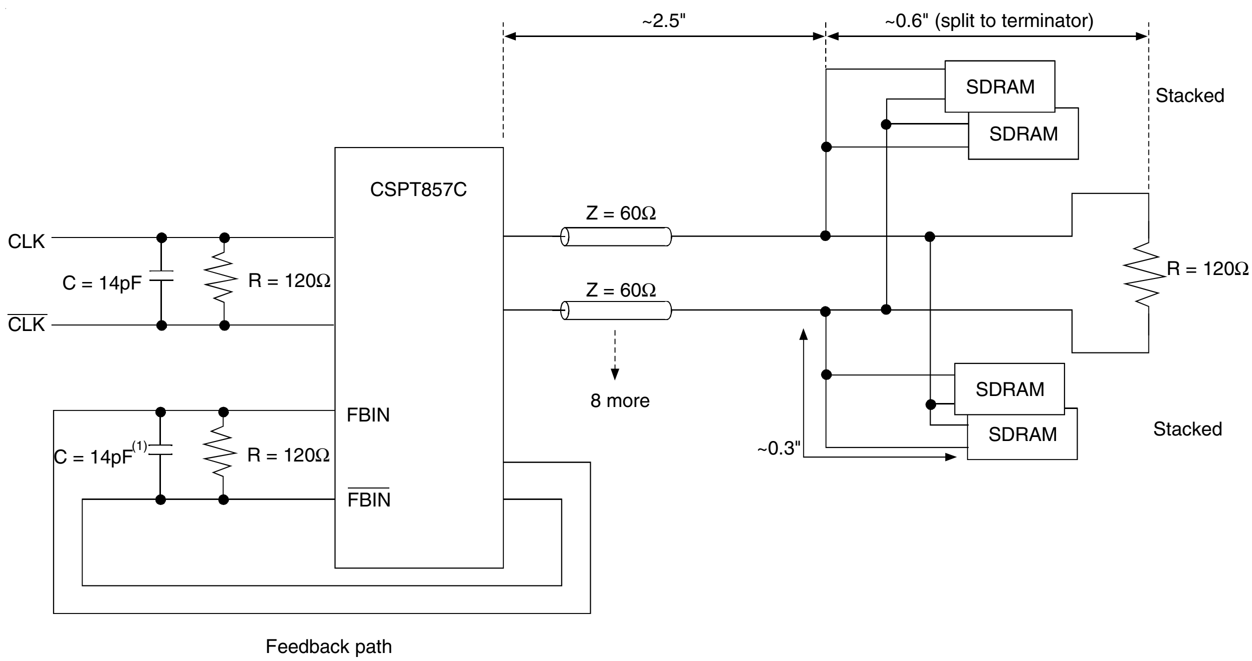


Figure 10. Clock Structure 2

NOTE:
1. Memory module vendors may need to adjust the feedback capacitive load in order to meet DDR SDRAM registered DIMM timing requirements.

ORDERING INFORMATION

CSPT XXXXX XX X

Process	Blank	0°C to +70°C (Commercial)
	I	-40°C to +85°C (Industrial)
Package	PA	Thin Shrink Small Outline Package
	PAG	TSSOP - Green
	BV	Very Fine Pitch Ball Grid Array
	BVG	VFBGA - Green
	NL	Thermally-Enhanced Plastic Very Fine Pitch Flat No Lead Package
	NLG	VFQFPN - Green
Device Type	857C	2.5V - 2.6V PLL Differential 1:10 SDRAM Clock Driver

IMPORTANT NOTICE AND DISCLAIMER

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