1.8V PHASE LOCKED LOOP DIFFERENTIAL 1:10 SDRAM CLOCK DRIVER

IDTCSPUA877

FEATURES:

- 1 to 10 differential clock distribution
- Optimized for clock distribution in DDR2 (Double Data Rate) SDRAM applications
- Operating frequency: 125MHz to 410MHz
- Stabilization time: <6us
- Very low skew: ≤40ps
- Very low jitter: ≤40ps
- 1.8V AV_{DD} and 1.8V V_{DDQ}
- CMOS control signal input
- Test mode enables buffers while disabling PLL
- Low current power-down mode
- Tolerant of Spread Spectrum input clock
- Available in VFBGA package

APPLICATIONS:

- Meets or exceeds JEDEC standard CUA877 for registered DDR2 clock driver
- Along with SSTUA32864/66, DDR2 register, provides complete solution for DDR2 DIMMs

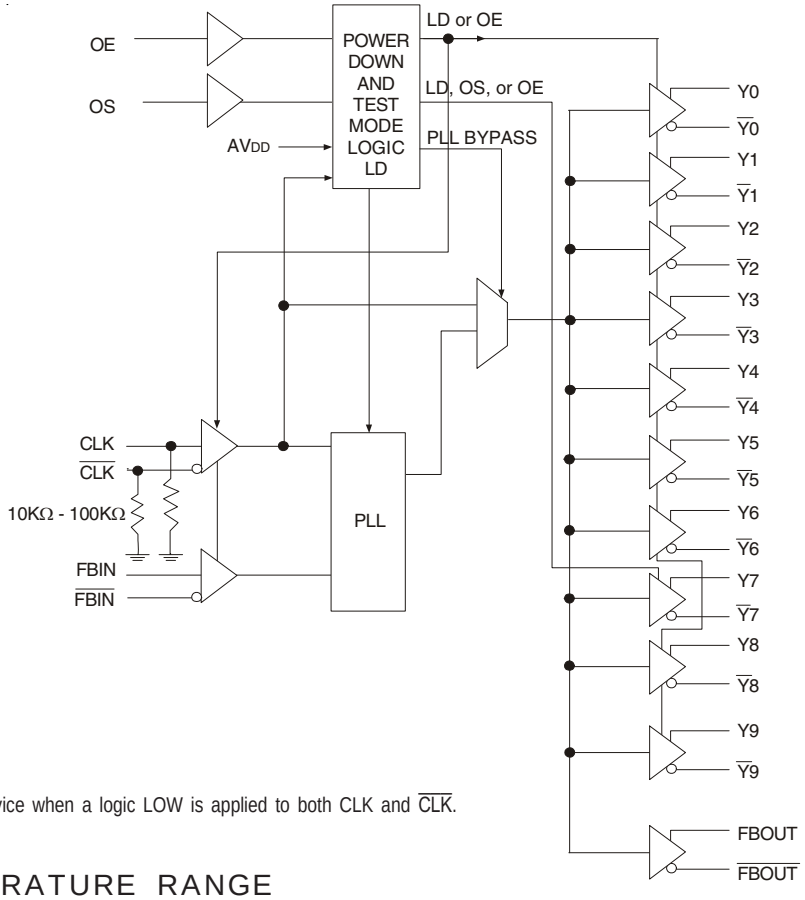
DESCRIPTION:

The CSPUA877 is a PLL based clock driver that acts as a zero delay buffer to distribute one differential clock input pair(CLK, $\overline{CLK}$) to 10 differential output pairs ($\overline{Y}$ [0:9], Y [0:9]) and one differential pair of feedback clock output (FBOUT, $\overline{FBOUT}$). External feedback pins (FBIN, $\overline{FBIN}$) for synchronization of the outputs to the input reference is provided. OE, OS, and A_{VDD} control the power-down and test mode logic. When A_{VDD} is grounded, the PLL is turned off and bypassed for test mode purposes. When the differential clock inputs (CLK, $\overline{CLK}$) are both at logic low, this device will enter a low power-down mode. In this mode, the receivers are disabled, the PLL is turned off, and the output clock drivers are disabled, resulting in a clock driver current consumption of less than 500µA.

The CSPUA877 requires no external components and has been optimised for very low phase error, skew, and jitter, while maintaining frequency and duty cycle over the operating voltage and temperature range. The CSPUA877 , designed for use in both module assemblies and system motherboard based solutions, provides an optimum high-performance clock source.

The CSPUA877 is available in Commercial Temperature Range (0°C to +70°C). See Ordering Information for details.

FUNCTIONAL BLOCK DIAGRAM



NOTE:
The Logic Detect (LD) powers down the device when a logic LOW is applied to both CLK and $\overline{CLK}$.

COMMERCIAL TEMPERATURE RANGE

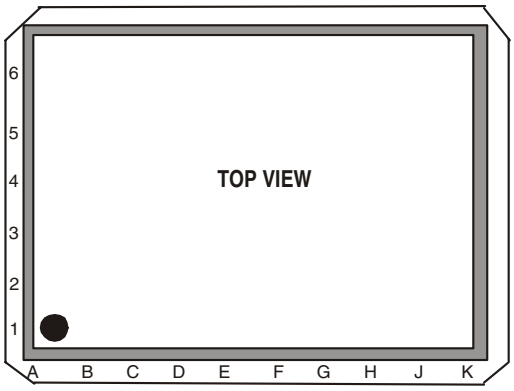
OCTOBER 2006

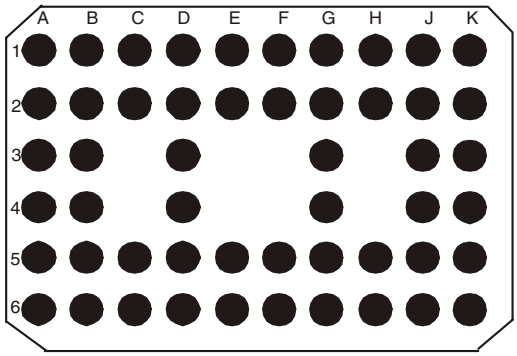
PIN CONFIGURATION

	A	B	C	D	E	F	G	H	J	K
6	Y_6	$\overline{Y_6}$	$\overline{Y_7}$	Y_7	FBIN	$\overline{FBIN}$	$\overline{FBOUT}$	FBOUT	Y_8	$\overline{Y_8}$
5	Y_5	GND	GND	OS	V_{DDQ}	OE	V_{DDQ}	GND	GND	$\overline{Y_9}$
4	$\overline{Y_5}$	GND	NB	V_{DDQ}	NB	NB	V_{DDQ}	NB	GND	Y_9
3	$\overline{Y_0}$	GND	NB	V_{DDQ}	NB	NB	V_{DDQ}	NB	GND	Y_4
2	Y_0	GND	GND	V_{DDQ}	V_{DDQ}	V_{DDQ}	V_{DDQ}	GND	GND	$\overline{Y_4}$
1	Y_1	$\overline{Y_1}$	$\overline{Y_2}$	Y_2	CLK	$\overline{CLK}$	AGND	AV_{DD}	Y_3	$\overline{Y_3}$

VFBGA
TOP VIEW

52 BALL VFBGA PACKAGE LAYOUT





ABSOLUTE MAXIMUM RATINGS(1,2)

Symbol	Rating	Max	Unit
V_{DDQ}, AV_{DD}	Supply Voltage Range	–0.5 to +2.5	V
V_I(3)	Input Voltage Range	–0.5 to V_{DDQ} + 0.5	V
V_O(3)	Voltage range applied to any output in the high or low state	–0.5 to V_{DDQ} + 0.5	V
I_{IK} (V_I <0)	Input clamp current	±50	mA
I_{OK} (V_O <0 or V_O > V_{DDQ})	Output Clamp Current	±50	mA
I_O (V_O =0 to V_{DDQ})	Continuous Output Current	±50	mA
V_{DDQ} or GND	Continuous Current	±100	mA
TSTG	Storage Temperature Range	– 65 to +150	°C

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
3. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed. This value is limited to 2.5V max.

CAPACITANCE(1)

Parameter	Description	Min.	Typ.	Max.	Unit
C_{IN}	Input Capacitance V_I = V_{DDQ} or GND	2	—	3	pF
$C_{I\Delta}$	Delta Input Capacitance CLK, $\overline{CLK}$, FBIN, $\overline{FBIN}$			0.25	pF
C_L	Load Capacitance	—	10	—	pF

NOTE:
1. Unused inputs must be held high or low to prevent them from floating.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
AV_{DD}(1)	Supply Voltage		V_{DDQ}		V
V_{DDQ}	I/O Supply Voltage	1.7	1.8	1.9	V
T_A	Operating Free-Air Temperature	0	—	+70	°C

NOTE:
1. The PLL is turned off and bypassed for test purposes when AV_{DD} is grounded. During this test mode, V_{DDQ} remains within the recommended operating conditions and no timing parameters are guaranteed.

PIN DESCRIPTION (VFBGA)

Pin Name	Pin Number	Description
AGND	G1	Ground for 1.8V analog supply
AV_{DD}	H1	1.8V analog supply
CLK, $\overline{CLK}$	E1, F1	Differential clock input with a 10KΩ to 100KΩ pulldown resistor
FBIN, $\overline{FBIN}$	E6, F6	Feedback differential clock input
$\overline{FBOUT}$, FBOUT	G6, H6	Feedback differential clock output
GND	B2 - B5, C2, C5, H2, H5, J2 - J5	Ground
V_{DDQ}	D2 - D4, E2, E5, F2, G2 - G5	1.8V supply
OE	F5	Output Enable
OS	D5	Output Select (tied to GND or V_{DDQ})
$\overline{Y_{[0:9]}}$	A3, A4, B1, B6, C1, C6, K1, K2, K5, K6	Buffered output of input clock, $\overline{CLK}$
$Y_{[0:9]}$	A1, A2, A5, A6, D1, D6, J1, J6, K3, K4	Buffered output of input clock, CLK
NB		No Ball

FUNCTION TABLE(1,2)

INPUTS					OUTPUTS				
AV_{DD}	OE	OS	CLK	$\overline{CLK}$	Y	$\overline{Y}$	FBOUT	$\overline{FBOUT}$	PLL
GND	H	X	L	H	L	H	L	H	OFF
GND	H	X	H	L	H	L	H	L	OFF
GND	L	H	L	H	L(z)	L(z)	L	H	OFF
GND	L	L	H	L	L(z) Y_7 Active	L(z) $\overline{Y_7}$ Active	H	L	OFF
1.8V (nom)	L	H	L	H	L(z)	L(z)	L	H	ON
1.8V (nom)	L	L	H	L	L(z) Y_7 Active	L(z) $\overline{Y_7}$ Active	H	L	ON
1.8V (nom)	H	X	L	H	L	H	L	H	ON
1.8V (nom)	H	X	H	L	H	L	H	L	ON
1.8V (nom)	X	X	L(3)	L(3)	L(z)	L(z)	L(z)	L(z)	OFF
X	X	X	H	H	Reserved				

NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
2. L(z) means the outputs are disabled to a LOW state, meeting the I_{ODL} limit in DC Electrical Characteristics table.
3. The device will enter a low power-down mode when CLK and $\overline{CLK}$ are both at logic LOW.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IK}	Input Clamp Voltage (All Inputs)	V_{DDQ} = 1.7V, I_I = -18mA	—	—	– 1.2	V
V_{IL}[2]	Input LOW Voltage (OE, OS, CLK, $\overline{CLK}$)		—	—	0.35V_{DDQ}	V
V_{IH}[2]	Input HIGH Voltage (OE, OS, CLK, $\overline{CLK}$)		0.65V_{DDQ}	—	—	
V_{IN}[1]	Input Signal Voltage		-0.3	—	V_{DDQ} + 0.3	V
$V_{ID(DC)}$[2]	DC Input Differential Voltage		0.3		V_{DDQ} + 0.4	V
V_{OD}[3]	Output Differential Voltage	A_{VDD}/V_{DDQ} = 1.7V	0.6	—	—	V
V_{OH}	Output HIGH Voltage	I_{OH} = -100µA, V_{DDQ} = 1.7V to 1.9V	V_{DDQ} - 0.2		—	V
		I_{OH} = -9mA, V_{DDQ} = 1.7V	1.1		—	
V_{OL}	Output LOW Voltage	I_{OL} = 100µA, V_{DDQ} = 1.7V to 1.9V			0.1	V
		I_{OL} = 9mA, V_{DDQ} = 1.7V			0.6	
I_{ODL}	Output Disabled LOW Current	OE = L, V_{ODL} = 100mV, A_{VDD}/V_{DDQ} = 1.7V	100	—	—	µA
I_{IN}	Input Current: CLK, $\overline{CLK}$	A_{VDD}/V_{DDQ} = Max., V_I = 0V to V_{DDQ}			±250	µA
	Input Current: OE, OS, FBIN, $\overline{FBIN}$				±10	
I_{DDLD}	Static Supply Current (I_{DDQ} and I_{ADD})	A_{VDD}/V_{DDQ} = Max., CLK and $\overline{CLK}$ = GND			500	µA
I_{DD}	Dynamic Power Supply Current (I_{DDQ} and I_{ADD})[4,5]	A_{VDD}/V_{DDQ} = Max., CLK = 410MHz			300	mA

NOTES:
1. V_{IN} specifies the allowable DC excursion of each different output.
2. V_{ID} is the magnitude of the difference between the input level on CLK and the input level on $\overline{CLK}$. The CLK and $\overline{CLK}$ V_{IH} and V_{IL} limits are used to define the DC LOW and HIGH levels for the power down mode.
3. V_{OD} is the magnitude of the difference between the true output level and the complementary level.
4. All Outputs are left open (unconnected to PCB).
5. Total I_{DD} = I_{DDQ} + I_{ADD} = F_{CK} * C_{PD} * V_{DDQ}, for Cpd = (I_{DDQ} + I_{ADD}) / (F_{CK} * V_{DDQ}) where F_{CK} is the input frequency, V_{DDQ} is the power supply, and C_{PD} is the Power Dissipation Capacitance.

TIMING REQUIREMENTS

Symbol	Parameter	Min.	Max.	Unit
f_{CLK}	Operating Clock Frequency[1,2,5]	125	410	MHz
	Application Clock Frequency[1,3,5]	160	410	MHz
t_{DC}	Input Clock Duty Cycle	40	60	%
t_L	Stabilization Time[4]	—	6	µs

NOTES:
1. The PLL will track a spread spectrum clock input.
2. Operating clock frequency is the range over which the PLL will lock, but may not meet all timing specifications. To be used only for low speed system debug.
3. Application clock frequency is the range over which timing specifications apply.
4. Stabilization time is the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal after power up. During normal operation, the stabilization time is also the time required for the PLL circuit to obtain phase lock of its feedback signal to its reference signal when CLK and $\overline{CLK}$ go to a logic LOW state, enters the power-down mode, and later return to active operation. CLK and $\overline{CLK}$ may be left floating after they have been driven LOW for one complete clock cycle.
5. Will lock to input frequency as low as 30MHz at room temperature and nominal or higher supply voltage (1.8V - 1.9V).

AC ELECTRICAL CHARACTERISTICS(1)

Symbol	Description	f_{CK} (MHz)	Min.	Typ.(2)	Max.	Unit
t_{EN}	OE to any Y/$\overline{Y}$	160 to 410	—	—	8	ns
t_{DIS}	OE to any Y/$\overline{Y}$	160 to 410	—	—	8	ns
$SLR_{(I)}$	Output Enable ($\overline{OE}$)	160 to 410	0.5	—	—	V/ns
	Input Clock Slew Rate, measured single-ended	160 to 410	1	2.5	4	
$SLR_{(O)}$(4)	Output Clock Slew Rate, measured single-ended	160 to 410	1.5	2.5	3	V/ns
V_{OX}(6)	Output Differential-Pair Cross-Voltage	160 to 410	(V_{DDQ}/2) -0.1	—	(V_{DDQ}/2) +0.1	V
$t_{JIT(CC+)}$	Cycle-to-Cycle Period Jitter	160 to 410	0	—	40	ps
$t_{JIT(CC-)}$	Cycle-to-Cycle Period Jitter	160 to 410	0	—	-40	ps
$t_{(\varnothing)}$(5)	Static Phase Offset	160 to 410	-50	—	50	ps
$t_{(\varnothing)DYN}$(7)	Dynamic Phase Offset	160 to 270	-50	—	50	ps
		271 to 410	$t_{(\varnothing)DYN(MIN)}$	—	$t_{(\varnothing)DYN(MAX)}$	
$t_{SK(O)}$(7)	Output Clock Skew	160 to 270	—	—	40	ps
		271 to 410	—	—	$t_{SK(O)MAX}$	
$t_{JIT(PER)}$(3,7)	Period Jitter	160 to 270	-40	—	40	ps
		271 to 410	$t_{JIT(PER)MIN}$	—	$t_{JIT(PER)MAX}$	
$t_{JIT(HPER)}$(3)	Half-Period Jitter	160 to 270	-75	—	75	ps
		271 to 410	-50	—	50	
$\Sigma t_{(SU)}$(7)	$\lvert t_{JIT(PER)} \rvert + \lvert t_{(\varnothing)DYN} \rvert + t_{SK(O)}$	271 to 410	—	—	80	ps
$\Sigma t_{(H)}$(7)	$\lvert t_{(\varnothing)DYN} \rvert + t_{SK(O)}$	271 to 410	—	—	60	ps
The PLL on the CSPUA877 will meet all the above test parameters while supporting SSC synthesizers with the following parameters:						
	SSC Modulation Frequency		30	—	33	KHz
	SSC Clock Input Frequency Deviation		0	—	0.5	%
CSPUA877 PLL designs should target the value below to minimize SSC-induced skew:						
	PLL Loop Bandwidth (-3dB from unity gain)		2	—	—	MHz

NOTES:

1. There are two different terminations that are used with the above AC tests. The output load shown in figure 1 is used to measure the input and output differential pair cross-voltage only. The output load shown in figure 2 is used to measure all other tests, including input and output slew rates. For consistency, use 50Ω equal length cables with SMA connectors on the test board.
2. Refers to transition of non-inverting output.
3. Period jitter and half-period jitter specifications are seperate specifications that must be met independently of each other.
4. To eliminate the impact of input slew rates on static phase offset, the input slew rates of reference clock input (CLK, $\overline{CLK}$) and feedback clock input (FBIN, $\overline{FBIN}$) are recommended to be nearly equal. The 2.5V/ns slew rates are shown as a recommended target. Compliance with these nominal values is not mandatory if it can be adequately demonstrated that alternative characteristics meet the requirements of the registered DDR2 DIMM application.
5. Static phase offset does not include jitter.
6. V_{OX} is specified at the DDR DRAM clock input or test load.
7. In the frequency range of 271 - 410MHz, the min and max values for $t_{JIT(PER)}$ and $t_{(\varnothing)DYN}$, and the max value for $t_{SK(O)}$, must not exceed the corresponding min and max values of the 160 - 270MHz range. Also, the sum of the specified values for $\lvert t_{JIT(PER)} \rvert$, $\lvert t_{(\varnothing)DYN} \rvert$, and $t_{SK(O)}$ must meet the requirement for $\Sigma t_{(SU)}$, and the sum of the specified values for $\lvert t_{(\varnothing)DYN} \rvert$ and $t_{SK(O)}$ must meet the requirement for $\Sigma t_{(H)}$.

TEST CIRCUIT AND SWITCHING WAVEFORMS

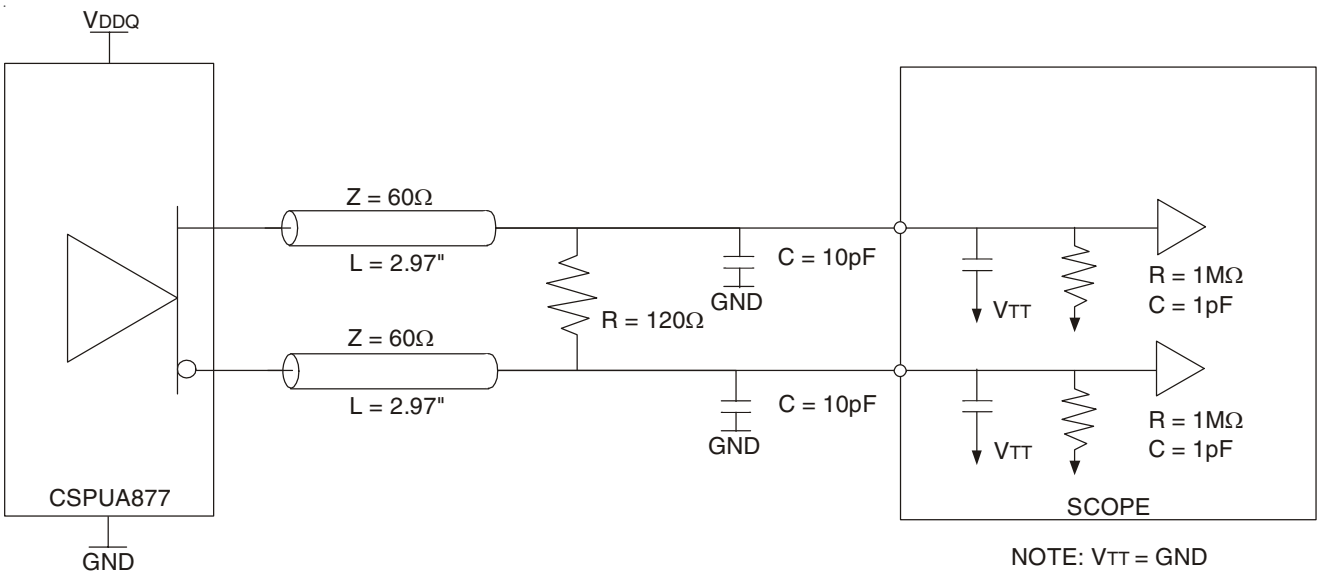


Figure 1: Output Load Test Circuit 1

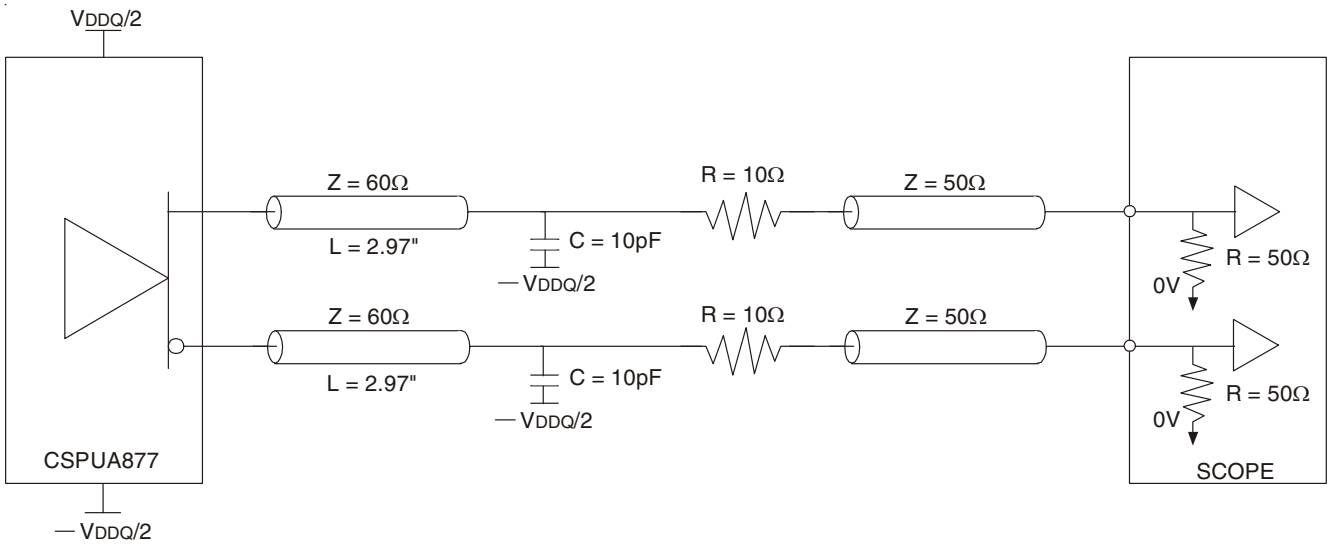
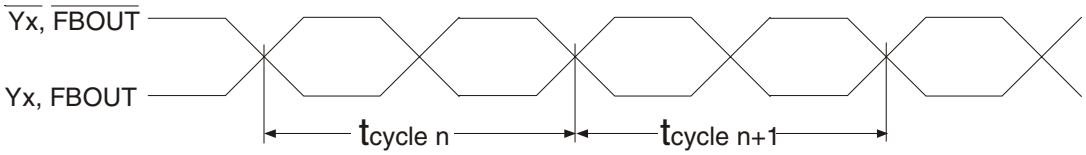


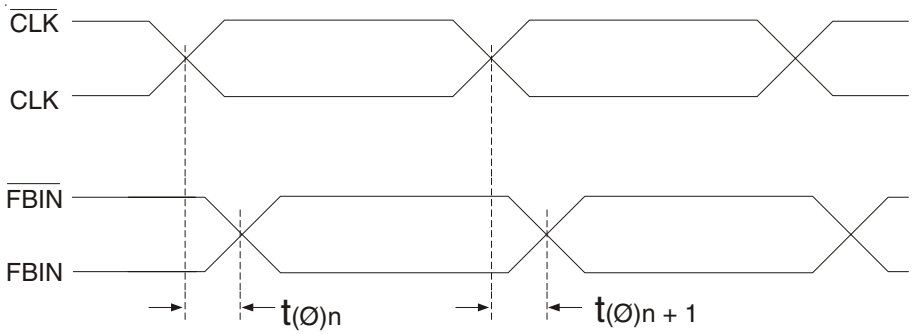
Figure 2: Output Load Test Circuit 2

TEST CIRCUIT AND SWITCHING WAVEFORMS



$$t_{jit(cc)} = t_{cycle\ n} - t_{cycle\ n+1}$$

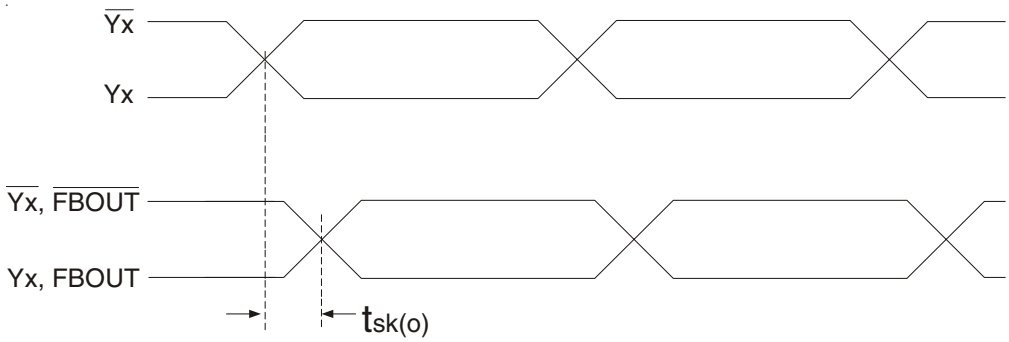
Cycle-to-Cycle jitter



$$t_{(Ø)} = \frac{\sum_{1}^{n=N} t_{(Ø)n}}{N}$$

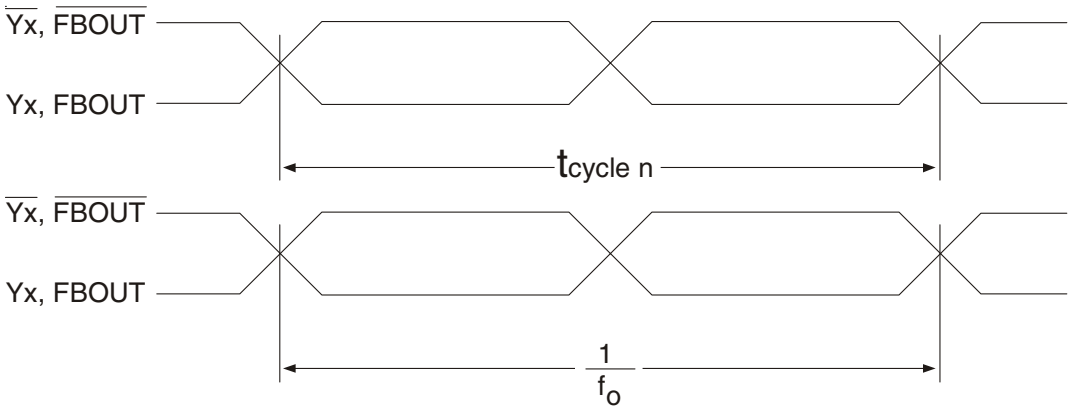
(N is a large number of samples)

Static Phase Offset



Output Skew

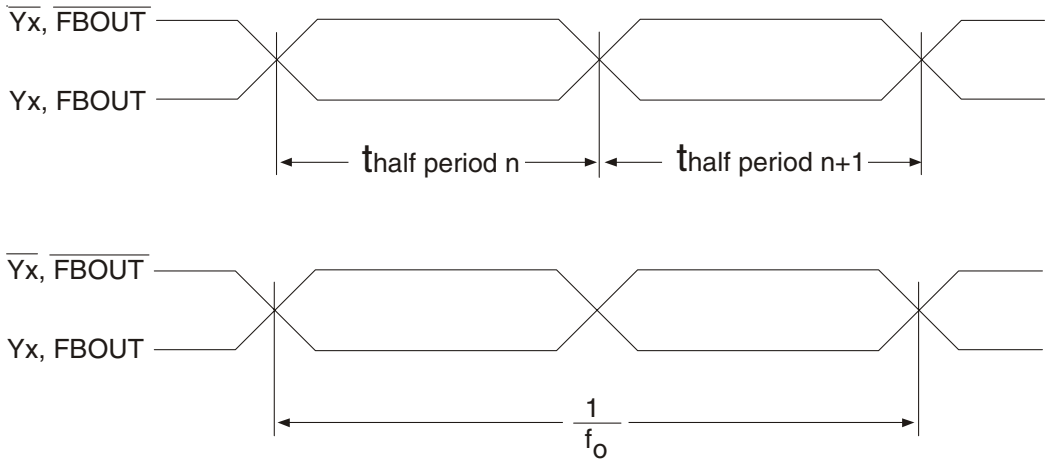
TEST CIRCUIT AND SWITCHING WAVEFORMS



$$t_{jit(per)} = t_{cycle\ n} - \frac{1}{f_o}$$

NOTE:
fo = Average input frequency measured at CLK / $\overline{CLK}$

Period jitter

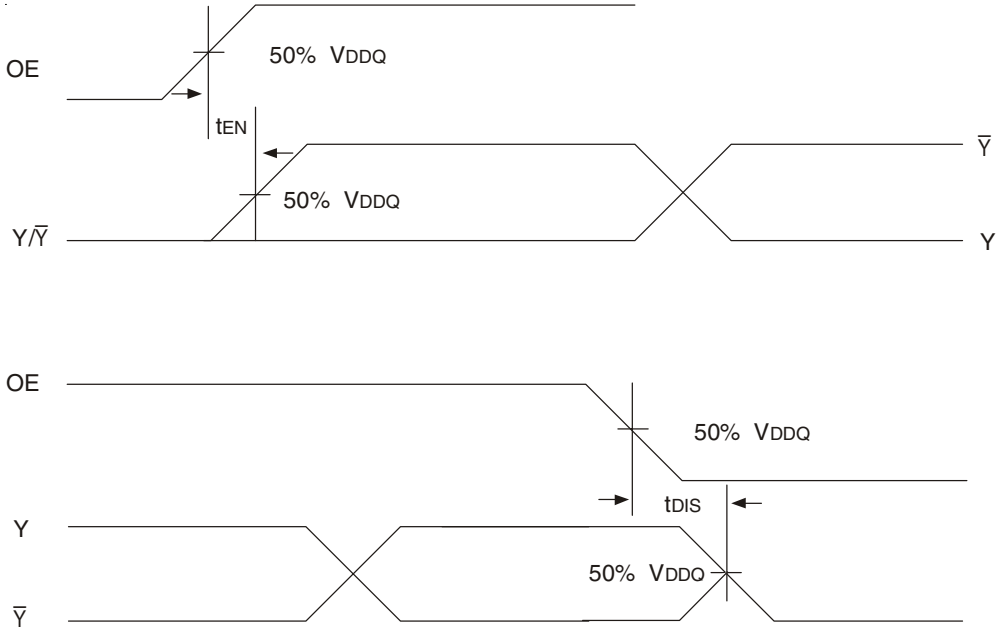


$$t_{jit(hper)} = t_{half\ period\ n} - \frac{1}{2*f_o}$$

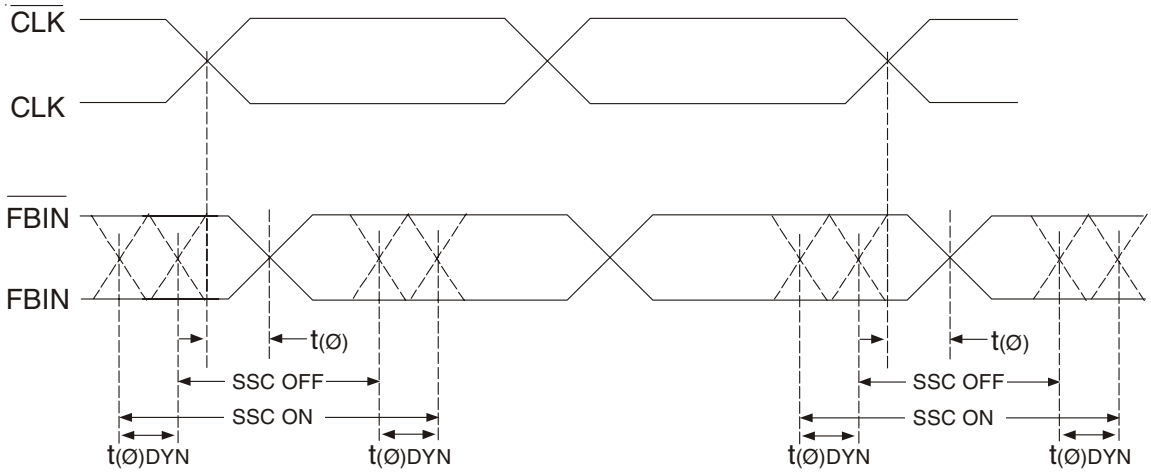
NOTE:
fo = Average input frequency measured at CLK / $\overline{CLK}$

Half-Period jitter

TEST CIRCUIT AND SWITCHING WAVEFORMS

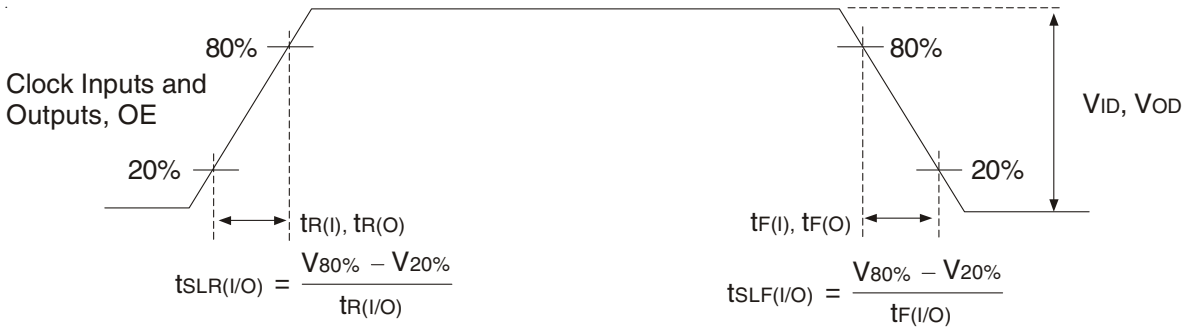


Time Delay Between Output Enable (OE) and Clock Output (Y, Y)

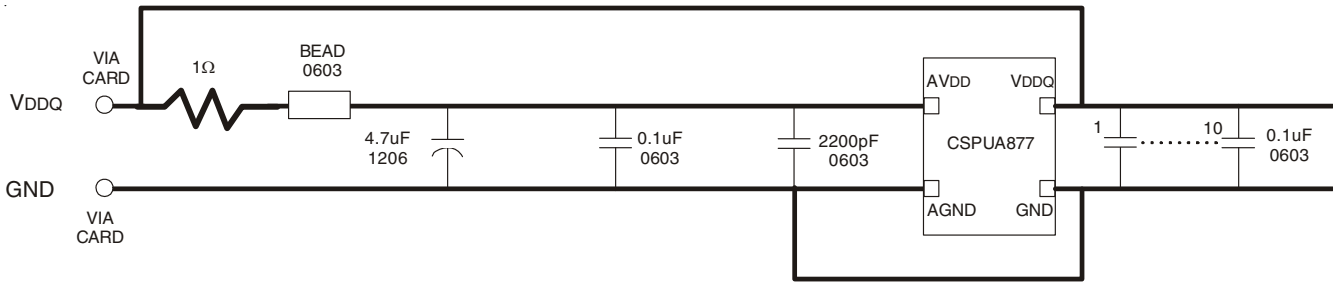


Dynamic Phase Offset

TEST CIRCUIT AND SWITCHING WAVEFORMS



Input and Output Slew Rates



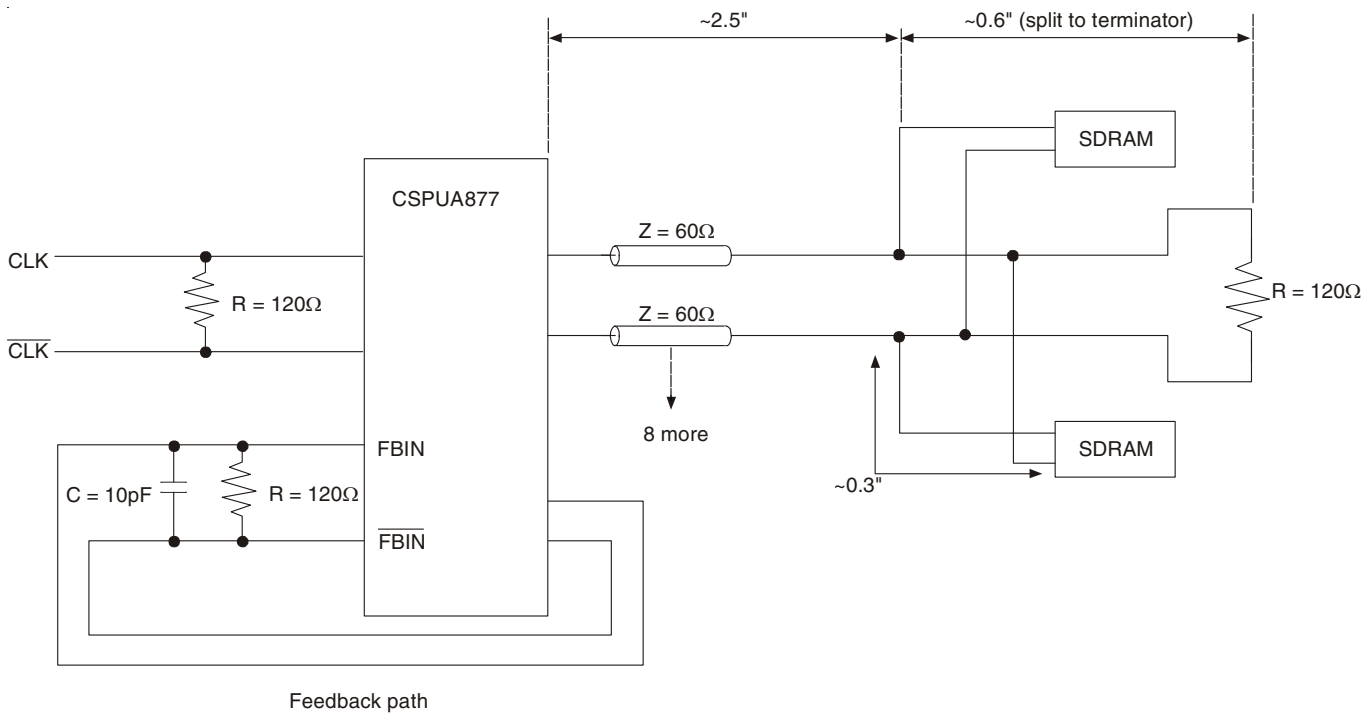
NOTES:
Place all decoupling capacitors as close to the CSPUA877 pins as possible.
Use wide traces for AVDD and AGND.
Recommended bead: Fair-rite P/N 2506036017Y0 or equivalent (0.8Ω DC max., 600Ω at 100MHz).

Recommended Filtering for the Analog and Digital Power Supplies (AVDD and VDDQ)

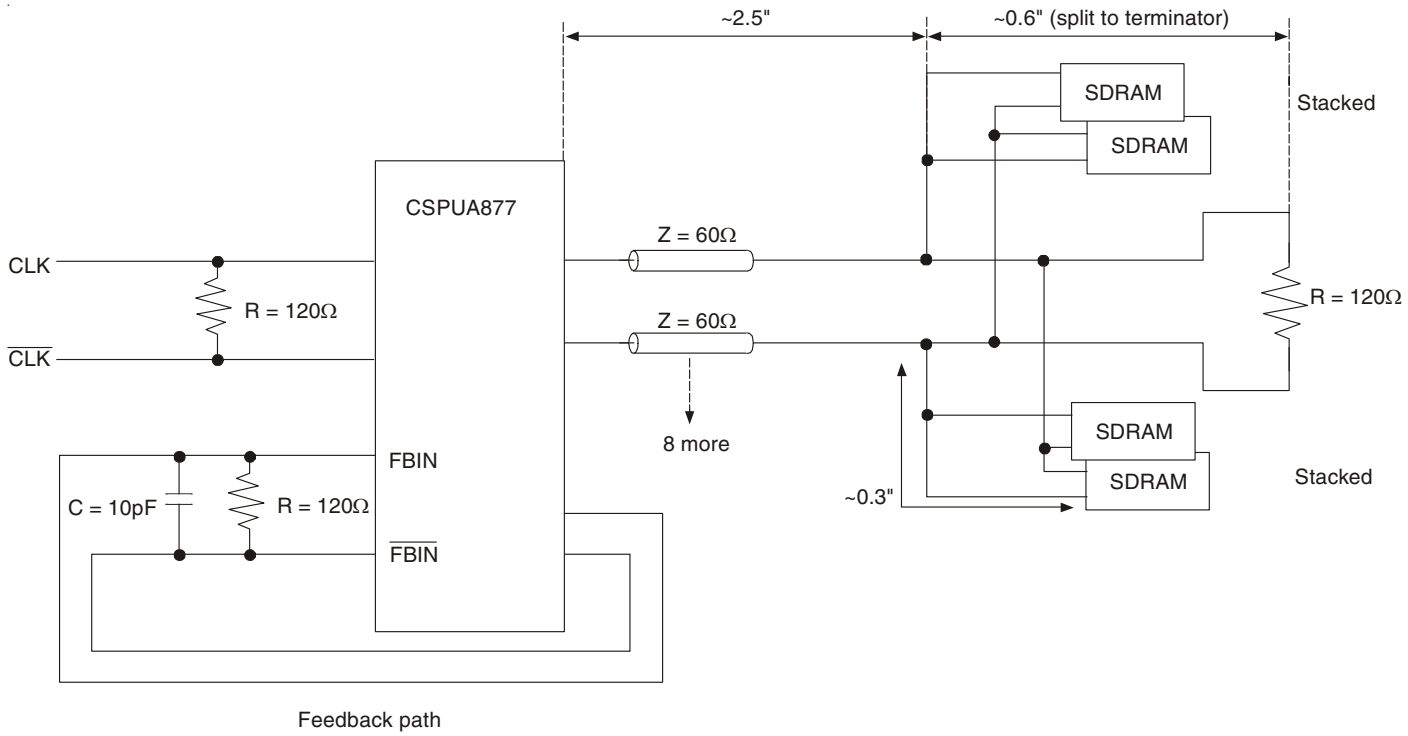
APPLICATION INFORMATION

Clock Structure	# of SDRAM Loads per Clock	Clock Loading on the PLL outputs (pF)	
		Min.	Max.
#1	2	3	5
#2	4	6	10

APPLICATION INFORMATION

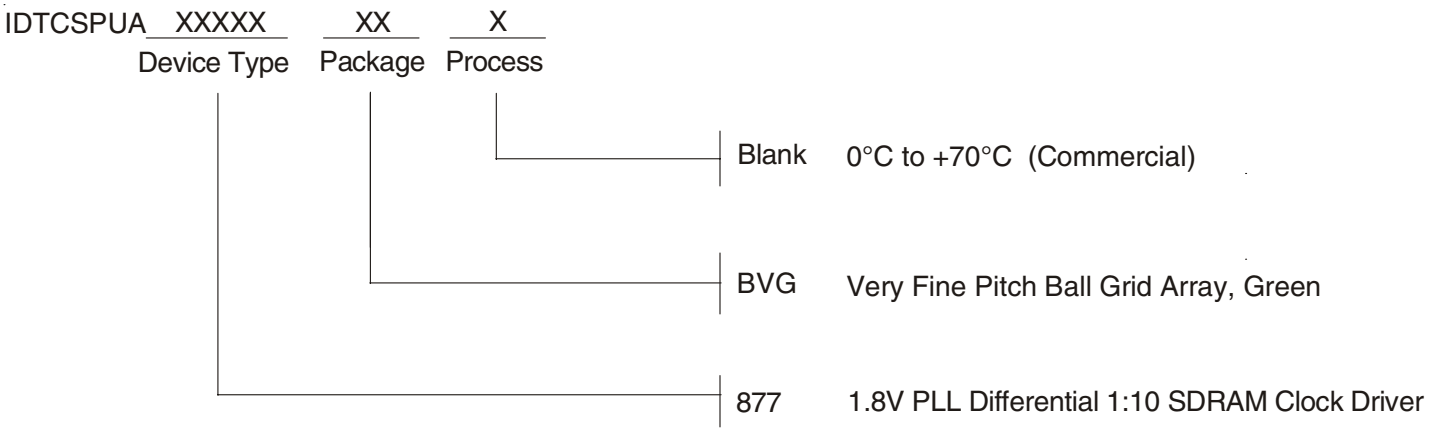


Clock Structure 1



Clock Structure 2

ORDERING INFORMATION



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