PROGRAMMABLE FLEXPC CLOCK FOR P4 PROCESSOR

IDTCV133

FEATURES:

- **Power management control suitable for notebook applications**
- **One high precision PLL for CPU, SSC and N programming**
- **One high precision PLL for SRC/PCI, supports 100MHz output frequency, SSC and N programming**
- **One high precision PLL for LVDS. Supports 100/96MHz output frequency, SSC programming**
- **One high precision PLL for 96MHz/48MHz**
- **Band-gap circuit for differential outputs**
- **Support spread spectrum modulation, –0.5 down spread and others**
- **Support SMBus block read/write, index read/write**
- **Selectable output strength for REF**
- **Allows for CPU frequency to change to a slower frequency to conserve power when an application is less execution-intensive**
- **Smooth transition for N programming**
- **Available in TSSOP package**

KEY SPECIFICATION:

- **CPU CLK cycle to cycle jitter < 100ps**
- **SRC CLK cycle to cycle jitter < 125ps**
- **PCI CLK cycle to cycle jitter < 500ps**

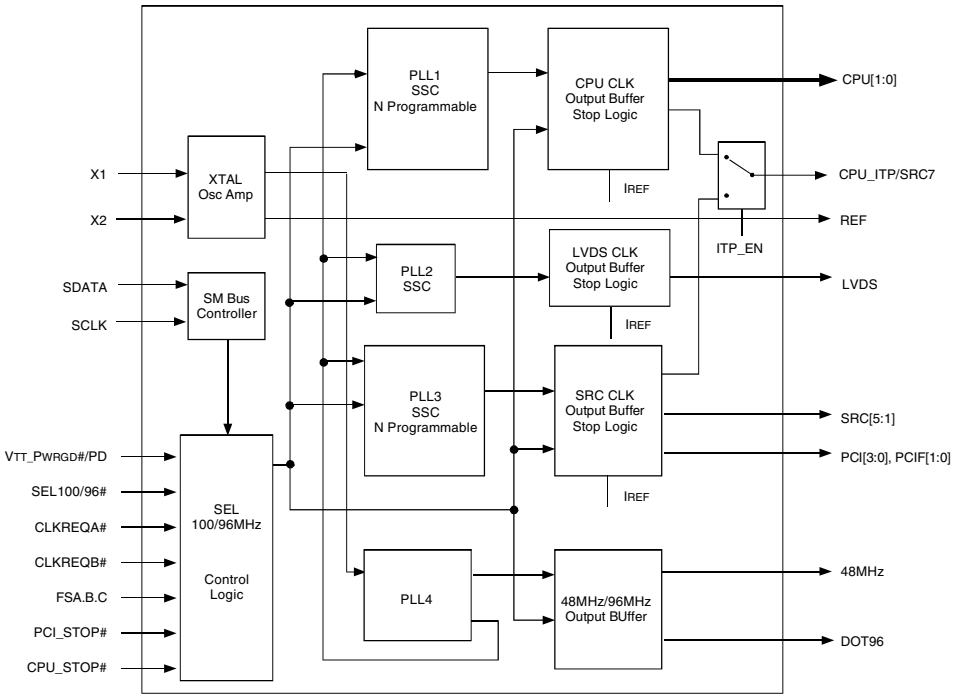
DESCRIPTION:

IDTCV133 is a 56 pin clock device, incorporating both Intel CK410M and CKSSCD requirements, for Intel advance P4 processors. The CPU output buffer is designed to support up to 400MHz processor. This chip has four PLLs inside for CPU, SRC/PCI, LVDS, and 48MHz/DOT96 IO clocks. This device also implements Band-gap referenced I_{REF} to reduce the impact of V_{DD} variation on differential outputs, which can provide more robust system performance. Each CPU/SRC/LVDS has its own Spread Spectrum selection.

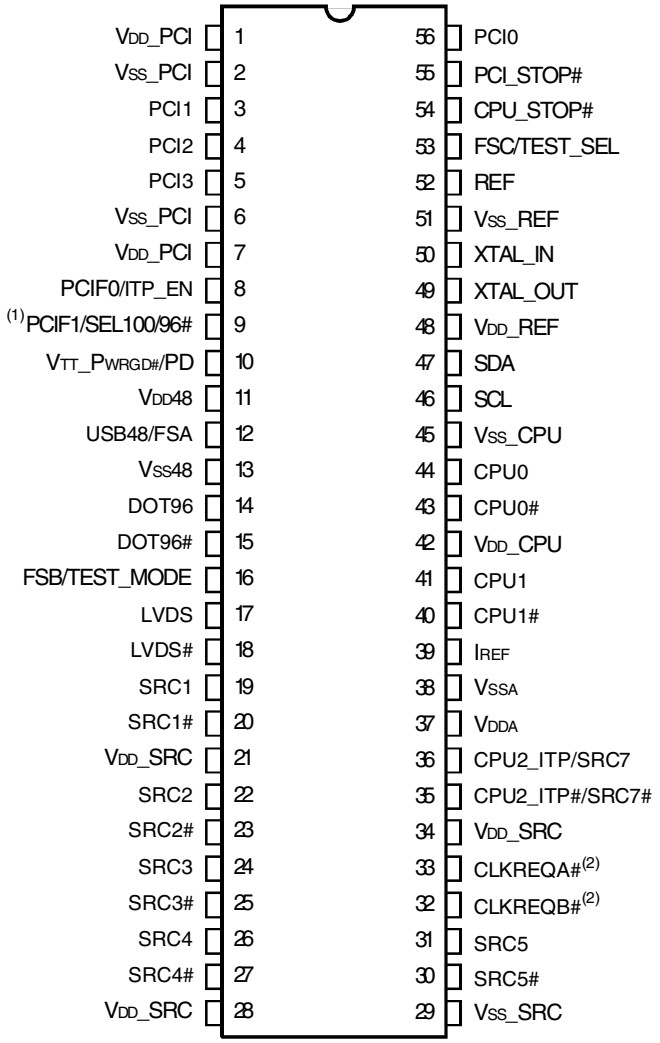
OUTPUTS:

- **2*0.7V current –mode differential CPU CLK pair**
- **5*0.7V current –mode differential SRC CLK pair**
- **One CPU_ITP/SRC selectable CLK pair**
- **6*PCI, 2 free running, 33.3MHz**
- **1*96MHz, 1*48MHz**
- **1*REF**
- **One 100/96 MHz differential LVDS**

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



NOTES:
1. 130K pull-up resistor.
2. 130K pull-down resistor.

TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Min	Max	Unit
V_{DDA}	3.3V Core Supply Voltage		4.6	V
V_{DD}	3.3V Logic Input Supply Voltage	GND - 0.5	4.6	V
T_{STG}	Storage Temperature	–65	+150	° C
$T_{AMBIENT}$	Ambient Operating Temperature	0	+70	° C
T_{CASE}	Case Temperature		+115	° C
ESD Prot	Input ESD Protection Human Body Model	2000		V

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

FREQUENCY SELECTION TABLE

FSC, B, A	CPU	SRC[7:0]	PCI	USB	DOT	REF
101	100	100	33.3	48	96	14.318
001	133	100	33.3	48	96	14.318
011	166	100	33.3	48	96	14.318
010	200	100	33.3	48	96	14.318
000	266	100	33.3	48	96	14.318
100	333	100	33.3	48	96	14.318
110	400	100	33.3	48	96	14.318
111	Reserve	100	33.3	48	96	14.318

PIN DESCRIPTION

Pin Number	Name	Type	Description
1	V_{DD}_PCI	PWR	3.3V
2	V_{SS}_PCI	GND	GND
3	PCI1	OUT	PCI clock
4	PCI2	OUT	PCI clock
5	PCI3	OUT	PCI clock
6	V_{SS}_PCI	GND	GND
7	V_{DD}_PCI	PWR	3.3V
8	PCIF0/ITP_EN	I/O	PCI clock, free running. CPU2 select (sampled on V_{TT}_P_{WRGD}# assertion) HIGH = CPU2.
9	PCIF1/SEL100/96#	I/O	PCI clock, free running. SEL100/96MHz (sampled on V_{TT}_P_{WRGD}# assertion) HIGH, LVDS = 100MHz.
10	V_{TT}_P_{WRGD}#/PD	IN	Level-sensitive strobe used to latch the FSA, FSB, FSC/TEST_SEL, and PCIF0/ITP_EN inputs. After V_{TT}_P_{WRGD}# assertion, becomes a real-time input for asserting power down. (Active HIGH). Latch PCIF1/SEL100/96# input.
11	V_{DD}48	PWR	3.3V
12	USB48/FSA	I/O	48MHz clock/FSA for CPU frequency selection
13	V_{SS}48	GND	GND
14	DOT96	OUT	96MHz 0.7 current mode differential clock output
15	DOT96#	OUT	96MHz 0.7 current mode differential clock output
16	FSB/TEST_MODE	IN	CPU frequency selection. Selects R_{EF}/N or Hi-Z when in test mode, Hi-Z = 1, R_{EF}/N = 0.
17	LVDS	OUT	Differential serial reference clock
18	LVDS#	OUT	Differential serial reference clock
19	SRC1	OUT	Differential serial reference clock
20	SRC1#	OUT	Differential serial reference clock
21	V_{DD}_SRC	PWR	3.3V
22	SRC2	OUT	Differential serial reference clock
23	SRC2#	OUT	Differential serial reference clock
24	SRC3	OUT	Differential serial reference clock
25	SRC3#	OUT	Differential serial reference clock
26	SRC4	OUT	Differential serial reference clock
27	SRC4#	OUT	Differential serial reference clock
28	V_{DD}_SRC	PWR	3.3V
29	V_{SS}_SRC	GND	GND
30	SRC5#	OUT	Differential serial reference clock
31	SRC5	OUT	Differential serial reference clock
32	CLKREQB#	IN	SRC clock enable (Active LOW, see Byte 21)
33	CLKREQA#	IN	SRC clock enable (Active LOW, see Byte 21)
34	V_{DD}_SRC	PWR	3.3V
35	CPU2_ITP#/SRC7#	OUT	Selectable CPU or SRC differential clock output. ITP_EN = 0 at V_{TT}_P_{WRGD}# assertion = SRC7#.
36	CPU2_ITP/SRC7	OUT	Selectable CPU or SRC differential clock output. ITP_EN = 0 at V_{TT}_P_{WRGD}# assertion = SRC7.
37	V_{DDA}	PWR	3.3V
38	V_{SSA}	GND	GND
39	I_{REF}	OUT	Reference current for differential output buffer
40	CPU1#	OUT	Host 0.7 current mode differential clock output
41	CPU1	OUT	Host 0.7 current mode differential clock output
42	V_{DD}_CPU	PWR	3.3V

PIN DESCRIPTION (CONT.)

Pin Number	Name	Type	Description
43	CPU0#	OUT	Host 0.7 current mode differential clock output
44	CPU0	OUT	Host 0.7 current mode differential clock output
45	V_{SS}_CPU	GND	GND
46	SCL	IN	SM bus clock
47	SDA	I/O	SM bus data
48	V_{DD}_REF	PWR	3.3V
49	XTAL_OUT	OUT	XTAL output
50	XTAL_IN	IN	XTAL input
51	V_{SS}_REF	GND	GND
52	REF	OUT	14.318 MHz reference clock output
53	FSC/TEST_SEL	IN	CPU frequency selection. Selects test mode if pulled above 2V when V_{TT}_P_{WRGD}# is asserted LOW.
54	CPU_STOP#	IN	Stop all stoppable CPU CLK
55	PCI_STOP#	IN	Stop all stoppable PCI, SRC CLK
56	PCI0	OUT	PCI clock

INDEX BLOCK WRITE PROTOCOL

Bit	# of bits	From	Description
1	1	Master	Start
2-9	8	Master	D2h
10	1	Slave	Ack (Acknowledge)
11-18	8	Master	Register offset byte (starting byte)
19	1	Slave	Ack (Acknowledge)
20-27	8	Master	Byte count, N (0 is not valid)
28	1	Slave	Ack (Acknowledge)
29-36	8	Master	first data byte (Offset data byte)
37	1	Slave	Ack (Acknowledge)
38-45	8	Master	2nd data byte
46	1	Slave	Ack (Acknowledge)
			:
		Master	Nth data byte
		Slave	Acknowledge
		Master	Stop

INDEX BLOCK READ PROTOCOL

Master can stop reading any time by issuing the stop bit without waiting until Nth byte (byte count bit30-37).

Bit	# of bits	From	Description
1	1	Master	Start
2-9	8	Master	D2h
10	1	Slave	Ack (Acknowledge)
11-18	8	Master	Register offset byte (starting byte)
19	1	Slave	Ack (Acknowledge)
20	1	Master	Repeated Start
21-28	8	Master	D3h
29	1	Slave	Ack (Acknowledge)
30-37	8	Slave	Byte count, N (block read back of N bytes), power on is 8
38	1	Master	Ack (Acknowledge)
39-46	8	Slave	first data byte (Offset data byte)
47	1	Master	Ack (Acknowledge)
48-55	8	Slave	2nd data byte
			Ack (Acknowledge)
			:
		Master	Ack (Acknowledge)
		Slave	Nth data byte
			Not acknowledge
		Master	Stop

INDEX BYTE WRITE

Setting bit[11:18] = starting address, bit[20:27] = 01h.

INDEX BYTE READ

Setting bit[11:18] = starting address. After reading back the first data byte, master issues Stop bit.

SSC MAGNITUDE CONTROL FOR CPU, SRC, AND SMC

SMC[2:0]	
000	-0.25
001	-0.5
010	-0.75
011	-1
100	±0.125
101	±0.25
110	±0.375
111	±0.5

RESOLUTION

CPU (MHz)	Resolution	N =
100	0.666667	150
133	0.666667	200
166	1.333333	125
200	1.333333	150
266	1.333333	200
333	2.666667	125
400	2.666667	150

SEL 100/96# CONFIGURATION

SEL 100/96#	LVDS Frequency	Unit
0	96	MHz
1	100	MHz

S.E. CLOCK STRENGTH SELECTION (PCI, REF, USB48)

Str[1:0]	Level
00	1
01	0.8
10	0.6
11	1.2

SPREAD SPECTRUM CONTROL SELECTION FOR LVDS (SSC-1)

S[3:0]	Spread
0000	-0.8%
0001	-1%
0010	-1.25%
0011	-1.5%
0100	-1.75%
0101	-2%
0110	-0.3%
0111	-0.5%
1000	±0.3%
1001	±0.4%
1010	±0.5%
1011	±0.6%
1100	±0.8%
1101	±1%
1110	±1.25%
1111	±1.5%

SPREAD SPECTRUM CONTROL SELECTION FOR LVDS (SSC-2)

S[3:0]	Spread
0000	-0.8%
0001	-1%
0010	-1.25%
0011	-1.5%
0100	-1.75%
0101	-2%
0110	-2.5%
0111	-3%
1000	±0.3%
1001	±0.4%
1010	±0.5%
1011	±0.6%
1100	±0.8%
1101	±1%
1110	±1.25%
1111	±1.5%

CONTROL REGISTERS

N PROGRAMMING PROCEDURE

- Use Index byte write.
- For N programming, the user only needs to access Byte 12, Byte 13, and Byte 10.

1. Write Byte 12 for CPU PLL N, CPU f = N* Resolution (see resolution table).
2. Write Byte 13 for SRC PLL N, SRC f = N*0.666667, PCI = SRC f /3.
3. Enable N Programming bit, Byte 10 bit 1. Once this bit is enabled, any N value will be changed on the fly.

BYTE 0

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
0	LVDS, LVDS#	Output Enable	Tristate	Enable	RW	1
1	SRC1, SRC1#	Output Enable	Tristate	Enable	RW	1
2	SRC2, SRC2#	Output Enable	Tristate	Enable	RW	1
3	SRC3, SRC3#	Output Enable	Tristate	Enable	RW	1
4	SRC4, SRC4#	Output Enable	Tristate	Enable	RW	1
5	SRC5, SRC5#	Output Enable	Tristate	Enable	RW	1
6	Reserved				RW	1
7	CPU2, CPU2#/ SRC7, SRC7#	Output Enable	Tristate	Enable	RW	1

BYTE 1

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
0	CPU[2:0], SRC[7,5:1], PCI[3:0], PCIF[1:0]	Spread Spectrum mode enable	Spread off	Spread on	RW	0
1	CPU0, CPU0#	Output Enable	Tristate	Enable	RW	1
2	CPU1, CPU1#	Output Enable	Tristate	Enable	RW	1
3	Reserved				RW	1
4	REF	Output Enable	Tristate	Enable	RW	1
5	USB48	Output Enable	Tristate	Enable	RW	1
6	DOT96	Output Enable	Tristate	Enable	RW	1
7	PCIF0	Output Enable	Tristate	Enable	RW	1

BYTE 2

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
0	PCIF1	Output Enable	Tristate	Enable	RW	1
1	Reserved				RW	1
2	Reserved				RW	1
3	Reserved				RW	1
4	PCI0	Output Enable	Tristate	Enable	RW	1
5	PCI1	Output Enable	Tristate	Enable	RW	1
6	PCI2	Output Enable	Tristate	Enable	RW	1
7	PCI3	Output Enable	Tristate	Enable	RW	1

BYTE 3

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	LVDS	Allow controlled by PCI_STOP# assertion	Free running, not affected by PCI_STOP#	Stopped with PCI_STOP#	RW	0
1	SRC1				RW	0
2	SRC2				RW	0
3	SRC3				RW	0
4	SRC4				RW	0
5	SRC5				RW	0
6	Reserved				RW	0
7	SRC7	Allow controlled by PCI_STOP# assertion	Free running, not affected by PCI_STOP#	Stopped with PCI_STOP#	RW	0

BYTE 4

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	CPU0, CPU0#	Allow control of CPU0 with assertion of CPU_STOP#	Not stopped by CPU_STOP#	Stopped with CPU_STOP#	RW	1
1	CPU1, CPU1#	Allow control of CPU1 with assertion of CPU_STOP#	Not stopped by CPU_STOP#	Stopped with CPU_STOP#	RW	1
2	CPU2, CPU2#	Allow control of CPU2 with assertion of CPU_STOP#	Not stopped by CPU_STOP#	Stopped with CPU_STOP#	RW	1
3	PCIF0	Allow controlled by PCI_STOP# assertion	Not stopped by PCI_STOP#	Stopped with PCI_STOP#	RW	0
4	PCIF1				RW	0
5	Reserved				RW	0
6	DOT96	DOT96 power down drive mode	Driven in power down	Tristate	RW	0
7	Reserved				RW	0

BYTE 5

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	CPU0, CPU0#	CPU0 PD drive mode	Driven in power down	Tristate in power down	RW	0
1	CPU1, CPU1#	CPU1 PD drive mode	Driven in power down	Tristate in power down	RW	0
2	CPU2, CPU2#	CPU2 PD drive mode	Driven in power down	Tristate in power down	RW	0
3	SRCS	SRC PD drive mode	Driven in power down	Tristate in power down	RW	0
4	CPU0	CPU0 CPU_STOP drive mode	Driven in CPU_STOP#	Tristate when stopped	RW	0
5	CPU1	CPU1 CPU_STOP drive mode	Driven in CPU_STOP#	Tristate when stopped	RW	0
6	CPU2	CPU2 CPU_STOP drive mode	Driven in CPU_STOP#	Tristate when stopped	RW	0
7	SRCS	SRC PCI_STOP drive mode	Driven in PCI_STOP	Tristate when stopped	RW	0

BYTE 6

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	CPU[2:0]	FSA latched value on power up			R	FSA
1	CPU[2:0]	FSB latched value on power up			R	FSB
2	CPU[2:0]	FSC latched value on power up			R	FSC
3	PCI, SRC	Software PCI_STOP control for PCI and SRC CLK	Stop all PCI, PCIF, and SRC which can be stopped by PCI_STOP#	Software STOP Disabled	RW	1
4	REF	REF drive strength	1x drive	2x drive	RW	1
5	Reserved				RW	0
6		Test clock mode entry control	Normal operation	Test mode, controlled by Byte 6, Bit 7	RW	0
7	CPU, SRC, PCI PCIF, REF, USB48, DOT96	Only valid when Byte 6, Bit 7 is HIGH	Hi-Z	REF/N	RW	0

BYTE 7

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0		Vendor ID			R	1
1		Vendor ID			R	0
2		Vendor ID			R	1
3		Vendor ID			R	0
4		Revision ID			R	0
5		Revision ID			R	0
6		Revision ID			R	0
7		Revision ID			R	0

BYTE 8, BLOCK READ BYTE COUNT

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0						0
1						1
2						1
3						0
4						1
5						0
6						0
7						0

BYTE 9, LVDS CONTROL BYTE

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
0	LVDS	HW/ SMBus control	HW(1)	SW	RW	0
1	LVDS SSC EN	Spread spectrum enable	Off	On	RW	1
2	Reserved				RW	0
3	SEL 100/96#	Select LVDS frequency	96MHz	100MHZ	RW	SEL 100/96#
4	S3	see SSC table			RW	0
5	S2	see SSC table			RW	1
6	S1	see SSC table			RW	1
7	S0	see SSC table			RW	1

NOTE:
1. If bit 0 is set to 0, LVDS output frequency is selected by HW SEL 100/96#. If bit 0 is set to 1, LVDS output frequency is selected by bit 3.

BYTE 10

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	Reserved				RW	0
1		N Programming enable	Disable	Enable	RW	0
2		LVDS PLL power down	Normal	Power Down	RW	0
3	Reserved				RW	0
4		USB PLL power down	Normal	Power Down	RW	0
5		SRC PLL power down	Normal	Power Down	RW	0
6		CPU PLL power down	Normal	PowerDown	RW	0
7	Reserved				RW	0

BYTE 11

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	SRC SMC0	SRC/PCI SSC control see SMC table			RW	1
1	SRC SMC1				RW	0
2	SRC SMC2				RW	0
3	Reserved				RW	0
4	CPU SMC0	CPU PLL SSC control see SMC table			RW	1
5	CPU SMC1				RW	0
6	CPU SMC2				RW	0
7	Reserved				RW	0

BYTE 12

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	CPU_N0, LSB	CPU CLK = N* Resolution			RW	0
1	CPU_N1	see Resolution table			RW	1
2	CPU_N2				RW	1
3	CPU_N3				RW	0
4	CPU_N4				RW	1
5	CPU_N5				RW	0
6	CPU_N6				RW	0
7	CPU_N7, MSB				RW	1

BYTE 13

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	SRC_N0, LSB	SRC f = N*SRC Resolution			RW	0
1	SRC_N1	Resolution = 0.666667			RW	1
2	SRC_N2	100MHz N= 150			RW	1
3	SRC_N3				RW	0
4	SRC_N4				RW	1
5	SRC_N5				RW	0
6	SRC_N6				RW	0
7	SRC_N7, MSB				RW	1

BYTE 14

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	48MHzStr0				RW	1
1	48MHStr1	USB48MHz0 strength selection			RW	1
2	REFStr0				RW	0
3	REFStr1	REF strength selection			RW	0
4	PCIStrC0				RW	0
5	PCIStrC1	PCI strength selection			RW	0
6	PCIFStr0				RW	0
7	PCIFStr1	PCIF strength selection			RW	0

BYTE 15

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	PCI0	Allow controlled by PCI_STOP# assertion	Free running, not affected by PCI_STOP#	Stopped with PCI_STOP#	RW	1
1	PCI1				RW	1
2	PCI2				RW	1
3	PCI3				RW	1
4	Reserved					0
5	Reserved					0
6	Reserved					0
7	Reserved					0

BYTES 16 - 20 ARE NOT TO BE USED

BYTE 18

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0		keep this bit 0			RW	0
1		keep this bit 0			RW	0
2		keep this bit 0			RW	0
3		keep this bit 0			RW	0
4		keep this bit 0			RW	0
5		keep this bit 0			RW	0
6	LVDS	SSCD Spread Table Selection	SSC-1	SSC-2	RW	0
7		keep this bit 0			RW	0

BYTES 19 - 20 ARE NOT TO BE USED

BYTE 21(1,2)

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	LVDS	Controlled by CLKREQA#. When CLKREQA# is HIGH, output is Hi-Z	Not Controlled	Controlled	RW	0
1	SRC2				RW	0
2	SRC4				RW	1
3	Reserved				RW	0
4	SRC1	Controlled by CLKREQB#. When CLKREQB# is HIGH, output is Hi-Z	Not Controlled	Controlled	RW	0
5	SRC3				RW	0
6	SRC5				RW	1
7	Reserved				RW	0

NOTES:
1. When SRCCLK outputs controlled by CLKREQA# and CLKREQB# are enabled, clock output behavior will follow SMBus control bits (per CK410 spec).
2. Assertion/de-assertion time of CLKREQ# pins will match PCI_STOP# timing of the CK410 spec. This is 15ns from the assertion/de-assertion of CLKREQ# to the drive/tie-state of the respective SRCCLK output.

ELECTRICAL CHARACTERISTICS - INPUT / SUPPLY / COMMON OUTPUT PARAMETERS

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input HIGH Voltage	3.3V ± 5%	2	—	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage	3.3V ± 5%	V_{SS} - 0.3	—	0.8	V
V_{IH_FS}	LOW Voltage, HIGH Threshold	For FSA.B.C test_mode	0.7	—	V_{DD} + 0.3	V
V_{IL_FS}	LOW Voltage, LOW Threshold	For FSA.B.C test_mode	V_{SS} - 0.3	—	0.35	V
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}	–5	—	5	µA
I_{IL1}	Input LOW Current	V_{IN} = 0V, inputs with no pull-up resistors	–5	—	—	µA
I_{IL2}	Input LOW Current	V_{IN} = 0V, inputs with pull-up resistors	–200	—	—	µA
$I_{DD3.3OP}$	Operating Supply Current	Full active, C_L = full load	—	—	400	mA
$I_{DD3.3PD}$	Powerdown Current	All differential pairs driven	—	—	70	mA
		All differential pairs tri-stated	—	—	12	
F_I	Input Frequency(1)	V_{DD} = 3.3V	—	14.31818	—	MHz
L_{PIN}	Pin Inductance(2)		—	—	7	nH
C_{IN}	Input Capacitance(2)	Logic inputs	—	—	5	pF
C_{OUT}		Output pin capacitance	—	—	6	
C_{INX}		XTAL_IN	—	—	5	
C_{OUTX}		XTAL_OUT	—	—	12	
T_{STAB}	Clock Stabilization(2,3)	From V_{DD} power-up or de-assertion of PD to first clock	—	—	1.8	ms
	Modulation Frequency(2)	Triangular modulation	30	—	33	KHz
	T_{DRIVE_SRC}(2)	SRC output enable after PCI_STOP# de-assertion	—	—	15	ns
	T_{DRIVE_PD}(2)	CPU output enable after PD de-assertion	—	—	300	us
	T_{FALL_PD}(2)	Fall time of PD	—	—	5	ns
	T_{RISE_PD}(3)	Rise time of PD	—	—	5	ns
	$T_{DRIVE\_CPU\_STOP\#}$(2)	CPU output enable after CPU_STOP# de-assertion	—	—	10	us
	$T_{FALL\_CPU\_STOP\#}$(2)	Fall time of CPU_STOP#	—	—	5	ns
	$T_{RISE\_CPU\_STOP\#}$(3)	Rise time of CPU_STOP#	—	—	5	ns

NOTES:
1. Input frequency should be measured at the REF output pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.
2. This parameter is guaranteed by design, but not 100% production tested.
3. See TIMING DIAGRAMS for timing requirements.

ELECTRICAL CHARACTERISTICS - CPU, SRC, AND DOT96 0.7 CURRENT MODE DIFFERENTIAL PAIR(1)

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 2pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Z_O	Current Source Output Impedance(2)	$V_O = V_X$	3000	—	—	Ω
V_{OH3}	Output HIGH Voltage	I_{OH} = -1mA	2.4	—	—	V
V_{OL3}	Output LOW Voltage	I_{OL} = 1mA	—	—	0.4	V
V_{HIGH}	Voltage HIGH(2)	Statistical measurement on single-ended signal using	660	—	900	mV
V_{LOW}	Voltage LOW(2)	oscilloscope math function	–150	—	150	
V_{OVS}	Max Voltage(2)	Measurement on single-ended signal using absolute value	—	—	1150	mV
V_{UDS}	Min Voltage(2)		–300	—	—	
$V_{CROSS(ABS)}$	Crossing Voltage (abs)(2)		250	—	550	mV
d - V_{CROSS}	Crossing Voltage (var)(2)	Variation of crossing over all edges	—	—	140	mV
ppm	Static Error(2,3)	See T_{PERIOD} Min. - Max. values	—	—	0	ppm
T_{PERIOD}	Average Period(3)	400MHz nominal / -0.5% spread	2.4993	—	2.5133	ns
		333.33MHz nominal / -0.5% spread	2.9991	—	3.016	
		266.66MHz nominal / -0.5% spread	3.7489	—	3.77	
		200MHz nominal / -0.5% spread	4.9985	—	5.0266	
		166.66MHz nominal / -0.5% spread	5.9982	—	6.032	
		133.33MHz nominal / -0.5% spread	7.4978	—	7.54	
		100MHz nominal / -0.5% spread	9.997	—	10.0533	
		96MHz nominal	10.4135	—	10.4198	
T_{ABSMIN}	Absolute Min Period(2,3)	400MHz nominal / -0.5% spread	2.4143	—	—	ns
		333.33MHz nominal / -0.5% spread	2.9141	—	—	
		266.66MHz nominal / -0.5% spread	3.6639	—	—	
		200MHz nominal / -0.5% spread	4.9135	—	—	
		166.66MHz nominal / -0.5% spread	5.9132	—	—	
		133.33MHz nominal / -0.5% spread	7.4128	—	—	
		100MHz nominal / -0.5% spread	9.912	—	—	
		96MHz nominal	10.1635	—	—	
t_R	Rise Time(2)	V_{OL} = 0.175V, V_{OH} = 0.525V	175	—	700	ps
t_F	Fall Time(2)	V_{OL} = 0.175V, V_{OH} = 0.525V	175	—	700	ps
d-t_R	Rise Time Variation(2)		—	—	125	ps
d-t_F	Fall Time Variation(2)		—	—	125	ps
d_{T3}	Duty Cycle(2)	Measurement from differential waveform	45	—	55	%

NOTES:
1. SRC clock outputs run only at 100MHz.
2. This parameter is guaranteed by design, but not 100% production tested.
3. All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

ELECTRICAL CHARACTERISTICS - CPU, SRC, AND DOT96 0.7 CURRENT MODE DIFFERENTIAL PAIR, CONTINUED(1)

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 2pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{SK3}	Skew, CPU[1:0](2)	V_T = 50%	—	—	100	ps
	Skew, CPU2(2)		—	—	250	
	Skew, SRC(2)		—	—	250	
$t_{JCYC-CYC}$	Jitter, Cycle to Cycle, CPU[1:0](2)	Measurement from differential waveform	—	—	85	ps
	Jitter, Cycle to Cycle, CPU2(2)		—	—	100	
	Jitter, Cycle to Cycle, SRC(2)		—	—	125	
	Jitter, Cycle to Cycle, DOT96(2)		—	—	250	

NOTES:
1. SRC clock outputs run only at 100MHz.
2. This parameter is guaranteed by design, but not 100% production tested.

ELECTRICAL CHARACTERISTICS - PCICLK / PCICLK_F

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 10 - 30pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ppm	Static Error(1,2)	See Tperiod Min. - Max. values	—	—	0	ppm
T_{PERIOD}	Clock Period(2)	33.33MHz output nominal	29.991	—	30.009	ns
		33.33MHz output spread	29.991	—	30.1598	
V_{OH}	Output HIGH Voltage	I_{OH} = -1mA	2.4	—	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 1mA	—	—	0.55	V
I_{OH}	Output HIGH Current	V_{OH} at Min. = 1V	-33	—	—	mA
		V_{OH} at Max. = 3.135V	—	—	-33	
I_{OL}	Output LOW Current	V_{OL} at Min. = 1.95V	30	—	—	mA
		V_{OL} at Max. = 0.4V	—	—	38	
	Edge Rate(1)	Rising edge rate	1	—	4	V/ns
	Edge Rate(1)	Falling edge rate	1	—	4	V/ns
t_{R1}	Rise Time(1)	V_{OL} = 0.8V, V_{OH} = 2V	0.3	—	1.2	ns
t_{F1}	Fall Time(1)	V_{OL} = 0.8V, V_{OH} = 2V	0.3	—	1.2	ns
d_{T1}	Duty Cycle(1)	V_T = 1.5V	45	—	55	%
t_{SK1}	Skew(1)	V_T = 1.5V	—	—	500	ps
$t_{JCYC-CYC}$	Jitter, Cycle to Cycle(1)	V_T = 1.5V	—	—	500	ps

NOTES:
1. This parameter is guaranteed by design, but not 100% production tested.
2. All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

ELECTRICAL CHARACTERISTICS, 48MHZ, USB

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 10 - 20pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ppm	Static Error(1,2)	See Tperiod Min. - Max. values	—	—	0	ppm
T_{PERIOD}	Clock Period(2)	48MHz output nominal	20.8257	—	20.834	ns
V_{OH}	Output HIGH Voltage	I_{OH} = -1mA	2.4	—	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 1mA	—	—	0.55	V
I_{OH}	Output HIGH Current	V_{OH} at Min. = 1V	-29	—	—	mA
		V_{OH} at Max. = 3.135V	—	—	-23	
I_{OL}	Output LOW Current	V_{OL} at Min. = 1.95V	29	—	—	mA
		V_{OL} at Max. = 0.4V	—	—	27	
	Edge Rate(1)	Rising edge rate	1	—	2	V/ns
	Edge Rate(1)	Falling edge rate	1	—	2	V/ns
t_{R1}	Rise Time(1)	V_{OL} = 0.8V, V_{OH} = 2V	0.5	—	1.2	ns
t_{F1}	Fall Time(1)	V_{OL} = 0.8V, V_{OH} = 2V	0.5	—	1.2	ns
d_{T1}	Duty Cycle(1)	V_T = 1.5V	45	—	55	%
$t_{JCYC-CYC}$	Jitter, Cycle to Cycle		—	—	350	ps

NOTES:
1. This parameter is guaranteed by design, but not 100% production tested.
2. All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

ELECTRICAL CHARACTERISTICS - REF-14.318MHZ

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 10 - 20pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ppm	Long Accuracy(1)	See Tperiod Min. - Max. values	—	—	0	ppm
T_{PERIOD}	Clock Period	14.318MHz output nominal	69.827	—	69.855	ns
V_{OH}	Output HIGH Voltage(1)	I_{OH} = -1mA	2.4	—	—	V
V_{OL}	Output LOW Voltage(1)	I_{OL} = 1mA	—	—	0.4	V
I_{OH}	Output HIGH Current	V_{OH} at Min. = 1V	-33	—	—	mA
		V_{OH} at Max. = 3.135V	—	—	-33	
I_{OL}	Output LOW Current	V_{OL} at Min. = 1.95V	30	—	—	mA
		V_{OL} at Max. = 0.4V	—	—	38	
	Edge Rate(1)	Rising edge rate	1	—	4	V/ns
	Edge Rate(1)	Falling edge rate	1	—	4	V/ns
t_{R1}	Rise Time(1)	V_{OL} = 0.8V, V_{OH} = 2V	0.3	—	1.2	ns
t_{F1}	Fall Time(1)	V_{OL} = 0.8V, V_{OH} = 2V	0.3	—	1.2	ns
d_{T1}	Duty Cycle(1)	V_T = 1.5V	45	—	55	%
$t_{JCYC-CYC}$	Jitter, Cycle to Cycle(1)	V_T = 1.5V	—	—	1000	ps

NOTE:
1. This parameter is guaranteed by design, but not 100% production tested.

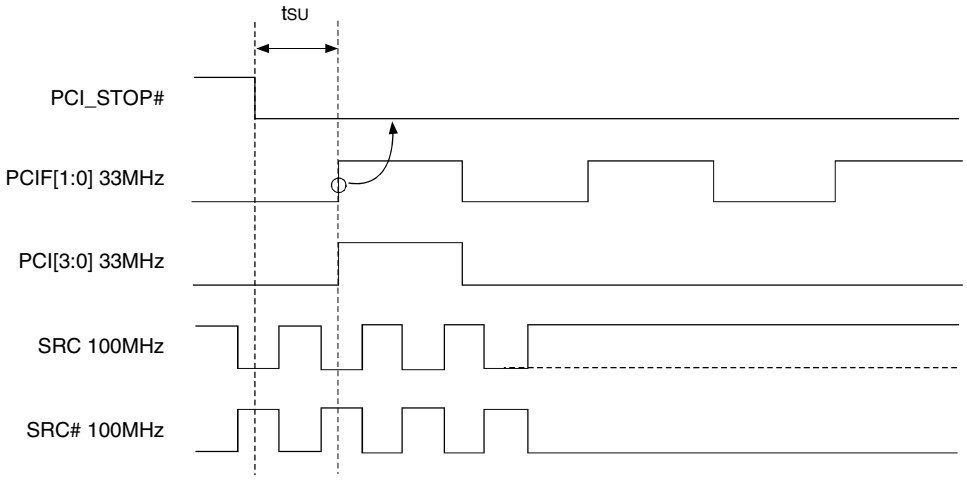
PCI STOP FUNCTIONALITY

The PCI_STOP# signal is on an active low input controlling PCI and SRC outputs. If PCIF[1:0] and SRC clocks can be set to be free-running through SMBus programming, they will ignore both the PCI_STOP# pin and the PCI_STOP register bit.

PCI_STOP#	CPU	CPU#	SRC	SRC#	PCIF/PCI	USB	DOT96	DOT96#	REF
1	Normal	Normal	Normal	Normal	33MHz	48MHz	Normal	Normal	14.318MHz
0	Normal	Normal	I_{REF} * 6 or float	Low	Low	48MHz	Normal	Normal	14.318MHz

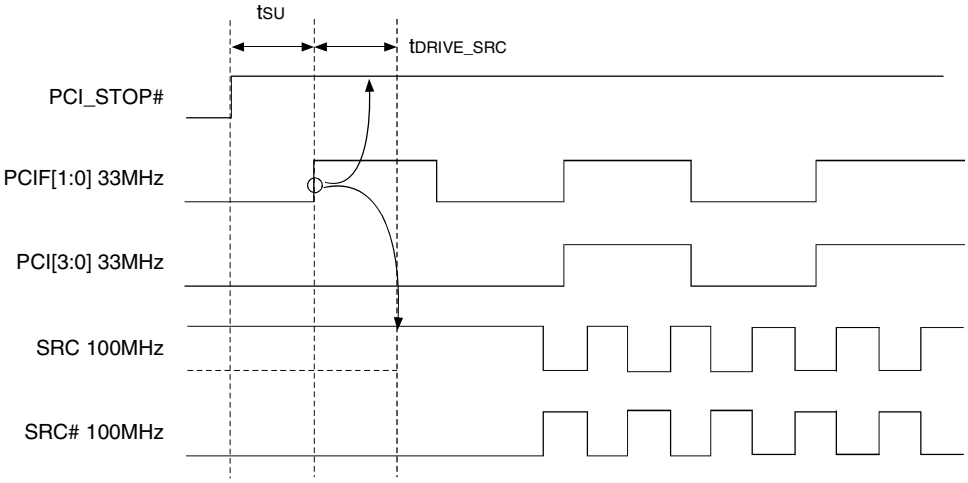
PCI_STOP# ASSERTION (TRANSITION FROM '1' TO '0')

The clock samples the PCI_STOP# signal on a rising edge of PCIF clock. After detecting the PCI_STOP# assertion low, all PCI[6:0] and stoppable PCIF[1:0] clocks will latch low on their next high to low transition. After the PCI clocks are latched low, the SRC clock, (if set to stoppable) will latch high at I_{REF} * 6 (or tristate if Byte 5 Bit 7 = 1) upon its next low to high transition and the SRC# will latch low as shown below.



PCI_STOP# - DE-ASSERTION

The de-assertion of the PCI_STOP# signal is to be sampled on the rising edge of the PCIF free running clock domain. After detecting PCI_STOP# de-assertion, all PCI[6:0], stoppable PCIF[1:0] and stoppable SRC clocks will resume in a glitch free manner.



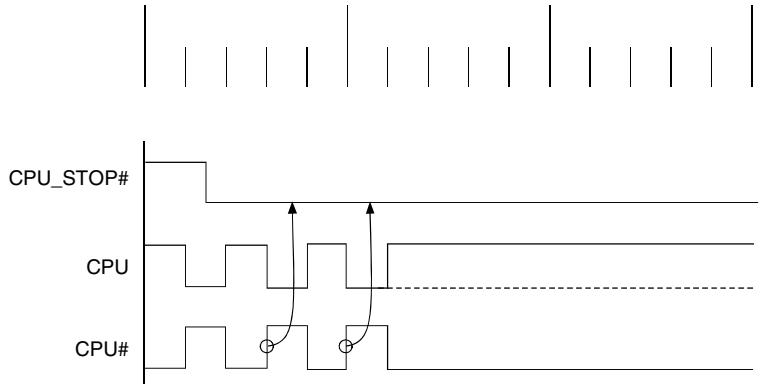
CPU STOP FUNCTIONALITY

The CPU_STOP# signal is an active low input controlling the CPU outputs. This signal can be asserted asynchronously.

CPU_STOP#	CPU	CPU#	SRC	SRC#	PCIF/PCI	USB	DOT96	DOT96#	REF
1	Normal	Normal	Normal	Normal	33MHz	48MHz	Normal	Normal	14.318MHz
0	I_{REF} * 6 or float	Low	Normal	Normal	33MHz	48MHz	Normal	Normal	14.318MHz

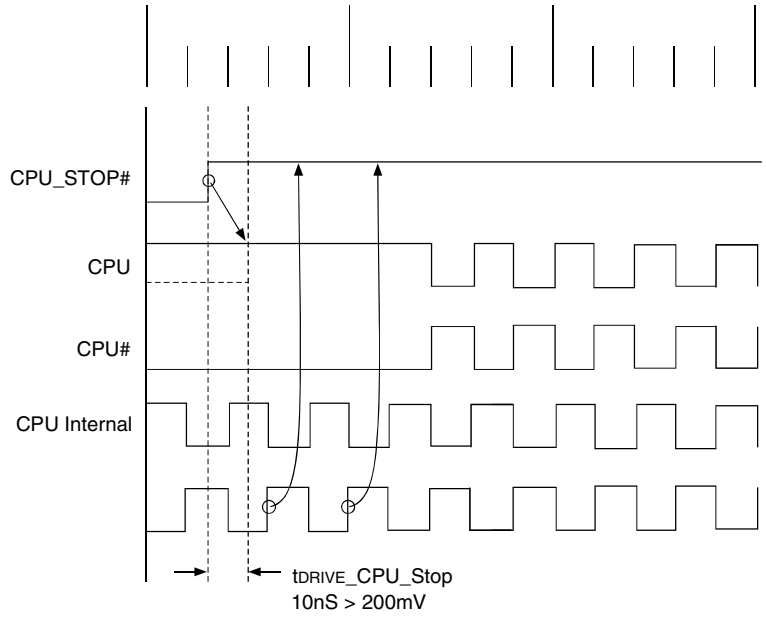
CPU_STOP# ASSERTION (TRANSITION FROM '1' TO '0')

Asserting CPU_STOP# pin stops all CPU outputs that are set to be stoppable after their next transition. When the SMBus CPU_STOP tri-state bit corresponding to the CPU output of interest is programmed to a '0', CPU output will stop CPU_True = High and CPU_Complement = Low. When the SMBus CPU_STOP# tri-state bit corresponding to the CPU output of interest is programmed to a '1', CPU outputs will be tri-stated.



CPU_STOP# - DE-ASSERTION (TRANSITION FROM '0' TO '1')

With the de-assertion of CPU_STOP# all stopped CPU outputs will resume without a glitch. The maximum latency from the de-assertion to active outputs is two to six CPU clock periods. If the control register tristate bit corresponding to the output of interest is programmed to '1', then the stopped CPU outputs will be driven High within 10nS of CPU_STOP# de-assertion to a voltage greater than 200mV.

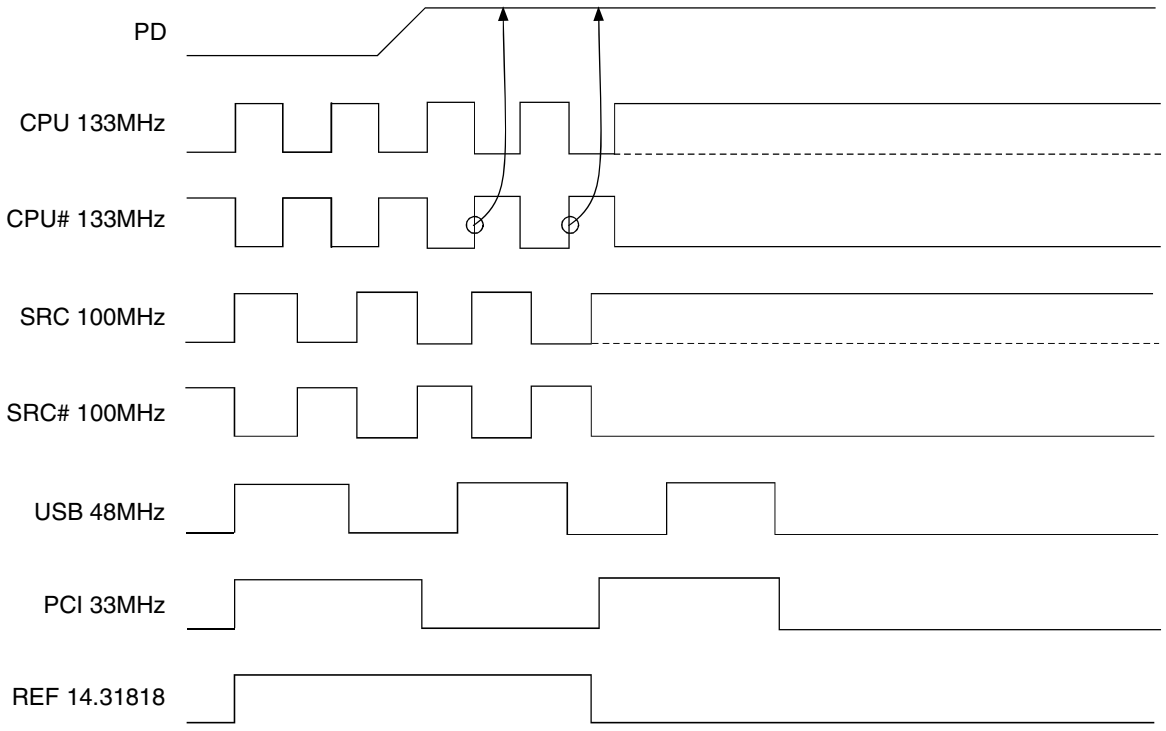


PD, POWER DOWN

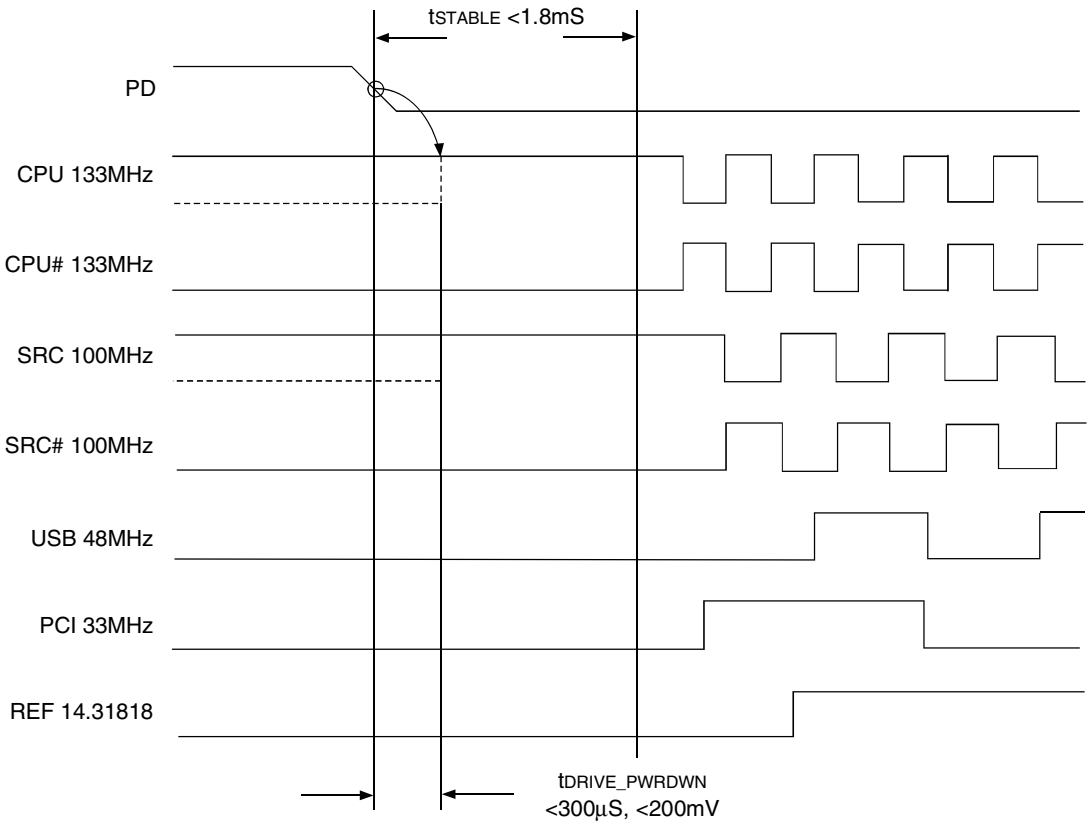
PD is an asynchronous active high input used to shut off all clocks cleanly prior to clock power. When PD is asserted high all clocks will be driven low before turning off the VCO. In PD de-assertion all clocks will start without glitches.

PD	CPU	CPU#	SRC	SRC#	PCIF/PCI	USB	DOT96	DOT96#	REF
0	Normal	Normal	Normal	Normal	33MHz	48MHz	Normal	Normal	14.318MHz
1	I_{REF} * 2 or float	Float	I_{REF} * 2 or float	Float	Low	Low	I_{REF} * 2 or float	Float	Low

PD ASSERTION



PD DE-ASSERTION



DIFFERENTIAL CLOCK TRISTATE

To minimize power consumption, CPU[2:0] clock outputs are individually configurable through SMBus to be driven or tristated during PD and CPU_STOP# mode and the SRC clock is configurable to be driven or tristated during PCI_STOP# and PD mode. Each differential clock (SRC, CPU[2:0]) output can be disabled by setting the corresponding output's register OE bit to "0" (disable). Disabled outputs are to be tristated regardless of "CPU_STOP", "SRC_STOP" and "PD" register bit settings.

Signal	Pin PD	Pin CPU_STOP#	CPU_STOPTristate Bit	PD Tristate Bit	Non-Stoppable Outputs	Stoppable Outputs
CPU	0	1	X	X	Running	Running
CPU	0	0	0	X	Running	Driven at I_{REF} x 6
CPU	0	0	1	X	Running	Tristate
CPU	1	X	X	0	Driven at I_{REF} x 2	Driven at I_{REF} x 2
CPU	1	X	X	1	Tristate	Tristate

NOTES:
1. Each output has four corresponding control register bits; OE, PD, CPU_STOP, and "Free Running".
2. I_{REF} x 6 and I_{REF} x 2 is the output current in the corresponding mode.
3. See CONTROL REGISTERS section for bit address.

Signal	Pin PD	Pin PCI_STOP#	PCI_STOPTristate Bit	PD Tristate Bit	Non-Stoppable Outputs	Stoppable Outputs
SRC	0	1	X	X	Running	Running
SRC	0	0	0	X	Running	Driven at I_{REF} x 6
SRC	0	0	1	X	Running	Tristate
SRC	1	X	X	0	Driven at I_{REF} x 2	Driven at I_{REF} x 2
SRC	1	X	X	1	Tristate	Tristate

NOTES:
1. SRC output has four corresponding control register bits; OE, PD, SRC_STOP, and "Free Running".
2. I_{REF} x 6 and I_{REF} x 2 is the output current in the corresponding mode.
3. See CONTROL REGISTERS section for bit address.

TRISTATE DOT96 CLOCK CONTROL

Signal	Pin PD	PD Tristate Bit	Output
DOT96	1	X	Running
DOT96	0	0	Driven at I_{REF} x 2
DOT96	0	1	Tristate

NOTES:
1. DOT output has two corresponding control register bits; OE and PD.
2. I_{REF} x 6 and I_{REF} x 2 is the output current in the corresponding mode.
3. See CONTROL REGISTERS section for bit address.

LVDS AC TIMING REQUIREMENTS

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{R1}	Clock Rise Time[1,2,3]	175	—	700	ps
t_{F1}	Clock Fall Time[1,2,3]	175	—	700	ps
Δt_R	Clock Rise Time Variation[2,3,4]	—	—	125	ps
Δt_F	Clock Fall Time Variation[2,3,4]	—	—	125	ps
	Rise/Fall Matching[2,3,5]	—	—	20	%
V_{HIGH}	Voltage HIGH[2,3,6]	660	700	850	mV
V_{LOW}	Voltage LOW [2,3,7]	-150	0	—	mV
$V_{CROSS(ABS)}$	Crossing Voltage (abs)[2,3,8,9,10]	250	—	550	mV
$V_{CROSS(REL)}$	Crossing Voltage (rel)[2,3,10,11]	Calc.	—	Calc.	
$T_{OTAL}\ \Delta\ V_{CROSS}$	Total Variation of V_{CROSS} Over All Edges[2,3,12]	—	—	140	mV
$t_{JCYC-CYC}$	Cycle-to-Cycle Jitter[2,13]	—	—	350	ps
d_{T3}	Duty Cycle[2,13]	45	—	55	%
V_{OVS}	Maximum Voltage Allowed at Output (overshoot)[2,3,14]	—	—	V_{HIGH} + 0.3V	V
V_{UDS}	Minimum Voltage Allowed at Output (undershoot)[2,3,15]	-0.3	—	—	V
V_{RB}	Ringback Margin[2,3]	n/a	—	0.2	V

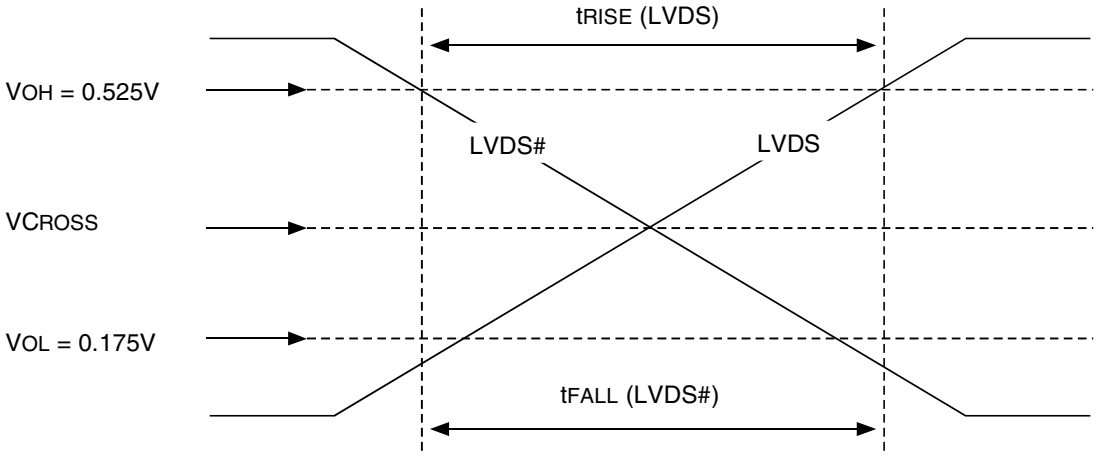
NOTES:
1. Measured from V_{OL} = 1.75V to V_{OH} =0.525V. Only valid for Rising LVDS and Falling LVDS#. Signal must be monotonic through the V_{OL} to V_{OH} region for t_{RISE} and t_{FALL}.
2. Test configuration is Rs = 32.2Ω, Rp = 49.9Ω, 2pF.
3. Measurement taken from single-ended waveform.
4. Measured with oscilloscope, averaging off, using Min. Max. statistics. Variation is the delta between Min. and Max.
5. Measured with oscilloscope, averaging off, the difference between the t_{RISE} (average) of LVDS versus the t_{FALL} (average) of LVDS#.
6. V_{HIGH} is defined as the statistical average HIGH value as obtained by using the oscilloscope V_{HIGH} math function.
7. V_{LOW} is defined as the statistical average LOW value as obtained by using the oscilloscope V_{LOW} math function.
8. Measured at crossing point where the instantaneous voltage value of the rising edge of LVDS equals the falling edge of LVDS#.
9. This measurement refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing.
10. The crossing point must meet the absolute and relative crossing point specifications simultaniously.
11. V_{CROSS} (rel) Min. and Max. are derived using the following: V_{CROSS} (rel) Min. = 0.25V + 0.5 (V_{HAVG} - 0.7V), V_{CROSS} (rel) Max. = 0.55V + 0.5 (0.7V - V_{HAVG}).
12. Δ V_{CROSS} is defined as the total variation of all crossing voltages of Rising LVDS and Falling LVDS#. This is the maximum allowed variance in V_{CROSS} for any particular system.
13. Measurement is taken from differential waveform.
14. Overshoot is defined as the absolute value of the maximum voltage.
15. Undershoot is defined as the absolute value of the minimum voltage.

LVDS AVERAGE PERIOD, TPERIOD(1,2,3,4)

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C

Spread	96MHz		100MHz		Unit
	Min.	Max.	Min.	Max.	
0% (no spread)	10.406	10.427	9.99	10.01	ns
0.8% down-spread	10.406	10.511	9.99	10.09	ns
1% down-spread	10.406	10.531	9.99	10.11	ns
1.25% down-spread	10.406	10.557	9.99	10.135	ns
1.5% down-spread	10.406	10.583	9.99	10.16	ns
1.75% down-spread	10.406	10.61	9.99	10.185	ns
2% down-spread	10.406	10.636	9.99	10.21	ns
2.5% down-spread	10.406	10.688	9.99	10.26	ns
3% down-spread	10.406	10.74	9.99	10.31	ns
±0.3% down-spread	10.375	10.458	9.96	10.04	ns
±0.4% down-spread	10.365	10.469	9.95	10.05	ns
±0.5% down-spread	10.354	10.479	9.94	10.06	ns
±0.6% down-spread	10.344	10.49	9.93	10.07	ns
±0.8% down-spread	10.323	10.511	9.91	10.09	ns
±1% down-spread	10.302	10.531	9.89	10.11	ns
±1.25% down-spread	10.276	10.557	9.865	10.135	ns
±1.5% down-spread	10.25	10.583	9.84	10.16	ns

NOTES:
1. Test configuration is Rs = 32.2Ω, Rp = 49.9Ω, 2pF.
2. The average period over any 1µS period of time must be greater than the minimum and less than the maximum specified period.
3. Measurement is taken from differential waveform.
4. Calculated using a ±0.1% accuracy in spread modulation. Assumes 300ppm long term accuracy on CLKIN.



Single-Ended Measurement Point for t_{RISE} and t_{FALL}

MISCELLANEOUS AC TIMING REQUIREMENTS

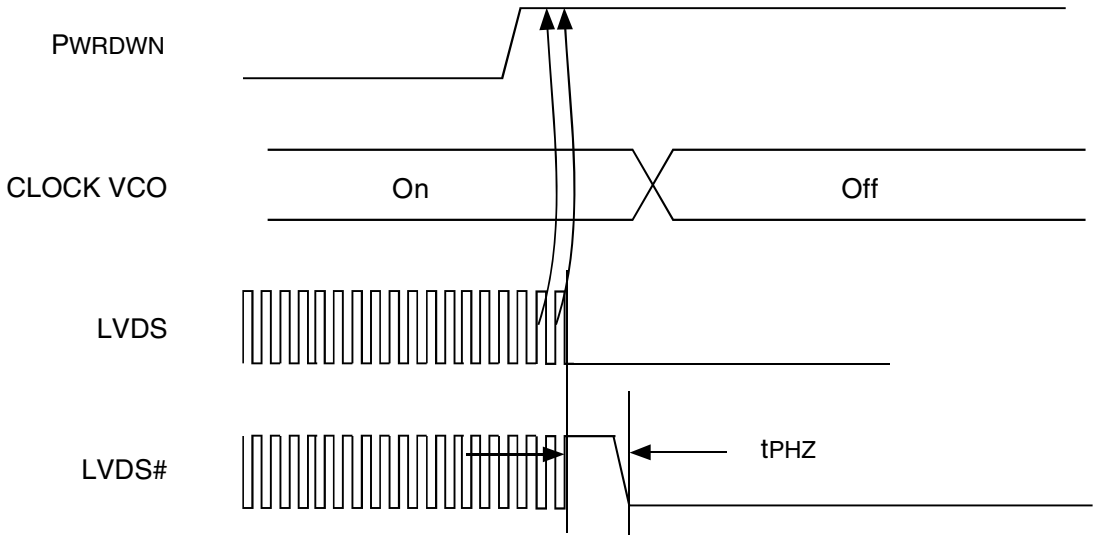
Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{PZL} t_{PZH}	Output Enable Delay (All Outputs)[1]	0	—	10	µs
t_{PLZ} t_{PHZ}	Output Disable Delay (All Outputs)[1]	0	—	10	µs
t_{STABLE}	All Clock Stabilization from Power-Up[2]	—	—	3	ms
t_{SPREAD}	Setting Period for Spread Selection Change[2,3]	—	—	3	ms

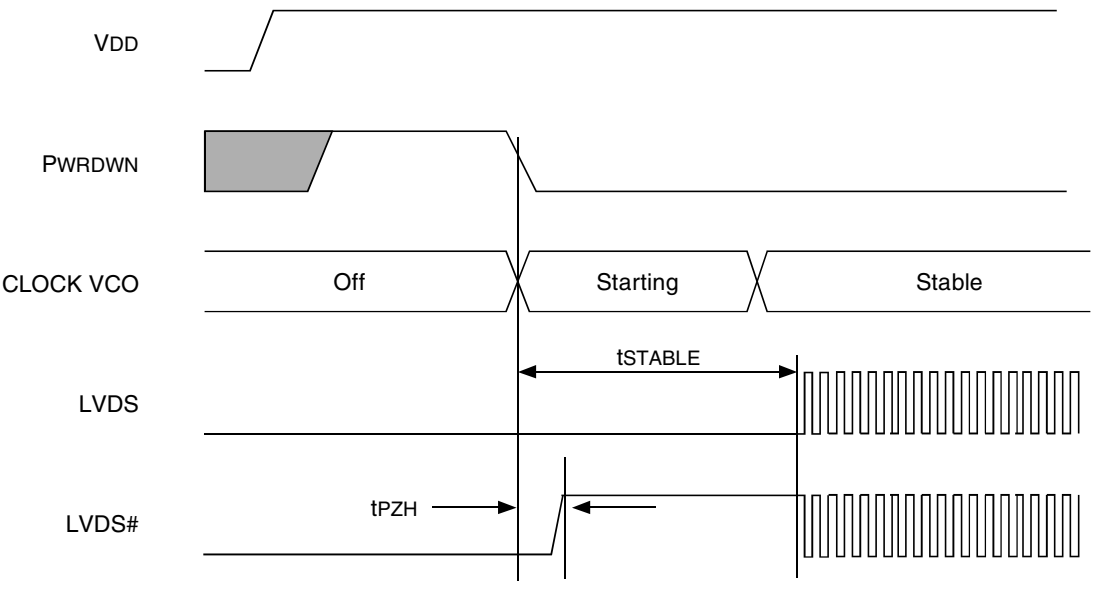
NOTES:

1. These specifications apply to the LVDS and SMBus pins. These pins must be tri-stated when P_{WRDWN} is asserted. LVDS is driven differential when P_{WRDWN} is de-asserted unless it is disabled.
2. The time specified is from when V_{DD} achieves its nominal operating level (typical condition V_{DD} = 3.3V) and P_{WRDWN} is de-asserted until the frequency output is stable and operating within specification.
3. The time specified is measured from the spread selection change or output frequency change until the LVDS clock is operating at the new spread modulation and frequency. If there is another change in spread selection or output frequency during the t_{SPREAD} settling period, then the settling period start resets to the most recent change in spread selection and output frequency.

PWRDWN (POWER DOWN) CLARIFICATION



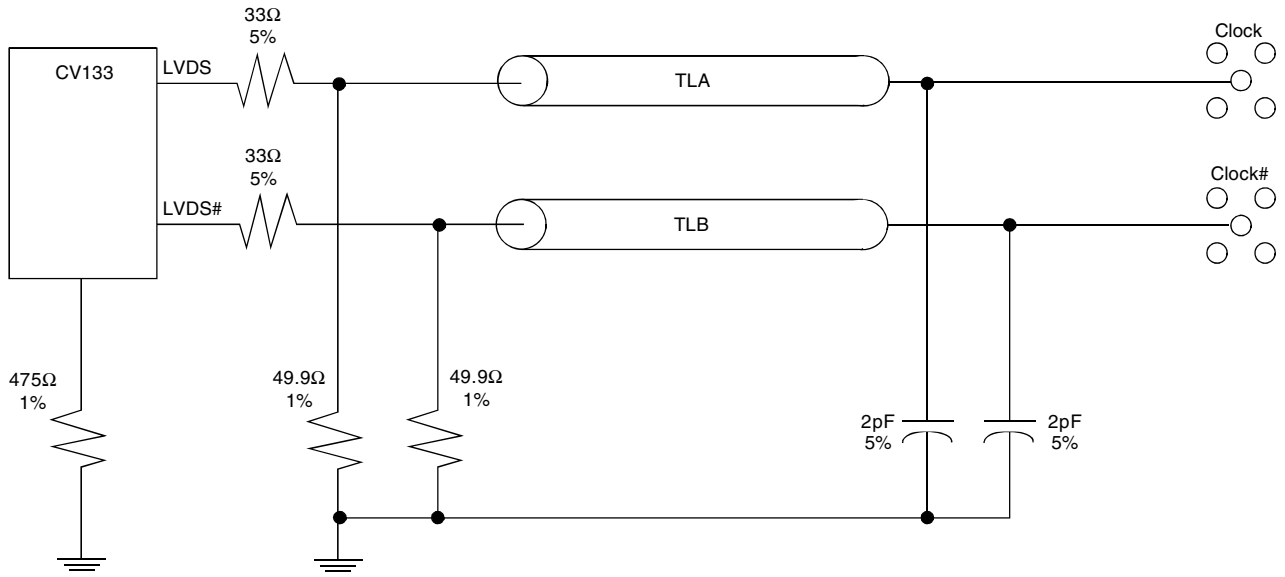
PWRDWN Assertion



PWRDWN De-Assertion

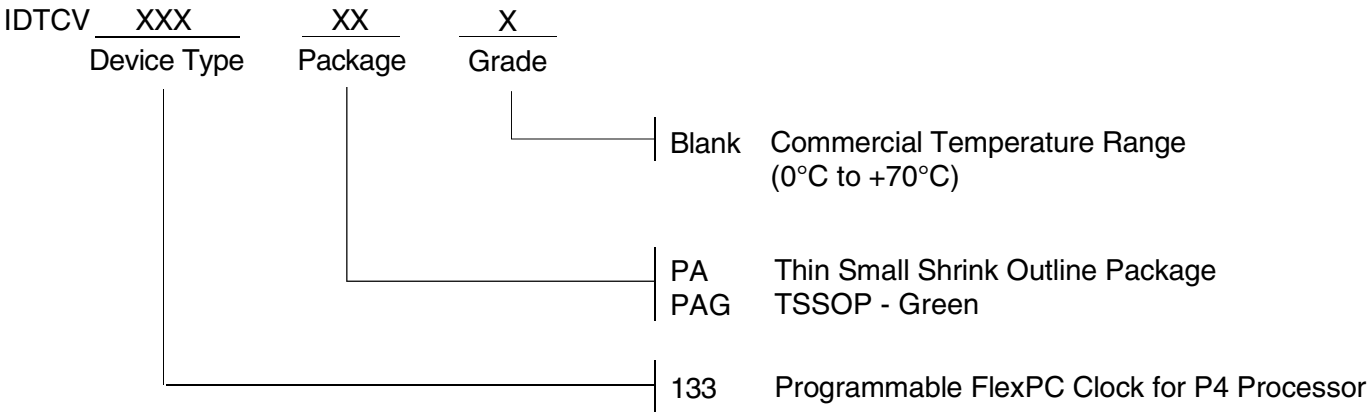
LVDS SYSTEM IMPLEMENTATION

Clock	Rs	Rp	Unit
LVDS Clock	33.2 5%	49.9 1%	Ω



Test Load Board Configuration

ORDERING INFORMATION



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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

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