EL7154

High Speed, Monolithic Pin Driver

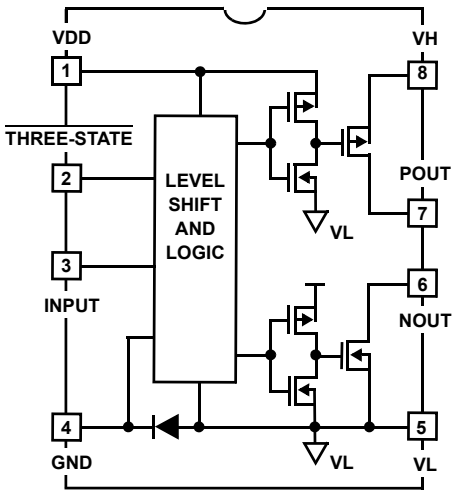
FN7278
Rev 4.00
November 23, 2015

The EL7154 three-state pin driver is particularly well suited for ATE and level shifting applications. The 4A peak drive capability, makes the EL7154 an excellent choice when driving high speed capacitive lines.

The P-Channel MOSFET is completely isolated from the power supply, providing a high degree of flexibility. Pin (7) can be grounded, and the output can be taken from pin (8) when a “source follower” output is desired. The N-Channel MOSFET has an isolated drain, but shares a common bus with pre-drivers and level shifter circuits. This is necessary to ensure that the N-Channel device can turn off effectively when V_L goes below GND. In some power-FET and IGBT applications, negative drive is desirable to insure effective turn-off. The EL7154 can be used in these applications by returning V_L to a moderate negative potential.

Pinout

EL7154
(8 LD PDIP, 8 LD SOIC)
TOP VIEW



Truth Table

THREE-STATE	INPUT	P_{OUT}	N_{OUT}
0	0	Open	Open
0	1	Open	Open
1	0	HIGH	Open
1	1	Open	LOW

Manufactured under U.S. Patent Nos. 5,334,883, #5,341,047, #5,352,578, #5,352,389, #5,351,012, #5,374,898

Features

- Comparatively low cost
- Three-State output
- 3V and 5V Input compatible
- Clocking speeds up to 10MHz
- 20ns Switching/delay time
- 4A Peak drive
- Isolated drains
- Low output impedance: 2.5Ω
- Low quiescent current: 5mA
- Wide operating voltage: 4.5V to16V
- Isolated P-Channel device
- Separate ground and V_L pins
- Pb-free available (RoHS compliant)

Applications

- Loaded circuit board testers
- Digital testers
- Level shifting below GND
- IGBT drivers
- CCD drivers

Ordering Information

PART NUMBER	PART MARKING	PACKAGE	PKG. DWG. #
EL7154CNZ **(No longer available, recommended replacement: EL7154CSZ)**	EL7154CN Z	8 Ld PDIP* (Pb-free)	MDP0031
EL7154CSZ (See Note)	7154CSZ	8 Ld SOIC (Pb-free)	M8.15E
EL7154CSZ-T7** (See Note)	7154CSZ	8 Ld SOIC (Pb-free)	M8.15E
EL7154CSZ-T13** See Note)	7154CSZ	8 Ld SOIC (Pb-free)	M8.15E

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

**Add “-T” or “-TK” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Nominal Operating Voltage Range

PIN	MIN	MAX
V_L	-3	0
V_{DD} to V_L	5	15
V_H to V_L	2	15
V_{DD} to V_H	-0.5	15
V_{DD}	5	15

Absolute Maximum Ratings (T_A = +25°C)

Supply (V_{DD} to V_L; V_H to V_L, V_H to GND),
V+ to V_H. 16.5V
V_L to GND . . . . . -5V
Input Pins. . . . . -0.3V below V_L to +0.3V above V_{DD}
Peak Output Current 4A

Thermal Information

Storage Temperature Range . . . . . .-65°C to +150°C
Ambient Operating Temperature . . . . . .-40°C to +85°C
Operating Junction Temperature . . . . . .+125°C
Power Dissipation
SOIC 570mW
PDIP* 1050mW
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp
*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

1. Limits established by characterization and are not production tested.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

DC Electrical Specifications

T_A = +25°C, V_{DD} = +12V, V_H = +12V, V_L = -3V, unless otherwise specified.

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT						
V_{IH}	Logic “1” Input Voltage		2.4			V
I_{IH}	Logic “1” Input Current	$V_{IH} = V_{DD}$		0.1	10	µA
V_{IL}	Logic “0” Input Voltage				0.6	V
I_{IL}	Logic “0” Input Current	V_{IL} = 0V		0.1	10	µA
V_{HVS}	Input Hysteresis			0.3		V
OUTPUT						
R_{OH}	Pull-Up Resistance	I_{OUT} = -100mA		1.5	4	Ω
R_{OL}	Pull-Down Resistance	I_{OUT} = +100mA		2	4	Ω
I_{OUT}	Output Leakage Current	V_{DD}/GND		0.2	10	µA
I_{PK}	Peak Output Current	Source/Sink		4.0		A
I_{DC} (Note 1)	Continuous Output Current	Source/Sink	200			mA
POWER SUPPLY						
I_S	Power Supply Current	Inputs = V_{DD}		1	2.5	mA
V_S	Operating Voltage		4.5		16	V
I_G	Current to GND (Pin 4)			1	10	µA
I_H	Off Leakage at V_H	Pin 8 = 0V		1	10	µA

AC Electrical Specifications

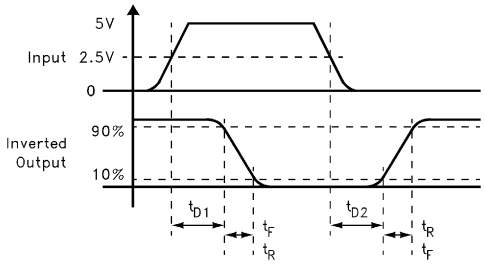
T_A = +25°C unless otherwise specified.

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS ($V_{DD} = V_H$ = 12V; V_L = -3V)						
t_R (Note 1)	Rise Time	C_L = 100pF		4	25	ns
		C_L = 2000pF		20		ns
t_F (Note 1)	Fall Time	C_L = 100pF		4	25	ns
		C_L = 2000pF		20		ns
t_{D-1} (Note 1)	Turn-Off Delay Time	C_L = 2000pF		20	25	ns

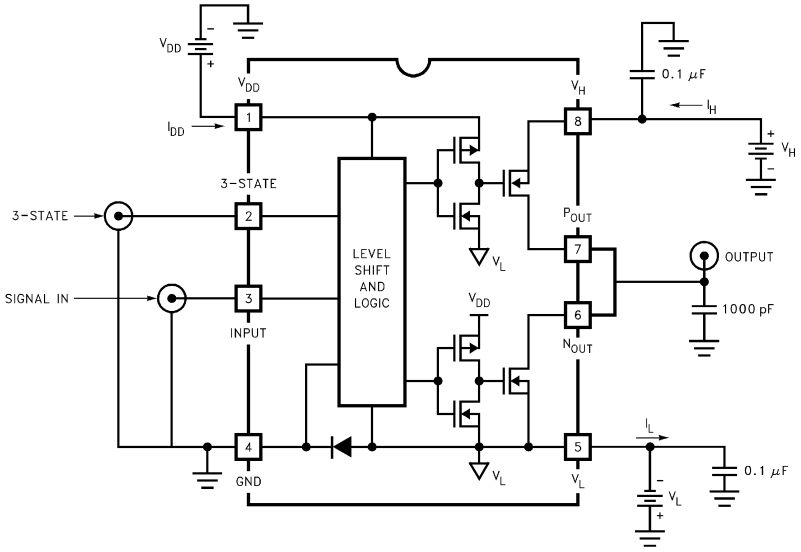
AC Electrical Specifications T_A = +25°C unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{D-2} (Note 1)	Turn-On Delay Time	C_L = 2000pF		10	25	ns
t_{D-1} (Note 1)	Three-State Delay				25	ns
t_{D-2} (Note 1)	Three-State Delay				25	ns

Timing Table



Standard Test Configuration



Typical Performance Curves

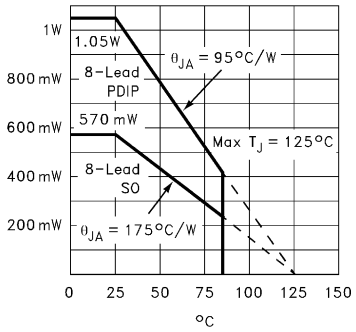


FIGURE 1. MAX POWER DERATING CURVES

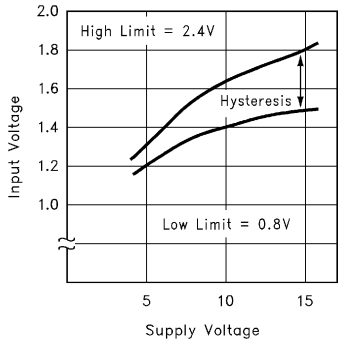


FIGURE 2. SWITCH THRESHOLD vs SUPPLY VOLTAGE

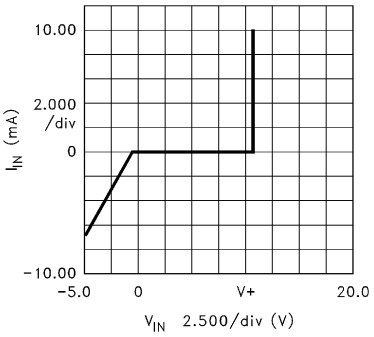


FIGURE 3. INPUT CURRENT vs VOLTAGE

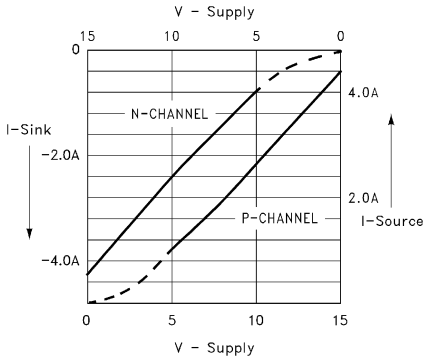


FIGURE 4. PEAK DRIVE vs SUPPLY VOLTAGE

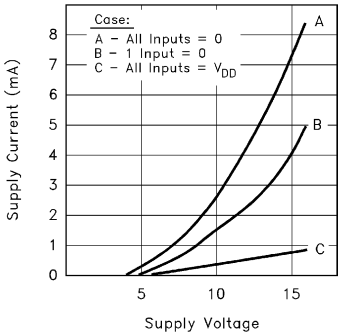


FIGURE 5. QUIESCENT SUPPLY CURRENT

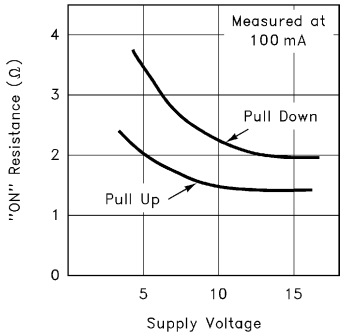


FIGURE 6. "ON" RESISTANCE vs SUPPLY VOLTAGE

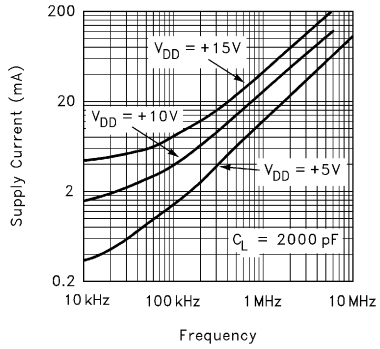


FIGURE 7. AVERAGE SUPPLY CURRENT vs VOLTAGE AND FREQUENCY

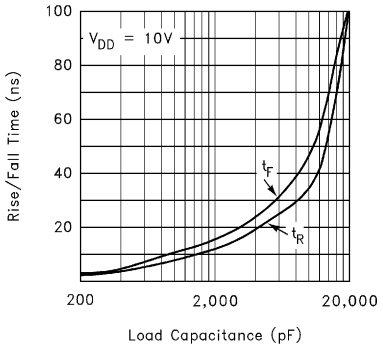


FIGURE 8. RISE/FALL TIME vs LOAD

Typical Applications

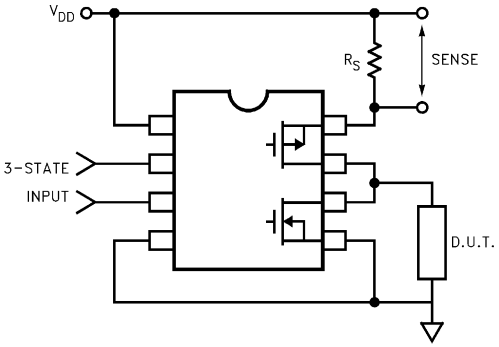


FIGURE 9. PIN DRIVER

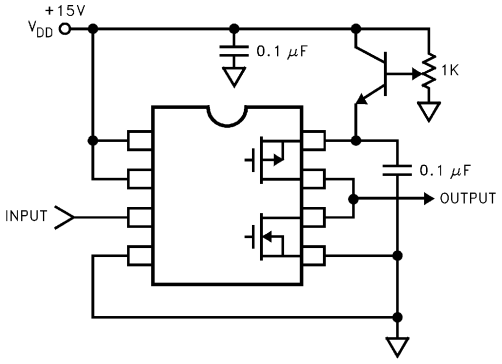


FIGURE 10. ADJUSTABLE AMPLITUDE PULSE GENERATOR

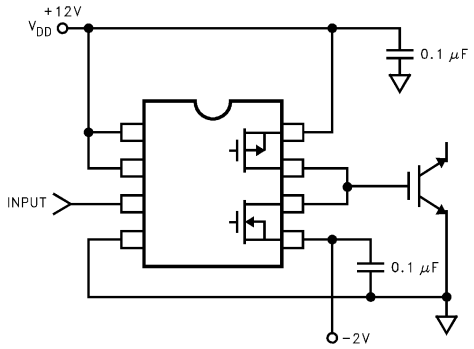


FIGURE 11. IGBT DRIVER WITH NEGATIVE SWING

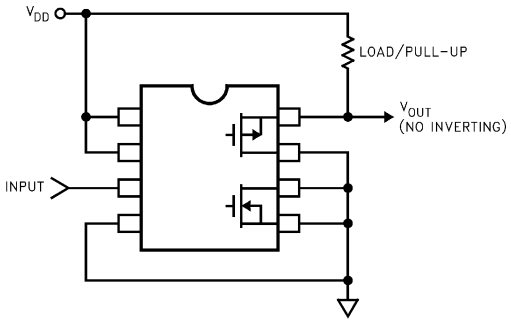


FIGURE 12. PMDS FOLLOWER

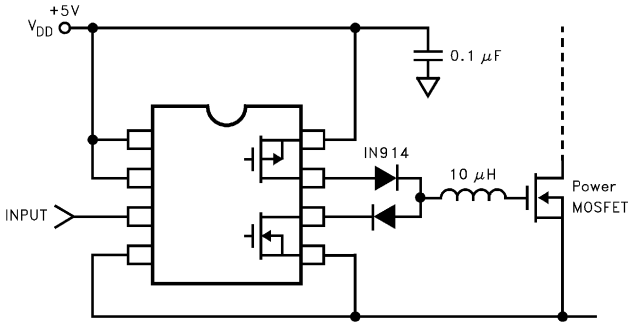


FIGURE 13. RESONANT GATE DRIVER

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
November 23, 2015	FN7278.4	- Updated Ordering Information Table on page 2. - Added Revision History. - Added About Intersil Verbiage. -Changed POD MDP0027 to POD M8.15E.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

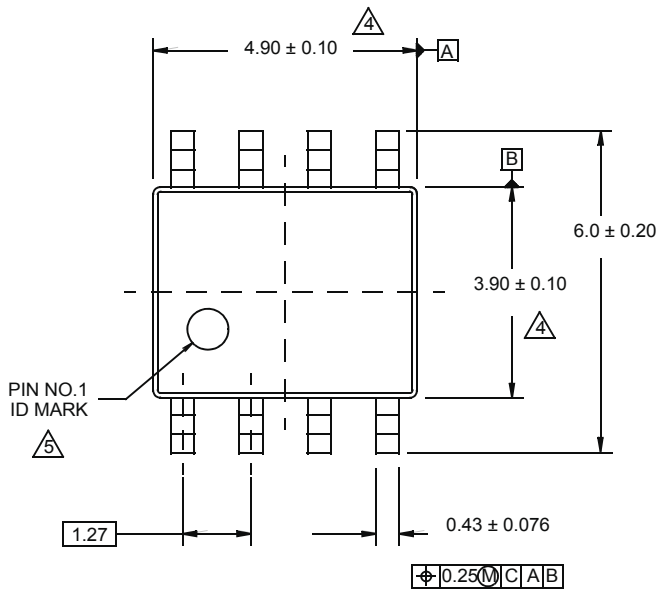
You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support.

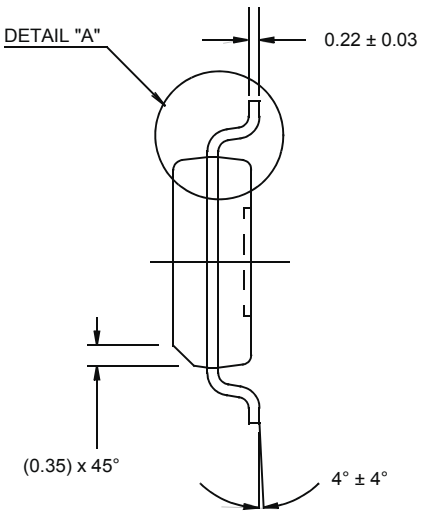
Package Outline Drawing

M8.15E

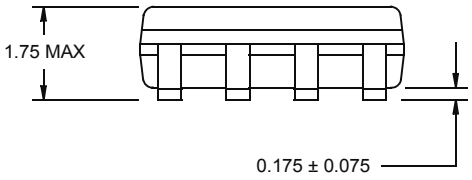
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE
Rev 0, 08/09



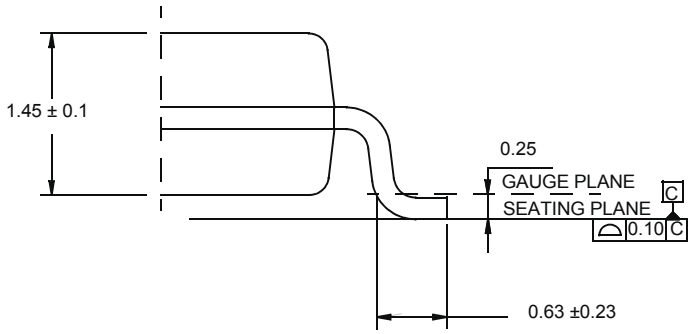
TOP VIEW



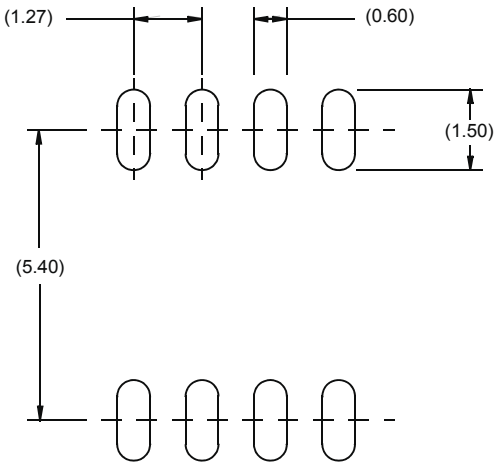
SIDE VIEW "B"



SIDE VIEW "A"



DETAIL "A"

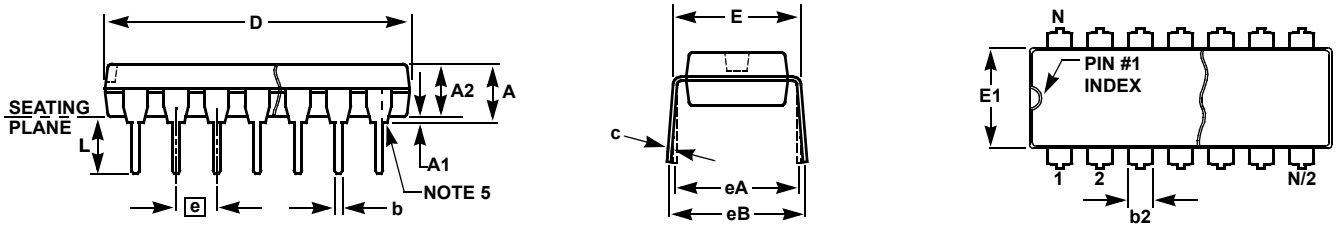


TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.

Plastic Dual-In-Line Packages (PDIP)



MDP0031

PLASTIC DUAL-IN-LINE PACKAGE

SYMBOL	INCHES					TOLERANCE	NOTES
	PDIP8	PDIP14	PDIP16	PDIP18	PDIP20		
A	0.210	0.210	0.210	0.210	0.210	MAX	
A1	0.015	0.015	0.015	0.015	0.015	MIN	
A2	0.130	0.130	0.130	0.130	0.130	±0.005	
b	0.018	0.018	0.018	0.018	0.018	±0.002	
b2	0.060	0.060	0.060	0.060	0.060	+0.010/-0.015	
c	0.010	0.010	0.010	0.010	0.010	+0.004/-0.002	
D	0.375	0.750	0.750	0.890	1.020	±0.010	1
E	0.310	0.310	0.310	0.310	0.310	+0.015/-0.010	
E1	0.250	0.250	0.250	0.250	0.250	±0.005	2
e	0.100	0.100	0.100	0.100	0.100	Basic	
eA	0.300	0.300	0.300	0.300	0.300	Basic	
eB	0.345	0.345	0.345	0.345	0.345	±0.025	
L	0.125	0.125	0.125	0.125	0.125	±0.010	
N	8	14	16	18	20	Reference	

Rev. C 2/07

NOTES:

1. Plastic or metal protrusions of 0.010” maximum per side are not included.
2. Plastic interlead protrusions of 0.010” maximum per side are not included.
3. Dimensions E and eA are measured with the leads constrained perpendicular to the seating plane.
4. Dimension eB is measured with the lead tips unconstrained.
5. 8 and 16 lead packages have half end-leads as shown.